

# THE **pcb** **design** MAGAZINE

AUGUST 2016

SPECIAL ANNOUNCEMENT

I-Connect007



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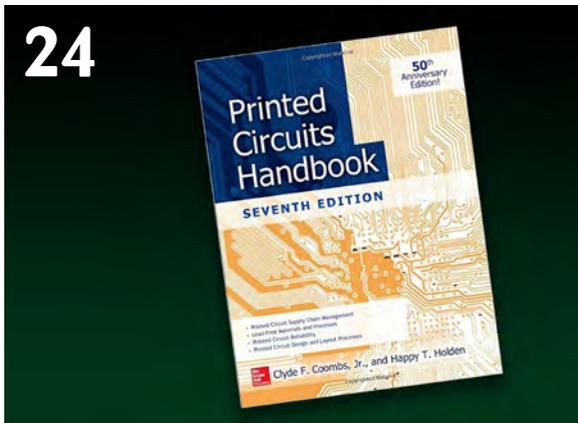
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# Voices of the Industry

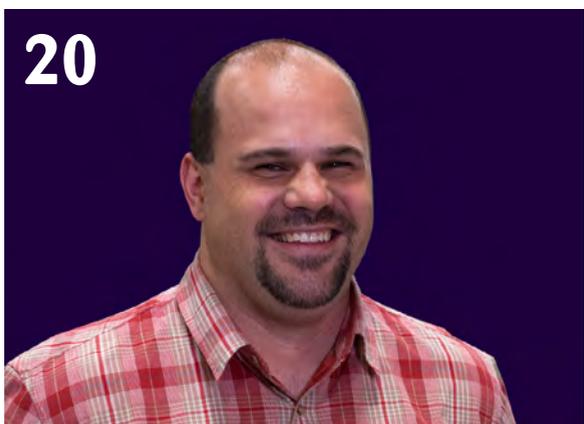
In most issues, we focus on the technical challenges facing PCB designers and design engineers. But this month, we've turned the spotlight on our readers with our special edition, *Voices of the Industry*. We asked for your thoughts on PCB design and the electronics industry, and—as usual—you weren't shy about telling us exactly what you think. So read on!



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The logo for Isola Group, featuring the word "isola" in a bold, lowercase, red sans-serif font.



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# Voices of the Industry

by **Andy Shaughnessy**

I-CONNECT007

It's good to switch things up. This month, we did just that.

Most issues of *The PCB Design Magazine* focus on technical challenges that our readers are facing, or will be facing soon. It is a technical magazine, after all. And other times we delve deeper into more high-level problems that can affect your job, such as upcoming legislation or onshoring.

But in the end, this magazine is for you. One day, we editors started thinking, "What if we asked the readers to talk directly to us, and tell us what's on their mind?"

So, in a survey, we asked readers like you to share some of your thoughts about PCB design, design engineering, and the electronics manufacturing industry in general. We even provided a few helpful "trigger" statements to get your brains firing right, including, "If they would just do this..." and "If I were in charge..." But my favorite has to be "This is really stupid, but we do it all the time..." Haven't we all made one of these statements at some point in our professional lives?

The result is this issue, *Voices of the Industry*. This issue is a snapshot of the PCB design community—a look at where we are now, and what challenges and opportunities you all are facing.

Your replies were all over the map. Of course, as journalists, we are drawn to your complaints and challenges—our publications exist to help you address these challenges. And you were not shy about sharing your complaints, that's for sure! It's funny to see how designers' main complaints haven't changed much in the years that I've been covering this segment.

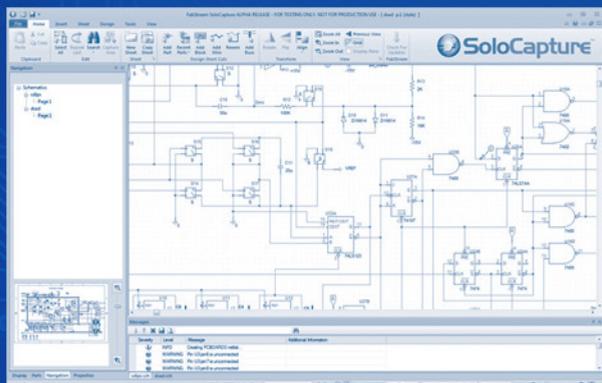
But if this issue is any indication, you all are pretty upbeat about your careers, if not your current company. You may not like everything about your job, but you all seem to really love what you do. And how many people can honestly say they love what they do?

As part of our *Voices of the Industry* coverage, we've included an index to all of the interviews—written and video—that we've conducted over the past year or so. It's quite a list. We're constantly interviewing technologists and executives at trade shows and conferences,

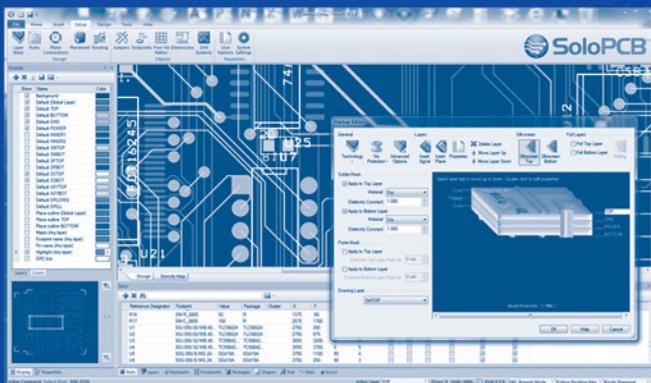


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## Join the Community

Our online community is dedicated to all electronics enthusiasts and is a place where you can download tutorials, post your questions and ideas.



including plenty of “non-PCB” events that focus on flexible displays and LEDs, for example. We’ve done so many interviews that it’s easy for readers to miss one or two over time.

So check out our handy interview index; it can help you catch up on any of our tête-à-têtes that you may have missed. It’s even alphabetical by last name.

Another Voice of the Industry, by any calculation, is the *Printed Circuits Handbook*. This “Bible of the industry” is now in its seventh edition, and editors Clyde F. Coombs and Happy Holden are celebrating the ubiquitous tome’s 50<sup>th</sup> anniversary. So, this month we asked the editors and authors of the new edition to discuss their contributions to the book, and what it was like working on such a seminal publication.

The editors and some of the veteran authors share stories that read like a timeline of the 20<sup>th</sup> century PCB industry. Shameless plug: I wrote the EDA tools chapter, the first ever in the history of the handbook, and I’m just happy to be in such great company. As I say in my part of this feature, working with Clyde and Happy was effortless, and a lot of fun too.

And no *Voices of the Industry* issue would be complete without a nod to Alex Stepinski, winner of our “Good for the Industry” award. Alex

designed the manufacturing lines at Whelan Engineering, making Whelan the first new captive shop in decades. Whelan was spending \$7 million annually having PCBs made in China; Alex created a fully automated PCB shop at Whelan, with zero waste water discharge, for only \$12 million, thus bringing the work back to the U.S. and setting a standard for other OEMs. In fact, Alex gives tours of the shop for any other OEMs who wish to follow his lead and keep production in-house. Alex is definitely “Good for the Industry.”

As September approaches, we’re getting ready for trade show season again. We’ll be attending PCB West, SMTA International, TPCA, Electronica, and HKPCA. If you can’t make it to the show, don’t worry—we’ll bring all you the coverage you need.

See you next month. **PCBDESIGN**



**Andy Shaughnessy** is managing editor of *The PCB Design Magazine*. He has been covering PCB design for 17 years. He can be reached by clicking [here](#).

## Lithium-ion Batteries: Capacity Might be Increased by Six Times

A team from the Helmholtz-Zentrum Berlin (HZB) Institute of Soft Matter and Functional Materials has observed for the first time in detail how lithium ions migrate into thin films of silicon. It was shown that extremely thin layers of silicon would be sufficient to achieve the maximal load of lithium.

Lithium-ion batteries provide laptops, smart phones, and tablet computers with reliable energy. However, electric vehicles have not gotten as far along with conventional lithium-ion batteries. This is due to currently utilised electrode materials such as graphite only being able to stably adsorb a limited number of lithium ions, restricting the capacity of these batteries.

Now a team from the HZB Institute for Soft Matter and Functional Materials headed by Prof. Matthias Ballauff has directly observed for the first time a lithium-silicon half-cell during its charging

and discharge cycles.

She discovered two different zones during her investigations. Near the boundary to the electrolytes, a roughly 20-nm layer formed having extremely high lithium content: 25 lithium atoms were lodged among 10 silicon atoms.

After discharge, about one lithium ion per silicon node in the electrode remained in the silicon boundary layer exposed to the electrolytes. Seidhofer calculates from this that the theoretical maximum capacity of these types of silicon-lithium batteries lies at about 2300 mAh/g.

These are substantial findings that could improve the design of silicon electrodes: very thin silicon films should be sufficient for adsorbing the maximum possible amount of lithium, which in turn would save on material and especially on energy consumed during manufacture—less is more.



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In this issue of *The PCB Design Magazine*, we're focusing on you, the PCB designers and design engineers. We asked for your thoughts about PCB design and the industry in general, and we even offered a few "prompts" to get your minds going; my favorite prompt was "This is really stupid...but we do it all the time."

So, without further ado, here are the voices of the industry—your peers.



**Martyn Gaudion**  
Managing Director  
POLAR INSTRUMENTS

***If they would just do this...***

Realise that better modelling won't fix a poor design or make a low-specification material perform above its capabilities. Models allow you to get the best from the available materials, but they can't perform miracles. The important

message is that PCB designers need to understand the strengths and weaknesses of materials and feed the models with the appropriate process windows for the material in use. It's a trap that new designers have fallen into since the early days of imagining: You can drill a hole more accurately than the drill is capable of, simply by putting more decimal places on the fab drawing.

***If they would only listen...***

Just because you hear two subjects in one sentence, that doesn't necessarily mean that the factors that impact the two subjects are the same. "We are here for your comfort but primarily your safety" comes to mind. Flying in turbulent air is uncomfortable, precisely because the vertical stabiliser is larger than it needs to be to ensure the airplane can continue to fly with one failed engine. Likewise, lifeboats are self-righting for safety but (allegedly) very uncomfortable to travel in. In high-speed signal integrity, the critical factors that drive insertion loss differ from those that control impedance, and copper roughness, which aids reliability, is the enemy of the ultra-high speed signal. But

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sometimes a happy coincidence can help two seemingly unrelated issues. For example, the adoption of flat glass for better laser drilling has the beneficial side effect of a more homogenous dielectric constant in the base material, which is a positive.

***What I really like about the industry...***

How so many different disciplines need to work in conjunction with each other to realise the technically miraculous products we take for granted.

***My favorite tip or trick to share is...***

If you are unsure of a concept and how a system behaves, try thinking of what may happen at the extremes. For example if you are thinking about how to model pressed thickness, consider the thickness when all the layers are 100% Cu and then consider it with all the Cu removed. Apply this kind of thinking to any mathematical challenge, and it gives you a min and max to start working from.



**Abby Monaco, CID**  
Product and Marketing  
Director  
INTERCEPT TECHNOLOGY

***If they would just do this...***

One of my duties is trying to help steer software projects and priorities. As I continually cull information and make recommendations, I do find myself wishing that there was more love in the industry. First, between EDA software vendors, and second, between manufacturers and EDA software vendors.

Speaking of the friction between EDA vendors, it has caused our customers countless headaches to have larger company vendors prevent us access to their so-called “open” technology partnership programs. On the surface, these programs are intended to help the individuals behind the software grappling with the need to move among different vendors. But in

reality, they only operate on the surface—they look good to the engineering managers of said customers, but do nothing to help the actual designers with the real problems to solve.

There is also a gray middle ground between PCB design and manufacturing, where manufacturers and software vendors are doing very good work to help ease the transitions between the worlds. But a lot of the time, a happy solution for all involves custom coding on one side or another, and this custom code may or may not work for the long term because it goes between these two worlds that don’t exactly talk the same language. I do wish there was a bit more standardization of processes among manufacturers, though I also see clearly that it’s not an easy problem to solve.

***If they would only listen...***

Talk the finer points of politics and religion, mixed in with some banter about kids and grandkids. Political correctness is anathema around here.

***If I were in charge...***

Shoes would be optional. Nap time would be encouraged. Commuting would be out of the question.

***What I really like about the industry/my company is...***

What I really like about Intercept is our collective dedication, our expectation of nothing but the highest quality, and the positive attitude everyone brings in meeting that expectation. All facets of the company work together closely every day, and we never lose sight of our goal: to please our customers, prospects, and partners. I also don’t think I’ve ever heard anyone say a bad thing about Intercept. We’ve always been a friendly, work hard, play hard sort of company.

***My favorite tip or trick to share is...***

Be friends with everyone, and enemy to no one. There is no “us” and no “them” in this industry. We are all just individuals with the same choice to make. Remember that you never know how bad a day your coworker is really having. Assume it’s worse than you think, and let the

kindness flow. Cue the Kumbaya. I don't know when I got this love happy.



**Joel Krawczyk**  
Electrical Engineer  
LINX TECHNOLOGIES

### ***If they would just do this...***

PCB fab shops should do a better job at clearly defining design rules. I constantly get mixed results from turning in designs for DFM review. I could turn in the exact same design three times and get three totally different sets of suggestions.

### ***If they would only listen...***

Impedance matching should be the responsibility of the design engineers. The fab house should not be responsible for hitting a target impedance for signal traces by manipulating the substrate thickness and resin content. With that said, the design engineer needs better information about the electrical properties of the material that is available.

### ***This is really stupid... but we do it all the time...***

Sometimes as designers, we are forced to follow reference designs even if they are flawed, because our management does not understand the complexity of the problems and does not trust the engineers to get it right.

### ***If I were in charge...***

EE courses would include much more circuit design. Designers need better training. There is an enormous amount of conflicting information out there about circuit design. A student may take one layout class at a trade show or something, then take another layout class and get totally different and conflicting information.

### ***What I really like about the my company is...***

My company understands that the PCB is the heart of system, and we don't just treat it as another line on the BOM.

### ***My favorite tip or trick to share is...***

Importing mechanical components and enclosures, using 3D mode to check mechanical fit of the whole system.

### **Chris McKernan**

Director of Research  
and Development  
CID CORPORATION

### ***If they would just do this...***

The past decade has had a steep decline in product repairability. Companies choose to treat functional details such as service manuals and schematics as highly classified intellectual property. This paired with devices getting smaller and smaller makes repair difficult for most independent repair shops and encourages a throwaway mentality. Where 25 years ago electronics were sold with detailed service manuals (or they were attainable through the manufacturer) and schematics were typically right on the device, now we choose to dispose of the device and purchase a new better one with no attempt to make a repair. This may be great for the industry for sales, but does a disservice to the consumer and the environment.

It's time for the industry to begin making service information available again, and start to stand behind the products they have produced, not just the new devices they are releasing tomorrow.



**Vern Solberg**  
 Consultant  
 SOLBERG TECHNICAL  
 CONSULTING

***If they would just do this...***

As a manager and owner of a design service company, I had the opportunity to shepherd a product from conception, prototype, pre-production evaluation and finally implementation into high-volume manufacturing. Most designers today really don't have that opportunity. This may be in part due to the geographic distance between design and manufacturing sites or, as I have seen too often, the designer is discouraged by management from emerging outside the design domain. The PCB designers I meet at technical conferences are, with few exceptions, eager to learn how to make the product perform better, exceed reliability goals and ensure manufacturing efficiency.

The designer, whenever the opportunity arises, must get up close to every aspect of the manufacturing process. Become familiar with alternative materials and visit multiple suppliers to review each stage of board fabrication, as well as robotic assembly processing and automated electrical testing. Most suppliers will welcome your interest, and designers will realize that there is no single way to perform any of these tasks. However, firsthand knowledge of variations in manufacturing methodologies will enable the designer to have an opportunity to reach his producibility, performance and reliability goals the first time out.

"There is not glory in redesign, only lost time and lost time in today's competitive market can severely impact market share and profitability."



**Anaya Vardya**  
 CEO  
 AMERICAN STANDARD CIRCUITS

***What I really like about my company is...***

I believe very strongly in working closely with our customers in terms of technology, quality and finally the capability of their end-product. We are in the business of building products for other people, products that will make their products better. We, as their PCB experts, must have a complete understanding of our customers' products and what these products are for. We must constantly look out for their needs and make sure that our products benefit their end-products to the greatest extent possible.

I make it my mission to always remember that without our customers' designs, we have no product of our own. The better we understand our customers' needs, the better our products will be.

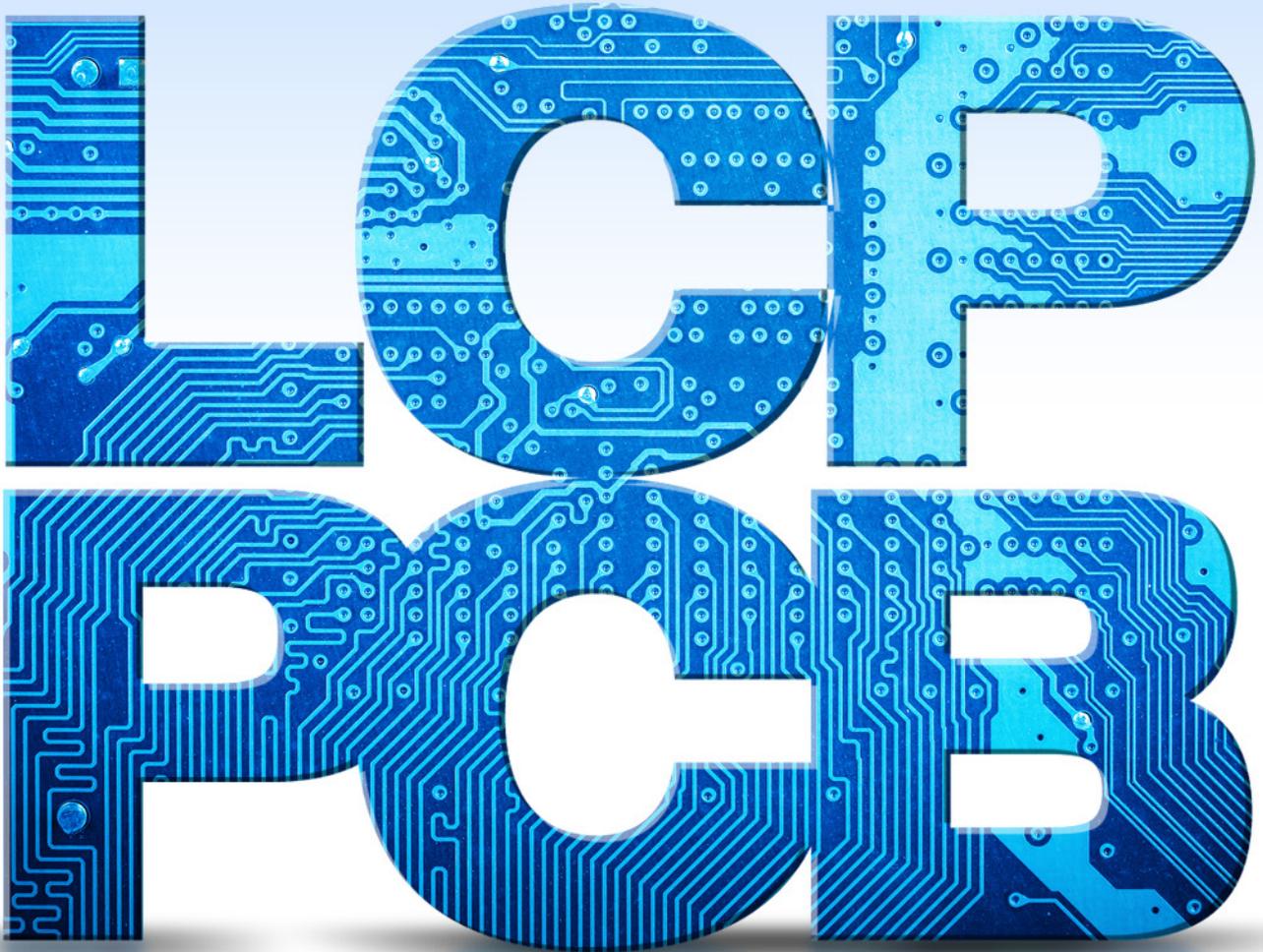


**David Ledger-Thomas**  
 PCB Design Engineer  
 HONEYWELL

***If I were in charge...***

Many of today's challenges in electronics design and manufacturing will not really be addressed until we have a completely new educational system. If I were in charge of everything, I would create a system for education and learning similar to open-source software. The open-source learning would be the beginning of a "new framework" for how to create a new model/path for running business, agriculture, organize a society, set up nations and even run the world—not in a world domination

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kind of way, but all participants could be a part of the governance through the contribution of their expertise.

They would be able to examine this open-source education system to make sure it's not doing anything they don't want it to do, and could change parts of it they don't like. Different levels might possibly be set up for the individual, the family, groups, community, regions, etc. The "establishment" would not be allowed to meddle. In fact, the establishment would become irrelevant by definition of open source.

The open source way has these components: open exchange, participation, rapid prototyping, meritocracy (the best idea wins) and community. Biases do have a part in this model, and they would have to be managed according to universal human values, basic universal social standards and basic human virtues. This might even be a way forward from the current economic conundrum. It is a conceptual model that might seem a bit utopian, but it also presents a methodology to move societies forward, and our industry would be just one of the beneficiaries.



**Dave Ryder**  
President  
PROTOTRON CIRCUITS

***What I really like about my company is...***

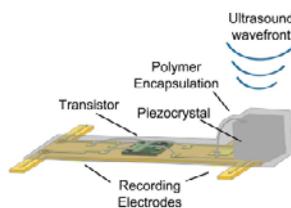
Our slogan at Prototron Circuits is "The design is not complete until the board is built." To me, this sums it all up. We are in the quick turn prototype business, so our customers often come to us with ideas that are not fully developed. We help the customer completely develop their ideas and then build the boards that complement those ideas.

Many times, our boards complete the new product that the customer is building, and it is often the first time that they will see their product work. This means that we have to do everything we can to give them the best PCBs we can possibly give them, and help these products work in the best way possible. This is our responsibility, and our duty: to complete their design.

**Implantable 'Neural Dust' Enables Precise Wireless Recording of Nerve Activity**

Now, as described in results published today in the journal *Neuron*, a DARPA-funded research team led by the University of California, Berkeley's Department of Electrical Engineering and Computer Sciences has developed a safe, millimeter-scale wireless device small enough to be implanted in individual nerves, capable of detecting electrical activity of nerves and muscles deep within the body, and that uses ultrasound for power coupling and communication. They call these devices "neural dust." The team completed the first in vivo tests of this technology in rodents.

The prototype neural dust "motest" currently measure 0.8 millimeters x 3 millimeters x 1 millimeter as assembled with commercially available



components. The researchers estimate that by using custom parts and processes, they could manufacture individual motest of 1 cubic millimeter or less in size—possibly as small as 100 microns per side. The small size means multiple sensors could be placed near each other to make more precise recordings of nerve activity from many sites within a nerve or group of nerves.

This proof of concept was developed under the first phase of the program. The research team will continue to work on further miniaturizing the sensors, ensuring biocompatibility, increasing the portability of the transceiver board, and achieving clarity in signals processing when multiple sensors are placed near each other.

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# Alex Stepinski, Our First Recipient of the **Good for the Industry** Award

I-Connect007 is proud to introduce the *I-Connect007 Good for the Industry* award. This new and prestigious award is bestowed upon individuals and companies that are good for the industry.

## What exactly does “good for the industry” mean?

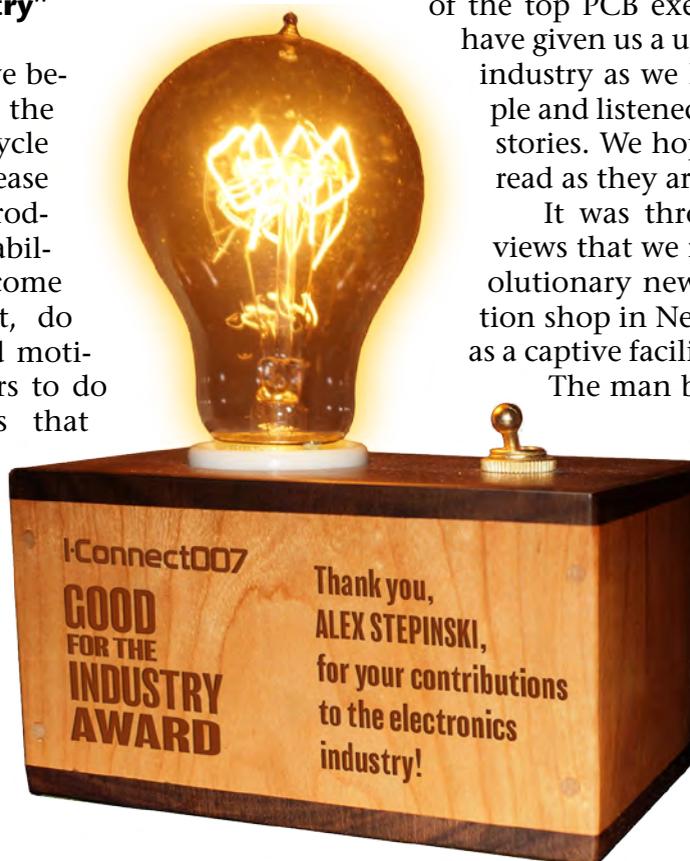
At I-Connect007 we believe it means helping the industry improve cycle time, lower cost, increase yields, build better products, increase profitability, reduce waste, become overall more efficient, do things differently, and motivate and inspire others to do the same—all things that are good for the industry.

This is what we at I-Connect007 do every day...we believe in this, and we know others do, too. We want to recognize those people that are good for the industry and share their stories.

Our goal is to consistently bring our readers fresh new content related to those characteristics listed above. Throughout the past year, the I-Connect007 team has done this by conducting interviews all over the world with hundreds of people from the industry, from congressmen to electrical engineering teenage prodigies to some of the top PCB executives. These interviews have given us a unique perspective into the industry as we have met all sorts of people and listened to, and then shared their stories. We hope they’re as much fun to read as they are to conduct.

It was through one of these interviews that we first caught wind of a revolutionary new automated PCB fabrication shop in New Hampshire, being built as a captive facility—Whelen Engineering.

The man behind the innovative design is Alex Stepinski.



## Why is Alex Stepinski good for the industry?

Alex Stepinski is good for the industry because of his first-of-a-kind, proof-of-concept creation—a fully automated PCB factory with zero waste water discharge—and his



# GOOD FOR THE INDUSTRY AWARD

and Whelen Engineering's willingness to open the doors and share their new captive manufacturing facility for others to learn from.

When designing and building the factory, Alex did not rely on the status quo. Instead, with a clear mission and a new way of thinking, he sought out and adopted leading-edge automated technology that would substantially cut manufacturing cycle time and the need for costly labor. Alex's innovative factory design has fewer than 20 people operating it on all shifts and has caught the attention of and gained recognition from some of the industry's biggest names. When I-Connect007 sat down with Gene Weiner at the most recent HKPCA show, he had this to say of the Whelen factory:

“The idea of the containment of the operating equipment, the maintenance, the effluent, and the central control overlooking the whole thing that forms a circle, from which you can side-step to do ENIG or some other special process or finish, is sheer genius in the way it was designed and built. Several pieces of equipment were created especially for that line as well as the waste treatment, such as digitizing the use of a plasma system for desmearing that uses oxygen instead of an organic. There are a lot of innovative things at Whelen.”



The Whelen factory represents the first fully automated PCB facility to open up on United States soil in decades, which is fitting because Whelen is a very pro-American company that manufactures sirens and indicator lights. Rather than continuing to spend \$7 million a year on product in China, for a little under \$12 million they were able to set up Alex's manufacturing line and start building their boards in-house. Taking chances on unproven technology and automation paid off in a big way and allowed Alex to significantly cut costs and reduce ROI. The Whelen factory offers American manufacturers evidence that adopting advanced technologies can pay off with even more opportunities in the future.

Of course, it's risky to take chances on expensive new technology when you're struggling to get by, which makes Whelen's openness even more admirable. They've offered to let anyone come in and look under the hood to see what they're doing. They want to share this technology and their unique approach with American companies.

The benefits and scope of Alex's design go beyond just North America, however. During our short visit at Whelen, a gentleman from the UK was examining the factory with hopes of setting up a similar facility in Europe. And these techniques and solutions aren't just beneficial to the West; it's expected many Asian manufacturers will be interested in Whelen's waste treatment system as environmental regulations continue

to get ramped up in China. Veteran PCB expert Happy Holden summed it up:

“Every couple of decades a “perfect storm” of opportunity presents itself to our industry. What Alex Stepinski has done at Whelen is that perfect storm! I like to call it, LEAN PLUS GREEN. Putting together a number of new innovations like inkjet printing, horizontal plating and conductive polymer metalization, along with his own innovations in water and chemical regeneration/recycling, he has cut the labor, environmental and chemical costs out of the PCB equation. This allows PCB merchants and OEMs alike to relook at the concept of re-shoring and captive production here in the USA, since waste emissions and labor costs are no longer relevant.



I congratulate Alex and his team for earning this first I-Connect007 Good for the Industry award. ”

Alex designed a factory that accomplished a number of firsts, and it looks like it could be adding more soon related to plating on plastics. It is for these ongoing accomplishments and continued innovation, as well as the willingness to share this information to further advance the industry as a whole, that we present Alex Stepinski with our *Good for the Industry* award. We’ve spent some time with Alex, and we’ve found that he is a genuinely nice guy.

If you get a chance, tour Whelen Engineering’s new PCB manufacturing facility in New Hampshire. Once you meet him, you will agree that Alex Stepinski is good for the industry.

To read the full story on Whelen Engineering and Alex Stepinski, [click here](#).

The I-Connect007 team is on a constant search for people or companies that can be considered good for the industry. If you know of someone like Alex who is *good for the industry*, let us know why, and perhaps one day it will be them being recognized in one of our magazines. **PCBDESIGN**



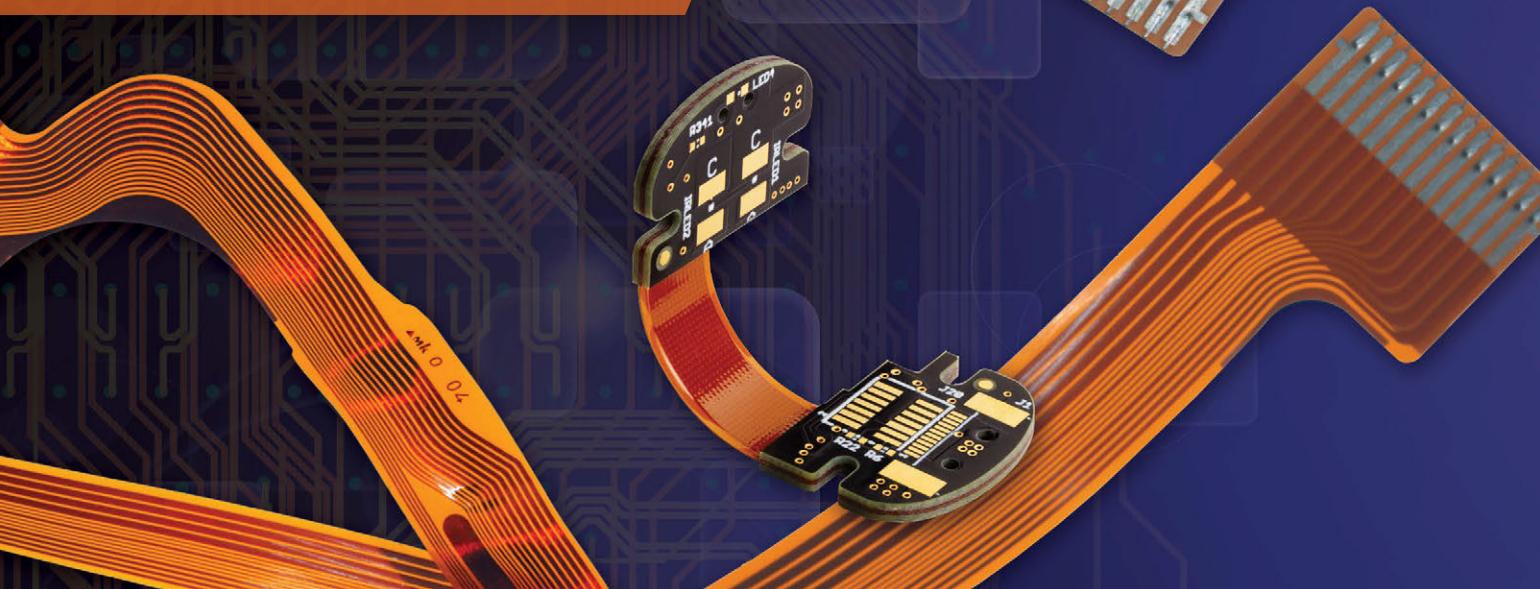
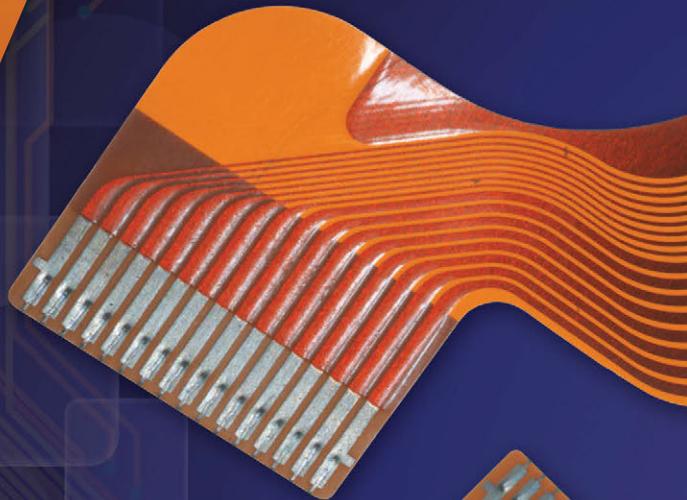
*Drone footage capturing Whelen Engineering’s fully automated PCB factory.*

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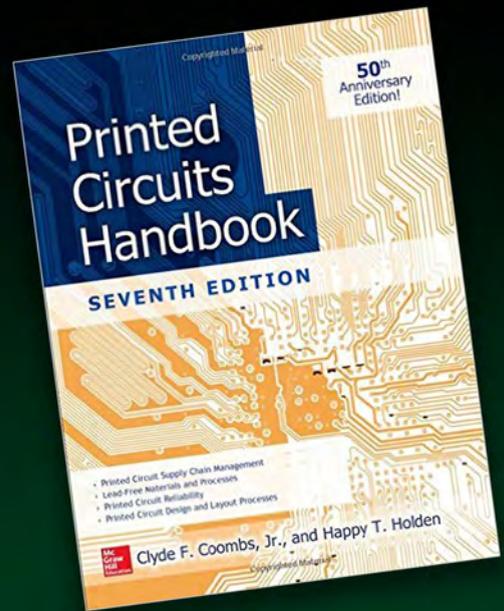
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# The Authors of the Printed Circuits Handbook Speak



*Editor's Note: The seventh edition of the Printed Circuits Handbook was published this spring, which was also the 50<sup>th</sup> anniversary of the first edition. For this issue—"Voices"—we asked the many authors of the Handbook for their thoughts—their voices. We asked a few questions to get them started; though not everyone spoke strictly about the Handbook, we found their comments interesting and thought-provoking, and we hope you do as well. We begin with a wonderful history of the Handbook by the main man himself, Clyde Coombs.*

**Clyde Coombs**  
Editor-in-Chief  
(Chapter 1)



## Background of the Printed Circuits Handbook

The *Printed Circuits Handbook* is now in its seventh edition, and we are observing the 50<sup>th</sup> anniversary of the publication of the first edition. This long-term level of importance in an industry is remarkable, but the need for this book seems obvious today. This is to put the concept of the book into the context of the industry when the first edition was published, and try to explain why there was a book in the first place, and what led to this long string of successful subsequent editions.

Touring a modern, technology- and capital-intensive, highly-automated printed circuit factory of today, supported by a staff of trained

specialists, many with advanced degrees in science, engineering and systems, would be a totally different experience than touring a printed circuit shop of 1959. For the most part, those shops were the creation of entrepreneur artisan platers or silk screeners, and the facilities were called "bucket shops" for good reasons. With the exception of IBM, Collins Radio, RCA, and a few others, along with the founding members of IPC, the estimated several thousand shops in the United States (numbers at the time ranged from 4,000 to 7,000) were operated by rules of thumb, years of experience in related trades, and generally considered an art, not a technology.

Shops were divided into two categories: captives, which made boards as a part of a vertically integrated OEM, and independents, which made and sold boards to OEMs that did not make their own. Both categories of shops could be justified since it was generally accepted that it did not take significant technical skill, or a large capital expenditure to start a shop. However, in 1959, the printed circuit world was on the brink of a major revolution that few shops were prepared to cope with, and most shop managers did not understand. The spark for this was the sudden introduction, and swift adoption, of the transistor into electronic devices. As vacuum tubes disappeared, and more functionality was designed onto much smaller boards, there was a sudden need to be able to connect circuits on both sides of a board reliably.

Entire OEM futures were being staked on whether printed circuits would even serve as an interconnection system. National advertis-



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ing campaigns were focused on the fact that the product did not use printed circuits. Hewlett-Packard's first push into this process world was a disaster, which brought into question whether a superbly engineered product could be left to the questionable quality that would result if printed circuits were the foundation of its manufacturing. At the same time, it was also obvious that, with transistors being designed into all new products, hand soldering was not a viable option, even for the short term, let alone the entire new product line.

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**“ The first try at printed circuit assembly—crimping component leads onto board pads—was slow and unreliable. ”**

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The first try at printed circuit assembly—crimping component leads onto board pads—was slow and unreliable. The next step was the use of eyelets, which had some success on single-sided boards, and was proposed as the basis for two-side connection. It's almost impossible to describe the level of controversy that existed in the electronics industry of the time over whether eyelets or plated-through-holes were the best alternative. Today, that seems laughable, but the discussion was deadly serious at the time. The general betting seemed to be on eyelets. The reasoning went as follows: It was absurd on the face of it, that a process could be developed that would plate copper on a non-conductive surface, and do it in hundreds of small holes in a board—without missing even one—while eyelets were positively put in place and missing one would be obvious.

This environment of uncertainty spawned a furious search for an alternate circuit packaging technology and resulted in some very creative proposed solutions. Most were developed for specific products, or types of products, but were often put forward as general purpose packaging

solutions. Most are now lost even to history.

As a recent graduate in electrical engineering and a new HP hire, with three years of experience in the United States Navy, my first assignment was to sort this out, propose, and develop a process that would be reliable and cost-effective, and could be integrated into the manufacturing capabilities of the company. I soon realized that they had assigned the wrong person. Instead of an EE, who could communicate with product developers, and board designers, what they really needed was a chemical engineer who could understand the chemical issues of plating and board materials. However, I had the job and needed to do a lot of learning.

First, however, I quickly eliminated eyelets, which HP was using successfully on single-sided, low volume boards, because 1) the difference in the coefficient of thermal expansion between the eyelet and the board material meant that after soldering, the two no longer could be counted on for an intimate contact, leading to potential intermittent, or open, circuits and required considerable touch-up with soldering irons; 2) eyelets had to be installed one at a time; and 3) the smaller eyelets needed for transistor interconnection were more expensive and even harder to install. That left plated through-holes, but the question remained: How could they be done reliably and consistently?

I went to the corporate library and found two books that claimed to be on printed circuits. One was really about silk screening, and the other was a high-level discussion with no real, or useful, information. The only actions left were to evaluate commercially available chemicals, and to see how others were doing it.

Giving some support to the concerns about the possibility of developing a reliable through-hole plating process was the problem that early chemical processes for reducing copper ions were very unstable. It was quite common for the solution to “go critical” and all the copper ions in solution suddenly reduce to a lump of copper at the bottom of the tank. In addition, there was a distinct interface between the copper that was deposited and the copper laminated to the base material. This required a separate sanding process to remove the copper deposited on the surface, leaving only the holes with new copper.

The result was no standard and low confidence.

Rising to meet these issues, however, a series of patents filed in the early 1960s introduced a chemistry that had a time-controlled reduction and resulted in copper deposited on the surface that did not require a sanding process. I've always felt that this was one of the most important technical advances of the twentieth century, and also the least appreciated. It became a commercial product from Shipley Chemical. We made two instruments with boards plated with this chemistry, and after full stress testing and evaluation, all discussion of eyelets stopped, and within six months all HP active boards were being made this way. The rest of the electronics industry took a little longer, but the plated through-hole has been at the heart of almost all electronic devices ever since.

At this time, the San Francisco Bay area was dominated by relatively large captive shops, with a number of small independents. I took this opportunity to leverage the Hewlett-Packard name and get invitations to visit as many of these shops as possible. The captives were just proud to show what they could do, while the independents saw us as a possible customer, but, in any case, not competitors. As a result, people were quite candid in telling me what they were doing. After a few visits, it became obvious that everybody was doing it the same way, thinking they had something unique. But it also became clear that what we were talking about was just chemistry, and of course it was basically the same. Since the people I had met did not feel competitive, I suggested that printed circuit association for our area might offer an opportunity for suppliers and users to get together to discuss technology issues confronting each. The result was the California Circuits Association (CCA). I had no idea how this would play out, but it grew from the five charter members in the Bay Area to three chapters, including two in Southern California, and more than 150 members at its peak. The biggest thing for me, however, was that I got to know who was doing what, and, more important, who really knew what.

One of the early efforts by the CCA was to hold a one-day seminar on all aspects of through-hole plating, featuring a PhD from

Stanford Research Institute, Ed Duffek, and his technical assistant, Ernie Armstrong. It included the chemistry of getting a reliable coating down in the holes. The event sold out immediately, and we could have used a much bigger auditorium and charged much more. That's how hungry people were for real information. As part of the cost of admission, we provided a summary of all the information Ed and Ernie presented (this later became the basis for the chapter on plating in the first edition).

With the success of the Plating Seminar, we asked if there were other parts of the printed circuit process that would yield similar interest and we decided that just about all parts of the process would get a big reception. However, being a volunteer organization, we did not have the resources to repeat this effort very often, and we decided to concentrate on monthly meetings.

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“ Every book that was available was done by a single author and tended to concentrate on that person's field. ”

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The need for real information was still there, however, and those with expertise in each process step were clear, so I decided that it was time to rectify the problem that there was no authoritative book on printed circuits in print. Every book that was available was done by a single author and tended to concentrate on that person's field. I felt that a contributed handbook, which is a McGraw-Hill specialty, could allow the use of a leader in each area. I made a formal proposal to McGraw-Hill based on this approach, and they sent it to a board of review for comment. One reviewer said he thought it would be OK, another said it represented a discussion of an unimportant issue and would be a huge mistake, a third said it was a great idea and McGraw-Hill would probably find they couldn't print them fast enough. The third reviewer was right.

When the book was published it went through printings as fast as McGraw-Hill could order them. Obviously, printed circuits were a very important issue, with a big, unsatisfied need for information to help technologists understand it. Large companies were buying the books by the hundreds and giving them to their entire technical teams. Small companies were using them as cookbooks. An authorized Japanese translation was quickly published, and an unauthorized reprinting appeared in Taiwan. I started getting mail and invitations to visit facilities around the world. That was 50 years ago, and the book has maintained its position as the industry's best source of information on all things printed circuits ever since. Also, as the industry has changed, so has the book, with new editions bringing new developments into focus and continuing to answer real questions. It's still a useful book about an important subject.

Looking back, I think that the key to the success of the book, from the first edition to the seventh, is the convergence of a series of points: 1) the printed circuit is the basic building block of electronic devices, and rather than receding in importance as components have seen more and higher levels of integration, it has become even more important as an application specific interconnection system; 2) it covers the entire process; 3) each chapter contains real information on how to perform processes and how things work; 4) as the need for information has developed in many parts of a company beyond manufacturing, we have put the same level of information on design and engineering issues.

Will there be an eighth edition? I can't say, but the challenges in the electronics industry haven't abated.

**Happy Holden**

Editor

(Chapters 1, 5, 16, 25, 26, 27, 43, 58, 65, 66)



**Q:** *What would you do differently for this Handbook (if you could do it over again)?*

**A:** There is nothing I would do differently, but I do have regrets. It is sad that we had to remove chapters and content in order to meet the publisher's size requirement and add all the new content that required a new edition. That is always a trade-off with a hardbound, published book. That's one reason I like e-books: they can be longer, in color, with hypertext connections and electronic searches. I have totaled the pages from the 1<sup>st</sup> edition of the handbook through the 7<sup>th</sup>. More than 1,200 pages have been removed. Most of that content was not obsolete, but used less often, or not in current practice or interest or covered in other publications that are readily available. Newcomers to our industry may never know these technologies or techniques.

The handbook also focuses on practice, not theory. So you may not understand the WHY when an author talks about the best practice. My regret is that I have nearly 35 boxes in my basement full of PCB information collected over my 45 years in the industry and very little of that found its way into the handbook. There was just too much information—most of it not available on the Internet.

Finally, we don't have a chapter called "Neat Stuff." I would love to have added a chapter on the neat stuff created over the last 45 years by printed circuit innovators. The AT&T/Western Electric metal-core additive of early rotary phone days; Pete Peligrino's flow-motion plating that would deposit a mil of copper in 15 minutes; plated-post technology that created microvias twenty years before laser drilling; Kollmorgen's Multiwire® and Microwire® boards; the unique properties of tin/nickel plating instead of nickel plating as a barrier metal; and landless vias!

**Q:** *Is there going to be an eighth edition?*

**A:** Well somebody will write it, and maybe I will edit it—if I'm still around. Most assuredly, it will be an e-Book. This industry is always changing. There will always be a need for a Handbook. Future Printed Circuit Handbooks will probably include printed electronics; metal inserts/wires and cavities for power dissipation; 3D laser-shaped circuitry on molded plastics, embedded components and new methods of optical wiring.



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My concern: who is going to write the chapters? Clyde and I found it very difficult to find the new authors for the 7<sup>th</sup> Edition. Those with the most expertise were also the busiest, and maybe didn't have time to write a chapter. Fortunately, we found those experts and they made time to help us. We are eternally grateful that they took time to help the industry. Next time, the selection may be much smaller—or for me—not English speaking.

**Q: Is there going to be enough new technology to justify an eighth edition?**

**A:** There is probably enough new technology now to start an eighth edition. The growth of digital imaging alone would need its own chapter. Not just laser direct imaging, but the use of powerful LEDs as light sources and TI's DMD micro-mirrors have started to proliferate. Inkjet printing of etch, plating, solder mask and legends is also growing. Given the use of these techniques at the new Whelen Engineering PCB fab facility, we also should bring back green technology (as it saved them a lot of money and "no permits required"). I like to call this new captive facility a "Lean plus Green" example. Lean is emphasized and results in a panel cost half that of China but with a two-day turnaround time instead of six weeks. These Lean concepts have simplified the entire PCB manufacturing process. They used horizontal pulse electroplating technology to reuse the copper from their etching process as well as other novel techniques to totally recycle all their rinse waters. It is also significant that all the technology came out of the U.S. or Europe, not Asia. But now that the cat is out of the bag, we may see more of it implemented in Asia. One key attribute is the less than three-year return on investment. Hopefully, this will now interest banks and other loaning institutions in financing more PCB factory growth in North America.

**Q: How will the Handbook be used by newcomers to the PCB profession?**

**A:** We now have a generation in college, and more coming up through K-12 schooling, that have grown up with digital devices, video

gaming, mobile phones and social networking. The effect of all of this has changed the nature of how they learn. To continue their education in electronics manufacturing—and specifically printed circuit fabrication and surface mounted assembly—we will have to adjust our training and education to this new generation of learners. For someone as old as I am, the challenge is to adapt my style of teaching to this new digital learner. I would like to work with the IPC to create a comprehensive, online, self-paced two-year and four-year degree in engineering (or at least a certificate of completion) for manufacturing in electronics that has the 7<sup>th</sup> edition of the Printed Circuits Handbook as one of its texts. PCB007 has other very good free e-books that can also be tapped in making up this new course. Given the work to create this, an eighth edition of the Handbook would have to wait until the coursework is finished.

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**Tim Rodgers**  
Adjunct Professor,  
University of Colorado  
(Chapters 3, 4, 6, 7, 8)



One area that I would have liked to explore in more detail in the latest edition of the *Printed Circuits Handbook* is the topic of supplier performance. A lot of people seem to think that the most effective way to ensure high performance is to threaten suppliers with legal action or the loss of future business. A supplier who works to avoid negative consequences may achieve a minimum level of performance, but probably not much more than that. If you expect your supplier to represent your interests when you're not actively observing their performance, you have to provide a reason for them to do so. What's in it for them?

A supplier is more likely to behave as a partner if they get something more out of the relationship than money for services rendered. What do suppliers want? The answer varies, but here are some examples:

- Large, well-known customers that they can use in their advertising to attract new customers. This is especially valuable for smaller suppliers that are looking for revenue growth.
- Technical capabilities that can be leveraged to other customers. If the customer's requirements drive the supplier to develop new technology, then the supplier will be able to attract other customers.
- Entry into new markets. Suppliers that focus on specific markets (e.g., consumer electronics, semiconductors, automotive, aerospace) are at risk due to economic and demand cycles. A diversified portfolio of customers and markets provides more stability.
- Predictable demand for better asset utilization. Suppliers are just like any other business—they like being able to confidently plan into the future. This is so important that some suppliers are willing to give a discount if the customer is willing to commit to use a fixed level of their capacity over a period of time.

Most suppliers operate with very small profit margins, and if they are in a position to choose their customers, they have to consider the cost to service each customer. If you can't give them a reason to value your business, then you shouldn't be surprised or disappointed if they don't go the extra mile.

**Andy Shaughnessy**  
 Managing Editor,  
 I-Connect007  
 (Chapter 18)



When Happy Holden asked me to contribute to the 7<sup>th</sup> edition of the *Printed Circuits Handbook*, I jumped at the chance. I still have an older edition of the book that I was given when I first started covering this industry, and just being associated with the movers and shakers of the PCB world is a real honor. I've edited Happy's articles for 17 years, so it was a little bit of a role reversal to have him editing my content. But Happy and Clyde couldn't have been easier to work with, and they really have this process down to a science.

They were great about dealing with my schedule. I still don't know how I found the time to put this chapter together. I remember working on weekends, and on Thanksgiving before and after our turkey dinner. But it was a lot of fun. Have you ever been on a video conference with Clyde and Happy?

Much of this chapter focuses on tools by the "big guys" of EDA, since they do have the lion's share of the market. But I was struck by the number of inexpensive and free PCB design software tools available. And these are solid tools that actually work well. Some of these free and budget tools are robust enough that the big EDA companies may be getting a little worried!

I'm glad to see the handbook expanding to include EDA tools and supply chain management. I think Clyde Coombs and Happy Holden deserve all the credit for updating this "Bible of the industry." If they ask for my help on the next edition, count me in.

**Bill Hargin**  
 President, Z-zero—  
 PCB Signal &  
 Power Solutions  
 (Chapter 20)



**Q:** *What would you have done differently in this Handbook?*

**A:** I do believe that the chapter Mark Montrose and I created adequately captures introductory educational material that's well-suited for people just getting into signal integrity, power integrity, and EMC. I've been doing that since the mid-'90s, and Mark, an EMC consultant, has been doing it even longer than that. I do wish there was more time to revamp the mechanical design section. That may be the focus for the next spin.

With the aging of baby boomers, like myself, I see educational materials like this book, which I use myself sometimes, as filling a critical need in the PCB design and fabrication world. In fact, my own company, which is an electronic-design software startup, is targeted, in part, to bridge that gap—taking about 20

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years of lessons learned, and putting it in a software tool.

I will say that it was tough to carve out the time to create something meaningful. I felt like I was in college again, cranking out pages and graphics into the evenings and on weekends as the deadline approached. But, it's done, and I think it'll be a helpful introduction to signal integrity.

**Q:** *Is there going to be an eighth edition?*

**A:** Heck if I know, but if there is, I'll probably double down on updating and improving the mechanical section.

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### **Suzy Webb**

**Sr. PCB Designer, Design Science**  
*(Chapter 21)*

As PCB designers, we have the responsibility to bring order and inclusion to the chaotic needs of all the groups we work with. Those groups include the circuit design, mechanical design, fabrication, assembly, test, reliability, EMI issues, data sheet and model requirements, industry standards, industry specifications, and so on. In short, we have much to understand, and many hats to wear! All that, and it is our responsibility to prevent problems as much as possible, so that the product will perform as expected, will not need re-design, and will reach the market in a timely manner.

Many of us understand these principals because we have been around the business a very long time. Unfortunately, that body of knowledge may be fading away from the newer designers. The recent recession thinned the designer ranks considerably, and other long-time designers are getting near retirement age. There are no schools or engineering classes that teach the nuances of PCB design. There are no books or classes that can teach all of the ramifications of choosing this issue over that (although the *Printed Circuits Handbook* and books on specific topics are a very good start). Some of us try to share our knowledge with newer designers by leading classes, writing articles, speaking at conferences, and consulting at businesses.

We encourage others to share their knowledge through user forums, software group meetings, and Designers Council meetings. Whether a designer is relatively new to the business, or an engineer is designing his own boards, we encourage him to read those articles or forums. Attend those classes, workshops, and conferences even if you must do it on your own time. (Many of us did it too.) Now is the time to be pro-active about your career! You will need a good foundation because there are many new challenges coming.

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**Michael Carano**  
**VP Technology and**  
**Business Development,**  
**RBP Chemical**  
**Technology**  
*(Chapter 32)*



As an industry veteran with 36-plus years of experience, I have come full circle in my belief as to how the North American electronics industry can compete in today's global economy. Many years ago I felt strongly that the North American electronics industry in general and the printed circuit board industry in particular were second to none. Then, as OEMs shifted to an outsourcing model, much of the expertise and know-how went with it. As I traveled globally I experienced this trend first hand.

First the migration of cellphones then smartphones, television sets, even semiconductors were finding a home outside of the United States. What would be the future? Well, a few data points recently allowed my belief to complete the circle. As an example, last October (2015), IPC hosted the HDI/Flex Conference in Minneapolis. The two-day event was well attended by over 115 participants. The latest information on via filling, reliability, materials and solderable finishes flowed from the experts to the audience. The PCB fabricators in attendance were some of the biggest and the best: Multek, TTM, and FTG. And all North American headquartered. Very impressive. All have a large manufacturing footprint on the continent.

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Then fast forward to the recent publication of the *Printed Circuits Handbook!* Just take a look and see the vast quality of information presented in this latest volume. You can't help but recognize that the reader would be getting a priceless education from the authors of the various chapters in the book. And just take a look and note where all these authors and editors reside. Yes, the North American electronics and printed circuit board industry is in good hands.

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**George Milad**  
National Accounts  
Manager for Technology,  
Uyemura USA  
(Chapters 33, 35)



I think that OEMs should discontinue specific process qualification and concentrate on specifying the attributes that they desire in the finished product.

The OEM may run a battery of tests on a specific vendor product and it may pass and then they specify the qualified vendor. Among the drawbacks of this method is that, defective parts may still occur as a result from variations in the processing conditions, that the manufacturer or the OEM, may not be aware of. In addition, new processes with a wider operating window may be available that the manufacturer may want to try but feels trapped in the qualified process.

Another advantage of specifying the attributes that they desire in the finished product is that the responsibility for the delivered parts remains with the manufacturer. In this case the manufacturer chooses the process that fits his shop conditions and may choose a vendor that he feels is knowledgeable and offers him the best service and problem resolution as the need arises. Some of the qualification procedures may be so extensive and cumbersome that they impede the progress of the industry as it comes up with better more robust processes that have not undergone qualification.

**Jason Keeping**  
Corporate Engineering  
Analyst, Celestica, Inc.  
(Chapter 44)



**Q:** *How was the experience of putting together your chapter of the Handbook?*

**A:** As a technology leader for our organization, I have written documents for industry in the past; however, this was my first opportunity to have information put into hard copy book not as a document but as a book, and it was a great pleasure. As the content of this chapter had not changed much in the past decade based on the legacy of information that was already available, my real goal was to find content that was new that could enhance this section for readers. With recent work that I had completed for the IPC-HDBK-830 Conformal Coating Handbook, I had this fairly easily available and just needed to confirm all aspects and have them incorporated into this handbook. After this was done the overall flow and images just needed to be amended and put more into the current century. With current industry progress on nano materials and new developments, the next time this section may have new material types as well as content to empower its readers both in hardcopy and digital form.

With the speed that our industry is developing at the moment, the amount of changes that were encountered within this edition will most likely be exponential and not linear, just to maintain a parallel path to these market innovations and changes.

**Q:** *Do you see any challenges in PCBs in general or PCB education in particular?*

**A:** Within my role I work with all market segments between military/aerospace, industrial, telecommunication and even consumer covering all aspects of ruggedization from assembly cleaning, staking, edge/corner/complete underfill, and selective/atomized/vapour/dip deposited conformal coating and even component encapsulation and full assembly potting tech-

nologies. However, these technology sectors are continuously in development due to newer material research and cost pressures to compensate for newer harsh environments than previous designs and/or even legal requirements such as RoHS and/or even local requirements connected to emission either into the air or down the drain.

With this all stated, one aspect that is a hot topic—depending on whom you discuss with—is no-clean. From the information that I have obtained over the years, this was a great marketing term; however, is not true if you have the perception that no-clean means that assembly cleaning is not required. For the bare PCB this may be true; however after you run a PCB via the SMT process, add manually and/or via automated equipment components for a wave soldering process, then perform various manual touch points such as handling for test and/or inspection, the resulting ionic levels at this point usually do not mean the assembly is clean—yet all materials are “no clean.” At this point the challenge is what the next step should be? This would be a challenge that I see coming that the industry will need to understand and what test methods and guidelines should be used and followed.

**Laura Turbini**  
International Reliability  
Consultant  
(Chapters 45, 59)



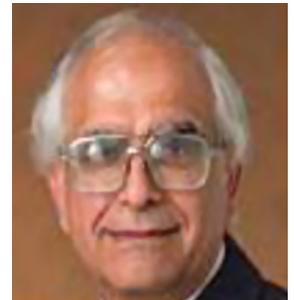
**Q:** *What do you really enjoy about the industry?*

**A:** I have had the privilege of working in the electronics industry for almost 40 years, starting in 1977 when I joined Western Electric's Engineering Research Center. As one of the early women in the industry, I was treated with respect and support by my many male associates. One thing that always impressed me in my colleagues is the way they worked together and helped each other. Over the years I had a chance to learn from the industry's leading thinkers. The insights I received from them

led me into the area of research related to failure modes in printed circuit boards—particularly to the study of CAF (conductive anodic filament) formation. “Standing on the shoulders of giants” enabled me and my students to identify the chemical nature of CAF and how it is formed.

I was first asked by Clyde Coombs to contribute to the 4th edition, which published in 1996, and subsequently to the 5th, 6th and 7th editions. The present 7th edition was very important as a central resource for lead-free soldering. Writing a technical book chapter took a great deal of time to compose it in a clear manner and to make sure there were no errors—but I had learned to do that early in my career when I was the editor of the Western Electric Engineer. I am pleased to have been a participant in this book and I hope my former students will pick up where I left off.

**Reza Ghaffarian**  
Principal Engineer,  
Jet Propulsion  
Laboratory, California  
Institute of Technology  
(or JPL/NASA, CIT)  
(Chapters 60, 61)



**Q:** *Why did you decide to write two chapters on PCB reliability for the Printed Circuits Handbook?*

**A:** Well, when I look back, I find it to be interesting, even maybe amusing, as how a simple request by Happy, a dear long-time colleague friend and a co-editor, caused me months of hard work followed by a final proud moment of accomplishment. I am not joking since this for me is another extra activity, only work during weekend since I have a day job to do and that also put additional burden of as what I can publish. Well, I said OK to a simple request of review and republish with minor modification of a previously written chapter on PCB reliability. I thought a few weekends would be OK, especially knowing the Christmas holiday of 2014 was on the way. A few weeks became more than six months of nonstop weekend work and now

a feeling of relief and accomplishment and I am concentrating on other activities. Rather just minor modification, I made a complete face-lift and one chapter becomes two, one on PTH reliability and the other on a new topic of micro reliability. My intention always has been to pay back to the industry, but this became a hefty one even though I am proud of it. I am proud to be able to add the most updated research on PCB reliability. Again, just a contribution to technical community with no financial gain.

**Q:** *It has only been a few months since the Handbook was published, but have you received any input from the industry?*

**A:** Just this month I received two emails, one asking for a good reference on PCBs and the other one had comments after review of the chapter on microvia reliability, especially on drawback of current coupon testing. Even

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“Just this month I received two emails, one asking for a good reference on PCBs and the other one had comments after review of the chapter on microvia reliability, especially on drawback of current coupon testing.”

.....

though I have heard similar comments during IPC Thermal Stress Test Methodology Subcommittee meetings, but this is on the stack microvia which is an interesting one and I like to share since it is timely too. Jerry Magera wrote that for stacked microvias, they have observed that opens may occur at temperature above the PCB T<sub>g</sub> (glass transition temperature), more typically around 220°C, it stays open through the peak temperature, followed by reconnect/closure during cooling. They have tested these

types of failures to thermal cycling, -40°C to 125°C, and found that such latent defects were undetectable. Solder float tests also does not detect these failures. They also found that current induced testing is not appropriate for acceptance test and also unable to detect microvia issues. He recommends that “the current induced test coupons should be used by PCB manufacturers to monitor their process for PTHs.” So the two chapters on PCB reliability need to be revisited to include new technologies and requirements when the co-editors decided to publish the 8<sup>th</sup> edition. I want to send my sincere appreciation to the two well-known coeditors of the 7<sup>th</sup> *Printed Circuits Handbook* for their tireless effort to put together such an invaluable new edition.

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**Joe Fjelstad**  
Verdant Electronics  
(Chapters 67, 68, 69, 71)



**Electronic Assembly...  
Is it time to remove the  
“training wheels”?**

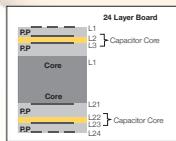
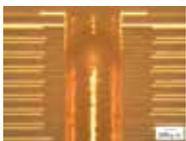
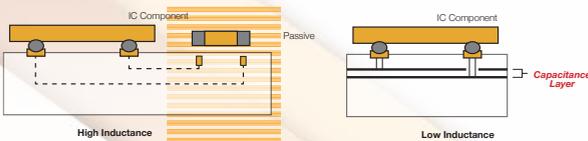
Many children learn how to ride a bicycle by using training wheels—two extra wheels attached to the rear axle to allow them to keep upright as they learn how to ride. The down side of training wheels is that they slow the rider down and impede changes in direction. In many ways, solder is the training wheels of electronic assembly. It slows down manufacturing and impedes the industry’s ability change direction when it comes to making products that are better, more reliable and less expensive. However, in order to gain those benefits, as with riding a bike, the would-be user has to exercise balance, discipline and good judgement. To illustrate, consider the following example.

Below are images of two electronic assemblies, they are identical in function and were designed by the same designer, Darren Smith<sup>[1]</sup>, using the same general design rules. Yet as can be seen, one is substantially larger than the other and has twice the number of circuit layers. What makes that possible? Three

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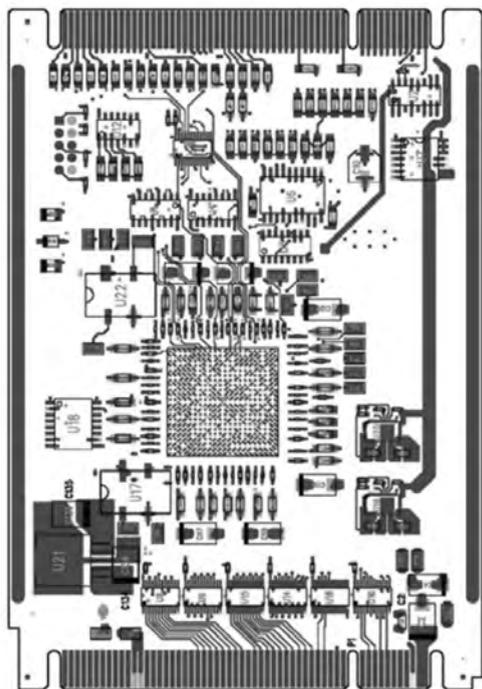
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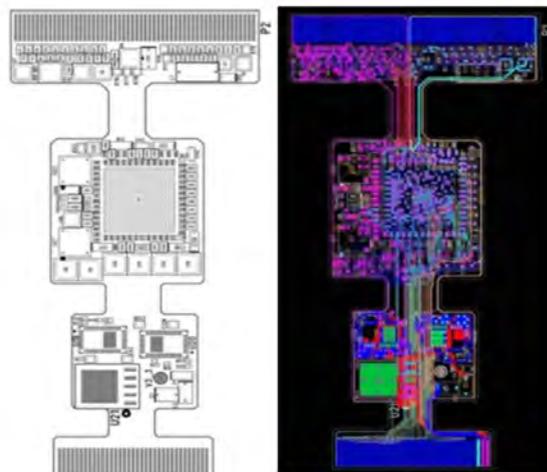
EMBEDDED CAPACITANCE

## Before



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~30mm X 40mm (when folded)  
All components on 0.5mm pitch  
50µm line/space with 50µm vias

Elimination of solder makes possible significant improvements in design efficiency.

things: the first is the elimination of solder; the second is the placement of all components (fully tested and burned in) beneath the surface with terminations facing up; and the third is selecting only components that have terminations on a common grid pitch. The combination of these three simple principles makes it all possible.

Consider first the elimination (or at least the minimization or possible replacement) of the use of solder. Solder pads take up a significant amount of space on the outer layers of a circuit assembly leaving little room for routing circuits. The fact that hundreds of millions of dollars are arguably wasted annually, inspecting, testing of PCBs and assemblies, x-raying and repairing defective solder joints seems, if one reflects without prejudice, a reasonable thing to try and eliminate. However, there is also the cleaning process which is getting ever more difficult as lead pitches shrink. Eliminate

(or replace) solder and you eliminate all of these wasted steps.

The elimination of solder is made possible (with the least number of steps) by the second item from above. That is the building of the components into the board and then applying the circuits. More succinctly, rather than building a circuit board and soldering components to the surface, build a “component board” and then build up the circuits on them. Some might consider this impractical but it can be done and fortunately while using nearly all of the current infrastructure. Circling back to the analogy that bikes work better without training wheels, the manufacturing process can as well.

The last item is perhaps the most challenging because components come with leads on many different sizes, shapes, pitches and lead forms. J-leads, gull wing leads, through-hole leads, radial leads, pins, balls and even no leads

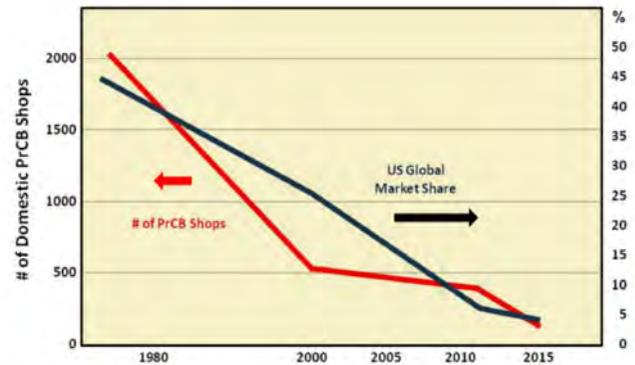
for QFNs and LGAs. It is these latter two that are of greatest interest and value because they are well-suited to getting to a standard grid (e.g., 0.5 mm). Moreover, in a solderless assembly they require no solder on their terminations. Less manufacturing steps and the elimination of high-temperature excursions which can impact long term reliability are both good things. The common grid pitch simplifies design by making routing more predictable. When all three of the principles suggested are combined, well, the results are self-evident above. It needs to be conceded here that some components cannot be easily adapted to the concept in their present configurations, but they are what they are because there were no real physical constraints when they were introduced.

In summary, it is possible to eliminate solder from numerous applications and minimize its use in countless others, and by doing so, enjoy significant benefits in design and manufacture. Not every company will be comfortable without the training wheels. They will worry about falling and it can be argued they will be less nimble as a result. Yes, eliminating the “training wheels” from electronic assembly requires some risk-taking but it is through taking risks that progress is made. It is the combined discipline of design, procurement and manufacturing that will carry the day. From experience it can be found that a key guiding principle of excellence in manufacturing is to first do the right things and then do those things right.

**P. Marc Carter**  
Printed Circuit Engineer  
(Appendix)



Those of us who deal with other aspects of electronic production realize how fortunate the printed circuit world is to have long-recognized, centralized resources like the *Printed Circuits Handbook*. The handbook (and a few other consensus resources, like IPC) allow us to



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speak in a common language. Often as not, we ARGUE, but at least we argue from a common starting point. Historically, assembly and microelectronics haven't enjoyed that same common tongue.

It is now a truly international business, and the shift of much of the fabrication base out of North America has resulted in (for an English-language resource of finite length at least) a necessary de-emphasis on fabrication details, and an increased emphasis on assembly, and securing printed circuit boards from remote sources. Another reviewer commented that an e-book that allowed the reader to focus on those areas that were of particular interest in their case might be preferable. The only other way I can think of to deal with that issue would be a two-or three-volume *Printed Circuits Handbook*, each volume addressing the needs of a particular segment. **PCBDESIGN**

To read a book review by Karl Dietz, [click here](#).

To view the Table of Contents on Amazon, [click here](#).

**References**

1. Darren Smith may be reached by [clicking here](#).



# The Many Voices Over the Past Year

## *The PCBDesign007 Interview Index*

In line with our “Voices of the Industry” theme this month, we’re publishing this handy index of all of the interviews we’ve conducted over the past year with the movers and shakers, the managers, entrepreneurs, and the rank-and-file designers and design engineers. In case you missed them the first time—we publish so much content that it’s easy to do—here’s another bite of the apple, alphabetized by the interviewee’s last name. Enjoy!



**Russ Adams, Prototron Circuits**  
[Strategies for Improving PCB Procurement](#)  
 July 23, 2015



**Nick Barbin, Optimum Design Associates**  
[Nick Barbin: From Designer to EMS Company Owner](#)  
 August 13, 2015



**Rick Almeida, DownStream Technologies**  
[What’s New at DownStream?](#)  
 The PCB Design Magazine,  
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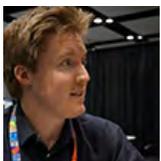
**Les Beller, EchoStar Technologies**  
[EchoStar’s Les Beller Shares the PCB Design-to-Fab Process](#)  
 May 10, 2015



**Natasha Baker, SnapEDA**  
[SnapEDA: The Female-Owned Startup Revolutionizing CAD Data](#)  
 The PCB Design Magazine,  
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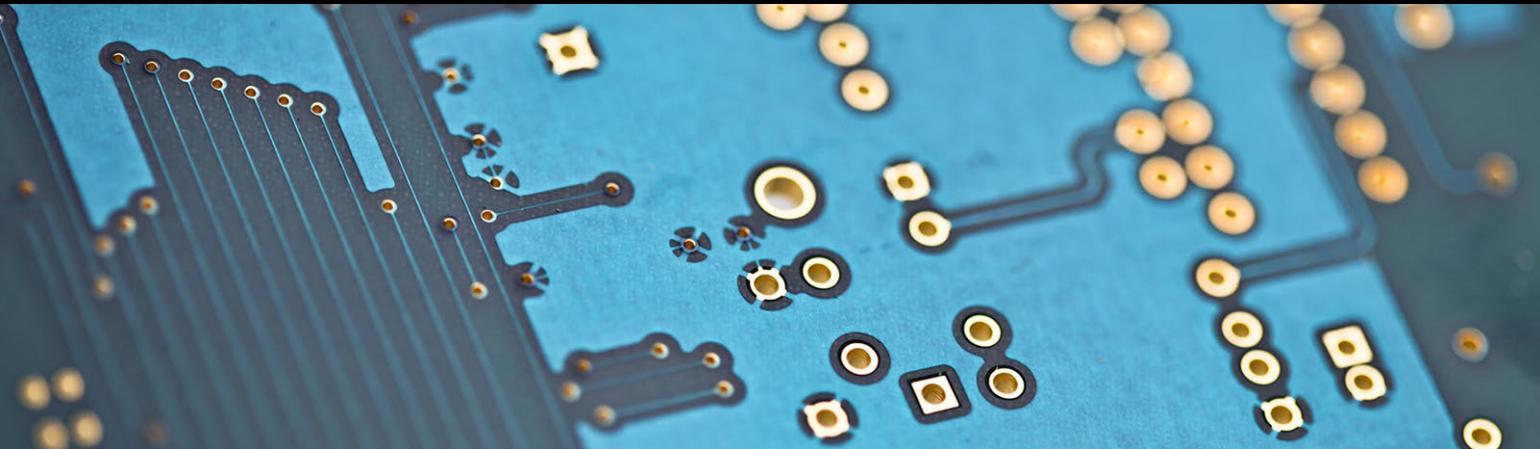
**Trenton Blizzard, Taylor Guitars**  
[Taylor Guitars Protected with Analog, RF Circuitry](#)  
 July 13, 2016



**Chris Banton, EMA Design Automation**  
[EMA Design Automation Connecting the Data with Arena PLM Software](#)

March 31, 2015

**Michael Bode and Geoffrey Hazlett, Polar Instruments**  
[Polar Talks Impedance Control and Insertion Loss Testing](#)  
 June 9, 2015



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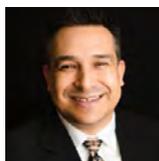
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# The Many Voices Over the Past Year



**Mike Brown**, Interconnect Design Solutions  
[The Importance of Design for Profit \(DFP\)](#)  
PCB Design Magazine, June 2016



**Stephen V. Chavez**, UTC Aerospace Systems  
[EDA Tools: Automation vs. Control](#)  
The PCB Design Magazine, May 2016

**Stephen V. Chavez**, UTC Aerospace Systems  
[UTC Aerospace Systems' Lead PCB Designer Presents at Designer Day](#)  
April 7, 2015



**Joe Clark**, DownStream Technologies  
[DownStream: What a Long EDA Trip it's Been](#)  
The PCB Design Magazine, May 2016



**John Coonrod**, Rogers Corporation  
[Rogers' John Coonrod on Insertion Loss](#)  
June 20, 2016



**Michael Creeden**, San Diego PCB  
[IPC Designers Council Viewpoint: Mike Creeden](#)  
The PCB Design Magazine, December 2015



**Andy Critcher**, Total Board Solutions Limited  
[Designers and Design Engineers: Two Sides of the Same Coin](#)  
The PCB Design Magazine, April 2016



**Kelly Dack**  
[Design Automation Tools, Today and in the Future](#)  
PCB Design Magazine, May 2016

**Kelly Dack and Mark Thompson**, Prototron Circuits  
[Kelly Dack and Mark Thompson Unite in the War on Failure](#)  
The PCB Design Magazine, August 2015

**Mehul Dave and H.D. Shreenivasa**, Entelechy Global  
[Justifying the Need to Outsource Design Work](#)  
February 16, 2016

**Jeff Davidson and Zev Gross**, Hunter Technology  
[Hunter Technology's Two Newest CID Recipients Discuss Certification](#), April 6, 2015



**Scott Davis**, Broadcom Corp.  
[Broadcom PCB Design: Miniaturization on the Cutting Edge](#)  
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**Amir Davoud**, Innovative Circuits  
[Innovative Circuits Sees Healthy Medical Market](#)  
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**Julie Ellis**, TTM Technologies  
[TTM: Consult Fabricators Early for PCB Designs](#)  
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**Randy Faucette**, Better Boards Inc.  
[The Partnership: Design Engineers and PCB Designers](#)  
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**Gary Ferrari**, Firan Technology Group Corp.  
[IPC Designers Council Viewpoint: Gary Ferrari](#)  
The PCB Design Magazine, Dec. 2015

**Gary Ferrari**, Firan Technology Group Corp.  
[Gary Ferrari Shares His Thoughts on PCB Design and More](#)  
The PCB Design Magazine, July 2015

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**Albert Gaines**, HiGain Design Services

[Designing with Fine Lines and Features](#)

The PCB Design Magazine,  
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**Mark Gallant**, DownStream Technologies

[DownStream Takes on Data Documentation Management](#)

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November 2015

**Stephen Garcia and Brian Paper**,  
Bay Area Circuits

[Good in, Good out: Bay Area Circuits Discusses Data Strategies](#)

The PCB Design Magazine, November 2015



**Brad Griffin**, Cadence Design Systems

[What's New at Cadence?](#)

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**Gary Griffin**, Fast Interconnect

[Fast Interconnect: Engineering Services for the Masses](#)

July 20, 2015



**Steve Hageman**, Analog Home

[The Roles of the Designer and the Design Engineer](#)

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**Rick Hartley**, RHartley Enterprises

[IPC Designers Council Viewpoint: Rick Hartley](#)

The PCB Design Magazine,  
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**Tom Hausherr**, PCB Libraries

[Catching up With Tom Hausherr of PCB Libraries](#)

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January 2016



**James Hofer**, Accurate Circuit Engineering

[Avoid Overbuilding your RF Printed Circuit Board](#)

July 9, 2015



**Nolan Johnson**, Sunstone Circuits

[Sunstone Circuits R&D: 3D Printing Great for Prototyping](#)

The PCB Design Magazine,  
March 2016



**David Ledger-Thomas**,  
Honeywell Aerospace

[Designing with Tighter Tolerances](#)

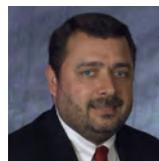
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**Kenneth MacCallum**,  
StarFish Medical

[Medical PCB Design: Not Just Another High-Rel Board](#)

The PCB Design Magazine,  
January 2016



**Manny Marciano**, EMA Design Automation

[EMA: Helping Technologists Manage Disparate Data](#)

The PCB Design Magazine,  
November 2015



**Max Maxfield**, Maxfield High-Tech Consulting, LLC

[Max Maxfield Looks at the Future of Electronics](#)

July 13, 2015



**Scott McCurdy**, Freedom CAD Services

[Trending at Freedom CAD: New Crop of Next-Gen Designers](#)

March 20, 2015



**Anne Marie Mulvihill**, IPC

[IPC Designers Council: Serving PCB Designers for Almost 25 Years](#)

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**Al Neves**, Wild River Technology  
[Wild River: Simplifying SI so Engineers Can Focus on Design](#)  
April 19, 2016

**Mark Thompson**, Prototron Circuits  
[From the CAM Shop: Tight Tolerance Design Tips](#)  
The PCB Design Magazine, June 2016



**Bob Potock**, Zuken USA  
[What's New at Zuken?](#)  
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**Tony Tung**, National Taiwan University  
[Changing the World of PCB Rapid Prototyping](#)  
June 22, 2016



**Greg Roberts**, EMA Design Automation  
[EMA is Bullish on Data Management](#)  
The PCB Design Magazine, March 2016



**Anaya Vardya**, American Standard Circuits  
[American Standard Circuits: Leading the Way in Medical Electronics](#)  
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**Tony Senese and Tomoyuki Abe**, Panasonic  
[Panasonic Meeting Market Needs with Higher-Performance Megtron 7](#)  
March 17, 2015

**Per Viklund and Alex Caravajal**, Mentor Graphics  
[Mentor Graphics Helps Bridge Gap Between PCB and RF](#)  
The PCB Design Magazine, August 2015



**Isam Shakour**, Shax Engineering  
[Shax Engineering: The Biggest Little Board Shop in the Bay Area](#)  
May 6, 2015



**Todd Westerhoff**, SiSoft  
[SiSoft: Optimizing the State of the Art](#)  
The PCB Design Magazine, April 2016



**Michael Steinberger**, SiSoft  
[Steinberger Talks PAM4, the Next Generation of Modulation](#)  
April 13, 2016



**David Wiens**, Mentor Graphics  
[Technology Outlook with Mentor Graphics](#)  
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**Mark Thompson**, Prototron Circuits  
[Mark Thompson: It's All about Communication](#)  
March 13, 2016

**Bob Williams and Tyrone Stephens**, Pulsonix  
[Pulsonix Poised to Take More EDA Market Share](#)  
December 9, 2015



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### [The Newest Flex Shop in the U.S.](#)

I-Connect007 sales team member Angela Alexander and I recently got a tour of Lenthor's new Silicon Valley flex board shop and then sat down with President and CEO Mark Lencioni to discuss the new flex facility, the markets, management, and the future.

### [The 21st Century PCB Factory—Designed to Eliminate Offshore Cost Advantages](#)

More than 15 years have passed since North America and Europe ceased being the center of worldwide PCB fabrication and were supplanted by a Chinese market with low-cost labor, lax environmental requirements, and strong government support

### [Happy's Essential Skills: Design for Manufacturing and Assembly, Part 1 and Part 2](#)

Advances in interconnection technologies have occurred in response to the evolution of component packages, electronic technology and increasing complex functions. Therefore, it comes as no surprise that various forms of printed wiring remains the most popular and cost effective method of interconnections.

### [All About Flex: Imaging Methods for Etch Resist, Part 3: LDI](#)

When LDI technology was first introduced around 20 years ago, throughput was an issue. LDI was often restricted to low volume or prototype runs. Subsequent advances in equipment as well as faster acting photoresist have made it practical for high volume circuit fabrication.

### [Against the Density Wall: Landless Vias Might be the Answer](#)

I saw my first landless via multilayer while visiting NEC in Japan in 1985. You may not know much about landless vias. This has been a well-kept secret for the last 30 years, possibly because it is not permitted on military boards, and therefore, discouraged in all IPC standards.

### [Standard of Excellence: The Future is in Fine lines](#)

The age of much finer lines and spaces is upon us. After years of slowly moving towards this technology our customers are now demanding that all of us provide them with fine lines and spaces. Our new trend in electronics is for denser and denser circuitry on smaller and smaller real estate.

### [Weiner's World](#)

The way that I see the problem relates to over-capacity for fabricators in the consumer segment of devices with flat panel displays—mobile and otherwise—as well as a decline in notebook PCs, TVs and other household and portable electronic devices.

### [Happy's Essential Skills: Understanding the Concept of Managing Management Time](#)

You can get the most value out of monkey management and one-minute management by using these principles together. Who knows? With these techniques, maybe you'll have a chance to take care of your own work instead of everyone else's!

### [Catching up with Sunrise Electronics' Ashok and Jigar Patel](#)

I had been hearing about Sunrise Electronics for many years, so when Ashok asked me to come and see them for myself, I jumped at the chance. It was one of the most amazing plant tours that I've been on in a long time. I wanted to know more, so we sat down and had a chat.

### [EPTE Newsletter: Transparent Circuits Gaining in Popularity](#)

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# How to Handle the Dreaded Danglers, Part 1

by Barry Olney

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Dangling via stubs can distort signals passing through your interconnect, and decrease the usable bandwidth of the signal. A via stub acts as a transmission line antenna, and has a resonant frequency determined by the quarter wavelength of the structure. At this frequency, the transmitted signal is greatly attenuated, by up to 3dB. For low-frequency signals, this is not much of an issue because these signals are significantly lower than the resonant frequency of the via stub.

However, for higher-frequency signals (>1GHz), which are becoming more common as performance specifications are increased, this issue becomes a problem because the signals are transmitted at frequencies near or at the resonant frequency of the via stub. Harmonic components that are odd multiples of the fundamental frequency can also be highly attenuated.

The conventional solution to this problem is to back-drill (or control-depth drill) the vias to bore out the via stub barrels, so that the via stubs are reduced in length, if not completely removed (Figure 1).

If the via is short, compared to the signal rise time, then it acts mostly as excess shunt capacitance. The entire length of the via contributes to the capacitance, while only the section where the signal current actually flows makes up the inductance. However, a long via stub can develop resonance that exacerbates the effects of its capacitance. I should point out that it is fine to have a plated through-hole (PTH) via, providing the signal goes in at one end and out at the other, using the entire length of the barrel.

When a via's stub length is equal to a quarter wavelength of the signal frequency, the signal travels from the trace to the end of the stub and

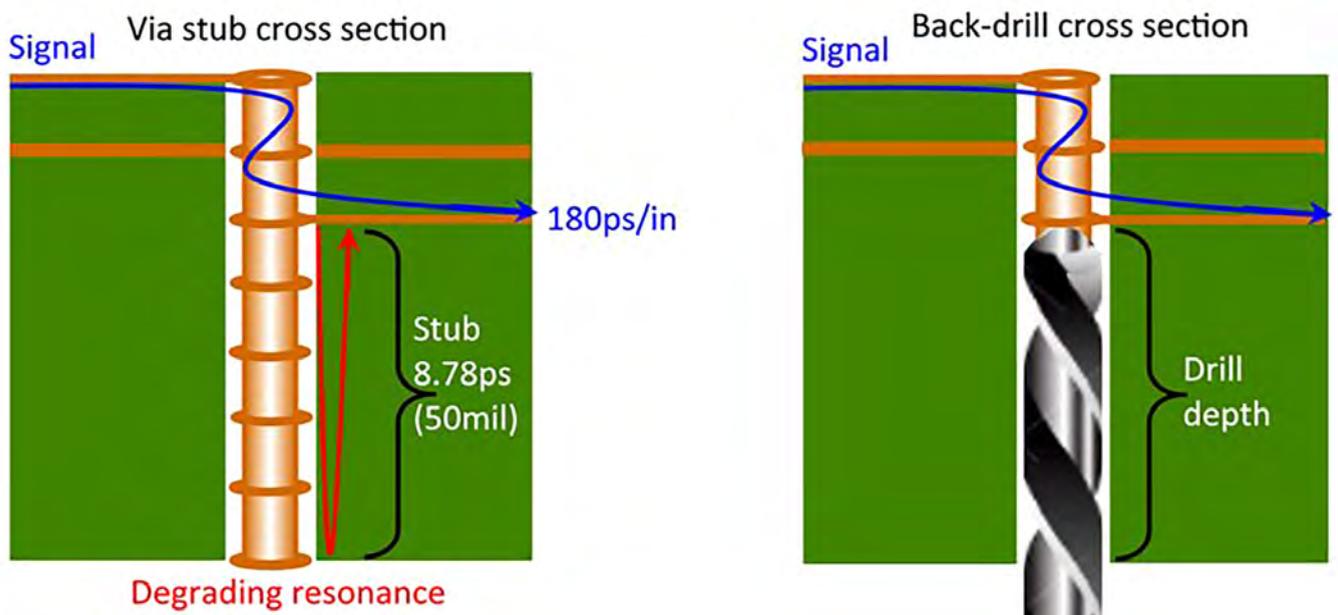


Figure 1: The unterminated via stub (left) and a back-drilled via stub (right).

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then bounces off the open circuit end-point and back to the trace for a total distance of a half wavelength. This half wavelength travel has the effect of shifting the phase of the signal by 180 degrees, creating resonance in the via stub. The phase-shifted, reflected signal has a maximum value at a time when the signal has a minimum value, and vice-versa.

The Nyquist frequency of a discrete signal is defined as a half of the sampling rate of the signal and will have a strong frequency component at this frequency. In addition, the signal can have strong power spectrum harmonic components at frequencies greater than the Nyquist frequency typically up to the 5<sup>th</sup> harmonic. The resonant frequency of the via stub is inversely proportional to the dielectric constant of the material, surrounding the via, with a wavelength of four times the length of the unused portion of the via. This relationship is given by the following equations:

$$T_{via} = l \frac{\sqrt{Er}}{c}$$

$$F_{res} = \frac{1}{4.l.T_{via}}$$

Where  $T_{via}$  is the time for the signal to propagate in a stub (~180ps/in for FR4),  $l$  is the length of the via stub,  $Er$  is the dielectric constant,  $c$  is the speed-of-light and  $F_{res}$  is the resonant frequency of the via stub.

When the resonant frequency is approximately equal to the Nyquist frequency, one or more frequency components, of a signal transmitted through the via, can be strongly attenuated which causes the impedance of the via drop. And although, it seems high enough to be outside consideration for most designs, the affects actually start to come into play above

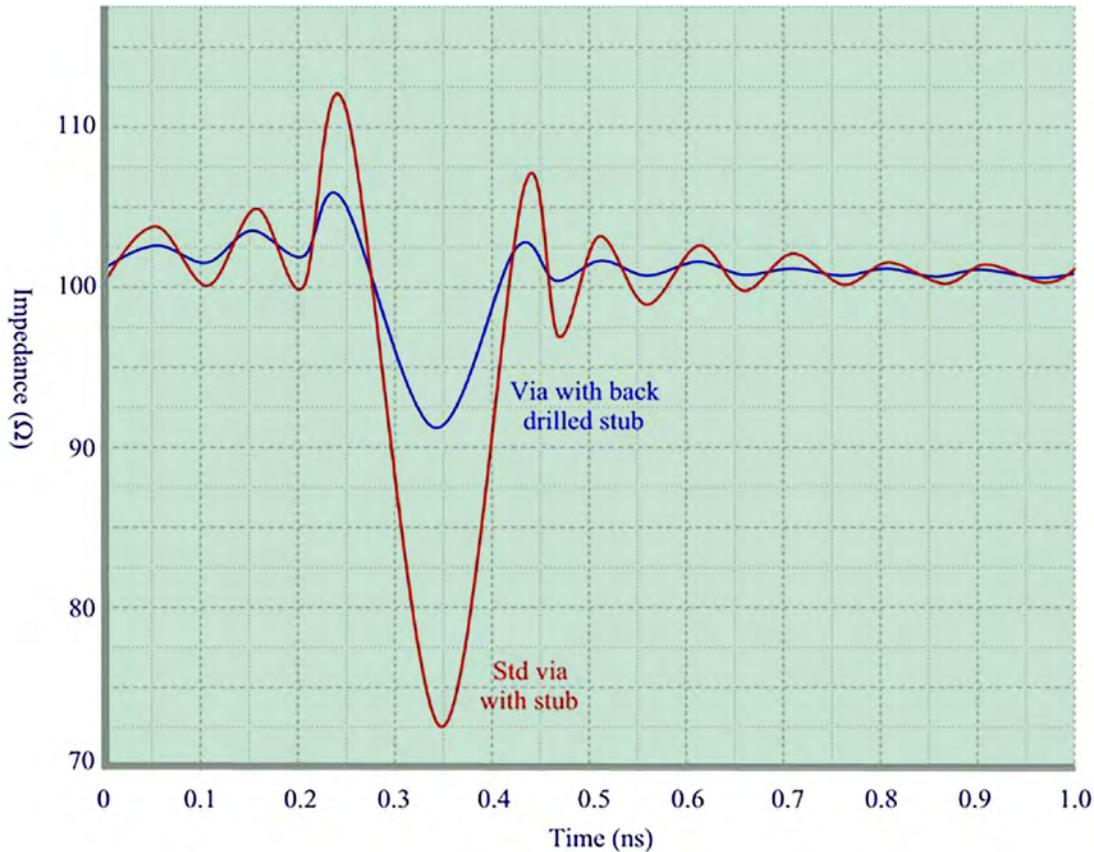


Figure 2: Differential 100Ω via with stub (red) vs. via with back-drilled stub (blue).



1GHz and become an issue at around 4–5GHz in most cases. This attenuation limits bandwidth. Figure 2, illustrates the impedance of a standard PTH via compared to a back-drilled via stub as displayed on a Time Domain Reflectometer (TDR). In the case of a high-speed backplane, the effects are even more dramatic as the Nyquist frequency can be in the order of 5GHz, for a 250-mil substrate, and the impact can be evident at 1GHz.

As mentioned, vias can appear as capacitive and/or inductive discontinuities. These parasitics contribute to the degradation of the signal as it passes through the via. One approach is to break each segment of the via into small discrete inductance and capacitance elements corresponding to each section of the barrel interacting with the planes and with each other. With this method, it is difficult to achieve an accurate result because the fields are inherently fringe field dominated. Also, matching discrete elements to overlapping fringe fields is difficult.

Figure 3 shows a simplified lumped LC  $\pi$  model (without non-function pads) to illustrate via capacitance and inductance affects. Although this model is only applicable if the

delay of the via is less than  $1/10^{\text{th}}$  of the signal rise time, it is still useful for understanding the capacitance and inductance affects. The attenuated phase-shifted signal (red) shows the degradation effects of the via stub, whereas the back-drilled via (blue) has an undistorted, broader signal.

Channel discontinuities can emanate from several sources and each of these must be carefully considered. One commonly overlooked cause is the signal via. Vias can add jitter and reduce eye openings that can cause data to be misinterpreted by the receiver. Length is the primary factor that influences the inductance of the via, which depends on the design complexity, the number of layers, and hence the overall PCB thickness. The length of the PTH via is the same as the overall thickness of the PCB. A typical high-speed PCB design ranges from 1.0 mm to 1.8 mm. For more complex designs, backplanes and military rugged applications, the PCB thickness can go above 3 mm. Given the increasing complexity of high-speed digital design, PCB thickness is expected to increase due to higher layer count. In order to mitigate the effects of the via stub, we need to:

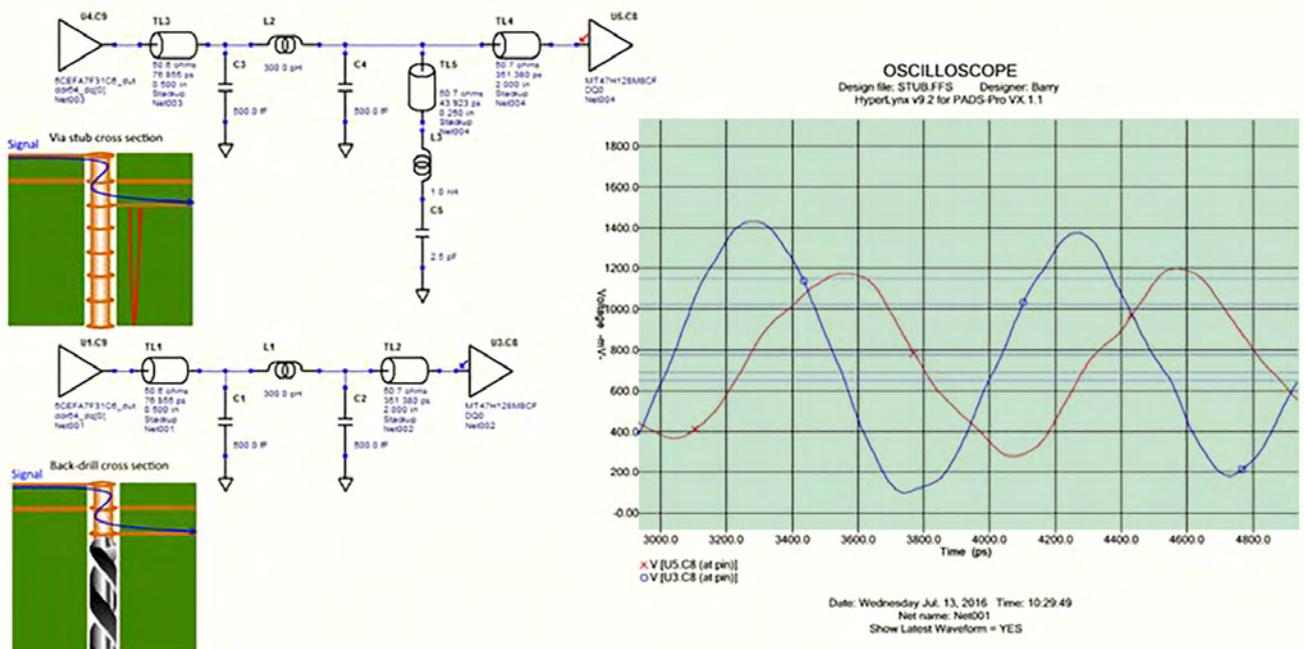


Figure 3: Simplified LC  $\pi$  model of via with and without the stub simulated in HyperLynx.

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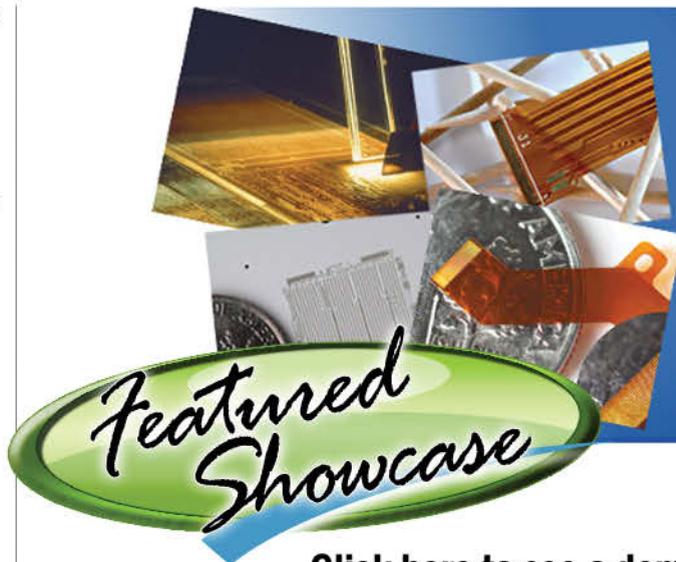
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Minimize the via inductance by

- Eliminating or reducing stubs
- Reducing the via barrel length

Minimize the via capacitance by

- Reducing the pad size
- Removing non-functional pads
- Increasing the antipad size

There have been a number of solutions put forward to alleviate this issue including:

- Back-drilling the stub
- Using blind vias
- Removing non-functional pads
- Increasing the antipad diameter
- Terminating the stub
- Lowering the surrounding dielectric constant
- Plating the via barrel with a lossy material

Next month, in Part 2 of this series, I will look into the possible solutions to alleviate this issue, including tuning methods to make the vias more transparent to faster edge rates are evaluated. Via trade-offs are also examined because of manufacturability concerns of higher oven temperatures associated with the recent switch to restriction of hazardous substances (RoHS) processes. Finally, general guidelines and recommendations will be made to show how to design an optimized the vias for better high edge-rate signal transmission will be discussed.

### Points to Remember

- Dangling via stubs distort signals passing through an interconnect and also decrease the usable bandwidth of the signal.

- A via stub acts as a transmission line antenna, and has a resonant frequency determined by the quarter wavelength of the structure.

- It is fine to have a plated through-hole (PTH) via providing the signal goes in at one end and out at the other using the entire length of the barrel.

- The Nyquist frequency of a discrete signal is defined as one-half of the sampling rate of the signal. The impedance of the via stub drops at this frequency.

- The resonant frequency of the via stub is inversely proportional to the dielectric constant of the material surrounding the via with a wavelength of four times the length of the unused portion of the via. **PCBDESIGN**

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2. [Dell products](#), by Stuart Allen Berke.
3. [IBM Corporation](#), by Bhyrav Mutnury.
4. Altera, Via Optimization Techniques for High-speed Channel Designs.
5. [High-Speed Signal Propagation — Advanced Black Magic](#), by Howard Johnson, Martin Graham



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD) Australia. The company is a PCB design service bureau that specializes in board-level simulation. ICD has developed the ICD Stackup Planner and ICD PDN Planner software, which is available [here](#).

## Chemical Sensing at Telecom Wavelengths

Lasers operating at the wavelength of 1,550 nanometers power high-speed fiber-optic Internet communications. MIT Microphotonics Center Principal Research Scientist Anuradha Agarwal is developing chemical sensors based on this wavelength using a new materials system built of silicon carbide on silicon dioxide on silicon.

Ashley Del Valle Morales, a junior at the Univer-

sity of Puerto Rico at Mayaguez, will test the silicon carbide-based sensor before and after it is exposed to gamma rays.

Del Valle says, "I know it's really important to select a project you like and you're interested in. I also liked the enthusiasm and the interest that the grad students and the principal research scientist showed."



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# Your Traces Have Hot Spots!

by Douglas G. Brooks, PhD

Your traces have hot spots. At least, those that carry a moderate current do. Surprised? Well, I was a little surprised, too, when I looked at this a little more closely.

One chapter in my recent book<sup>[1]</sup> focuses on fusing current. It contains the image (Figure 1), captured on video, which shows a 20 mil wide trace that had been heated for about 15 minutes, just at the moment of fusing. There are several interesting things in this image, especially how the smoke is blown out from under the trace at certain points with considerable pressure. But note that the trace fuses at a point, not everywhere along the trace. It is clear from observation that the trace is much hotter at some points than at others.

Figure 2 appeared in a separate article published in 2010<sup>[2]</sup>. (It has been enhanced after

some collaboration with the author of that article.) The image shows a trace being heated to the melting point. At this stage, the hottest portions of the trace are over 600°C, but other areas remain in the 200°C temperature range.

The reasons for the temperature variation at high temperatures is not too hard to understand. There may be minor contamination under the trace or in the copper that accounts for it. Certainly, at higher temperatures (say above about 300°C) the board may begin to delaminate, severely disrupting its cooling characteristics. There may be small variations in trace width or thickness that help account for the delam, and these effects would be randomly distributed along the length of the trace.

But in a variety of lower-temperature studies<sup>[1]</sup>, I personally took trace temperature mea-



Figure 1: A 20 mil wide trace at the moment of fusing.



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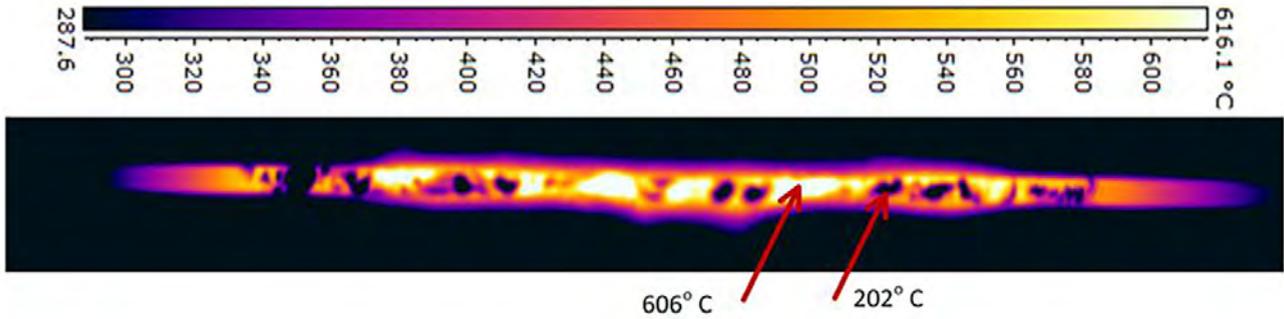


Figure 2: The trace temperature varies considerably along the trace length.

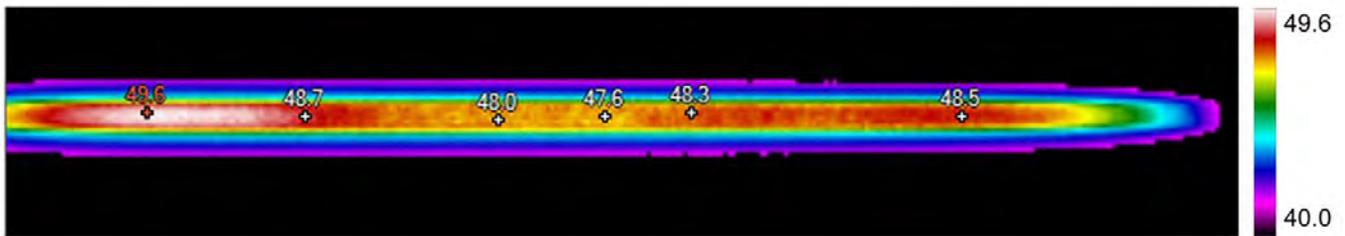


Figure 3: Temperature variation along a 100 mil wide trace.

measurements using a small thermocouple. I noticed that if I moved the thermocouple slightly, I would get a different temperature reading. Not by much, maybe 1.0° or 1.5°C. This is more than the resolution of the thermocouple, but not enough for me to be satisfied that the differences were real. So I began to wonder if these variations in temperature appeared at lower trace temperatures, say in the 40°C. range.

I had a variety of test boards available with different trace widths and thicknesses<sup>[3]</sup>, but I needed a thermal imager to look at them. A local firefighter loaned me a Fluke model TI32 imager which was invaluable for this investigation (see acknowledgements).

Figure 3 is one of the images I obtained from those sample boards. It is of a 100 mil wide, 0.5 oz. trace heated to just under 50°C. The temperature range of the image has been compressed from about 40°C to 49.6°C. in order to focus in on the minor temperature variations. It is evident that even at this low a temperature, there are temperature variations along the trace. And

the hottest point along the trace is not at the midpoint of the trace. In this instance, it is well to the left of that point.

But perhaps even more surprising is the temperature variations across the width of the trace. This was apparent in every observed trace<sup>[4]</sup>. The hottest part of the trace is along the centerline, but the trace cools as we move closer to the edge. These two effects are what I saw when I moved the thermocouple.

One would expect that the thermal conductivity of the copper is so good that there would be no thermal gradients possible along a trace (except, perhaps, as one approaches the pads at the ends). We would especially expect that to be the case for such a short distance as the width. But there is a theoretical explanation for the trace being cooler along the edge (Figure 4).

The trace cools by heat conducting away from the trace through the dielectric<sup>[5]</sup>. The dielectric conducts heat better in the horizontal (in-plane) direction than it does in the vertical (through-plane) direction. This cooling path is

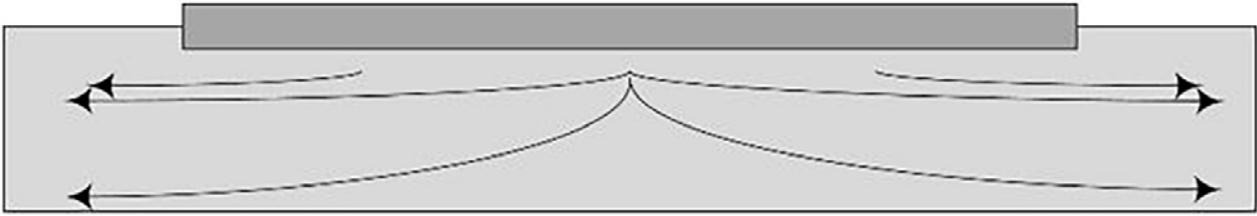


Figure 4: The cooling path for a trace is longer from the center of the trace than it is from the edge of the trace.

shorter for points along the edge of the trace than it is for the center of the trace. Therefore, the edge cools more effectively, and the edge is therefore cooler than the center.

Trace heating and cooling dynamics are much more complicated and subtle than perhaps we had previously understood.

### Acknowledgement

This (and several other investigations I've made) would not have been possible without the generous cooperation of Prototron Circuits, who provided a number of test boards for evaluation. I am also indebted to Scott Dau, a Seattle firefighter and part-time fire investigation instructor, who loaned me a thermal imager for capturing a variety of thermal images, many of which are provided in Chapter 12 of my latest book. Norocel Codreanu of the University of Bucharest's Center for Technological Electronics and Interconnection Techniques also provided assistance in looking at this relationship. And I want to especially thank Johannes Adam, of Leimen, Germany, for his collaborative support over the last 18 months. **PCBDESIGN**

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2. "New Methods of Testing PCB Traces Capacity and Fusing," Norocel Codreanu, Radu Bunea, Paul Svasta, Politehnica University of Bucharest, Center for Technological Electronics and Interconnection Techniques, UPB-CETTI,

internal research project and report of UPB-CETTI/Winter-2010. For more information, [click here](#).

3. Provided by Prototron Circuits for other investigations reported in reference 1.

4. The thermal images of all the traces I had available are included in reference 1, Chapter 12 and Appendix A9.

5. See reference 1, Chapter 4.



For the last 20 years, Douglas Brooks has owned a small engineering service firm and written numerous technical articles on printed circuit board design and signal integrity issues, and he has published two books on these topics. He has given seminars several times a year all over the US, as well as Russia, China, Taiwan, Japan, and Canada. His primary focus is on making complex technical issues easily understood by those without advanced degrees. His latest book, "PCB Trace and Via Currents and Temperatures: The Complete Analysis," was released earlier in 2016.



## Mike Creeden: Care and Training of Your Designers

The I-Connect007 team recently visited San Diego PCB Inc. and received a warm welcome from CEO Mike Creeden and his youthful-looking (relatively speaking) team of designers. Creeden spoke with Barry Matties and Judy Warner about what it takes to run a successful design service center, how to properly care for the PCB designers of today and tomorrow, and why IPC's design training is paramount when training a new designer.

**Barry Matties:** *Mike, tell us a little about yourself and San Diego PCB.*

**Mike Creeden:** San Diego PCB was incorporated in June of 2003, so we are in our 13th year of existence, and as a professional, I am in my 40th year of doing this. That makes me sound old, but I don't feel old.

**Matties:** *It does sound old. But you're only as old as you feel, I guess.*

**Creeden:** Well, here's why I don't feel old, it's because I love what I do.

**Matties:** *I guess it depends on when you started, because if you started when you were 40...*

**Creeden:** Oh, I started when I was two years old (laughs). No, I've had my 60th birthday, so...

**Matties:** *Ah, so you started in your twenties?*

**Creeden:** I started in my twenties, when I got out of the military. I was in the military in a short-range tactical nuclear missile unit. It was known as one of the deadliest and stupidest weapons ever made. People would say, "Not a good day to shoot this thing," and they'd check the wind. But I had a technical propensity back in the day, and so when I came out of the military, shortly thereafter, I started in this profession and there's been no looking back. I've had the privilege to work for a lot of different companies, from big-name companies to a lot of the different CAD companies. So I had the opportunity to learn a little bit about the business, the software that the business runs on, for PADS, now Mentor, and Cadence and Zuken.

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What I found out is that, regardless of how good I did as a designer, I didn't always control my destiny, so to speak. I concluded that rather than just going to the companies, it made more sense for me to create a good CAD environment and let the companies come to me, and that's worked well. It works well because I take care of the designers, and that shows, and the customers like that. It's been the staple that gives our business a corporate signature and a corporate culture.

**Matties:** *Just for context, tell us a little bit about San Diego PCB, what the mission is, and what you guys do.*

**Creeden:** We have a mission statement, because that's what they say you're supposed to do when you have a corporation: have a corporate culture based on a mission statement. The mission statement is, essentially, to have revision 1

.....

“There's nothing magical about it; it's just good work and determination to try to do that.”

.....

work, and I want quality, and I want to do it the best I can on time. Those are the three things that most people say, “You can have two of the three.” I'm sure you've heard that said. To the best degree we can, we're trying to do all three. There's nothing magical about it; it's just good work and determination to try to do that.

**Matties:** *First and foremost, are you a design bureau?*

**Creeden:** We're an engineering PCB layout design service. It would make a long acronym, but PCB CAD layout. Essentially, we're a “virtual CAD layout department,” because whether or not you're one cube away or you're a block down

the road, or on the other side of the country, you're one Ethernet port away. So with Internet computing skills, online meetings, and shared desktops, we've truly been able to bill ourselves and service customers as a virtual CAD layout department. We're doing primarily PCB design layout services. We offer schematic drafting and design services as a, kind of like hands three and four, if you would. We're not billing ourselves as a full engineering service; we support engineering departments.

**Matties:** *When we look at the engineering process, one of the things that we hear most often is that the systems designers don't bring in the circuit designers until it's time to throw the thing over the fence, and then you have these constraints to work in, or parameters to work within. But if they had brought you in earlier, life would be better for the end-product and everybody up and down the supply chain. What's your view of that, and how does it work here?*

**Creeden:** There's no one answer for that.

**Matties:** *Is that typically the case, though?*

**Creeden:** It is for a segment of the industry. I'm not being vague here; it's just that the industry truly is compartmentalized in what I would say are three categories. First are the enterprise companies, which basically have their initial products, and then they have a whole group, or many different groups, within these big companies that are doing the skunkworks projects—the test, the development, the R&D, and a lot of that work is farmed out. Often, it's very schedule-driven, and so it has tight time constraints.

Then there are a lot of mid-level companies that have chosen not to have their own CAD group, and then there are the startups that, again, do not have a CAD department.

**Matties:** *Are groups two and three really the ones that come to you most often?*

**Creeden:** No, we're doing work for Intel, HP, Qualcomm, Tesla, 3M—those are name-dropping companies, so here I am name-dropping—but to me, every customer has to have the same

value. I want to service them all equally. I'm not just saying that; I want to aspire to that.

**Matties:** *When do they get you involved in the engineering process? I would think Tiers 2 and 3 would bring you in pretty early, where Tier 1 may not.*

**Creeden:** The answer is still, in actuality, it's all over the map. But the point you were driving at, "Is it better when CAD is brought in earlier in the design phase?" and the answer is absolutely yes. The smart answer is that concurrent engineering is always the best solution. A stitch in time saves nine.

**Matties:** *We all agree with that, yet the reason for the question is that so few seem to do it. I hear what you're saying, and you're not putting yourself in any box, but the reality is, so few actually do it.*

**Creeden:** I'm going to give a little tongue-in-cheek answer to that. I'm going to do my best Rodney Dangerfield impression and say, "I get no respect." Oftentimes, PCB CAD layout is not respected as a discipline. It is an engineering profession, but you typically don't earn a degree in it. Most people who earn a degree go into hardware engineering or software, so if you've earned an EE, a BSEE, that's what you're doing. More and more, EEs are doing layout, but what they're finding is they only pass the layout cycle three times a year. So they do layout three times a year, because they understand engineering, but does that make them proficient in PCB layout? Most of them can comprehend it, but they don't have the packaging skillset.

If you'll look around you, there are some puzzles in this room, because a good PCB designer knows how to solve a puzzle and is intrigued. It just sparks the serotonin level in a designer, and he's thinking, "I want to solve that." Whereas an engineer tends to be a little bit more on the logical side. "Let me find an algorithm or a macro to just repeat this. I see that as repetitive, and I don't want to do it." No dis-



respect to my fellow PCB designers, but it is a tier down on the engineering food chain. A lot of engineers don't want to do it because of that, and then because they don't do it that often, when they do it, if they're not successful, and now they've looked bad: "You're supposed to know this, because you're above it, yet you weren't successful."

The engineer says, "Well, I'm too busy, so just farm it out to those guys." A lot of times, that's the way it plays out. Many engineers are very good at doing it, and those that have pursued their education, perhaps through an IPC CID certification, have learned some of the manufacturing issues that are involved in that.

To rephrase that, to PCB designers, there are several different caveats, and people don't look at all of them. Do you understand the electronics of it, is one part of it? The engineers do. Do you understand the CAD tool, and how to be proficient using the CAD tool? That's another part. Do you have a good puzzle-solving, spatial, a symmetrical knack to your person? Are you an orderly person? Is your desk orderly, do you see things with symmetry? Designers are good at that. Lastly, do you understand the manufacturing capabilities that are out there? What does it take to fabricate a good board? What does it take to assemble a board? What does it take to respect IPC specifications and build a high-yield product? The answer to that question is, those things are often assumed and disregarded.

**Matties:** *The other point that we hear is that so many designers don't understand the manufacturing process; they've never manufactured a board. How can they design a great board with manufacturing in mind without that experience?*

**Creeden:** Good question, and to the degree that a designer doesn't understand the manufacturing process, I say "Step away from the CAD tool"! I put to you that a designer is probably closer to the manufacturing, oftentimes, than a lot of EEs.

**Matties:** *Could be, but this is one of the things that we hear repeatedly.*

**Creeden:** You're going to hear that claim against anyone who uses a CAD tool to layout a board, regardless if they're a designer or an engineer.

**Matties:** *We just did an interview with Mentor, and they're coming out with their new tools, and it seems like they're bringing a lot more intelligence into the tools for the designers. I don't know what all the finer features are, but seems like we're seeing more of that embedded in the tools to assist the designers.*

**Creeden:** I've occasionally gotten a raised eyebrow from some of the software manufacturers, because there are a lot of verification tools to find the errors that are out there. I would put to you, how about you do it correct by construc-

.....  
**“ I would put to you, how about you do it correct by construction and not make the errors, and minimize the need for it? ”**

tion and not make the errors, and minimize the need for it? Thus I get a raised eyebrow at that, because they want to sell software, and God bless them, they need to sell software, but my point is that a good designer who's pursued their IPC certification does understand the manufacturing criteria. If you haven't pursued that, you should step away from the CAD tool, because there are a lot of people who are just connecting the dots, and whether they're a EE doing that or a designer doing it, you still have connected dots but you've not routed the circuit.

**Matties:** *Now, back to another point that you're raising, and one that we've heard, is there are other paths that young people want to take besides designing circuit boards. Designers are becoming an*

*aging population, and there's no funnel of young designers coming in. What can you say to attract bright young people to a career in PCB design?*

**Creeden:** I had the privilege at one point to write an article concerning that subject. As a demographic, a lot of baby boomers were brought into it, and so the average age of the PCB designer is the mid-50s. There is a lot of new blood being brought in, if you went through my staff right here, more than half of them are under 40. We are bringing them in, but what the industry has neglected for a decade or more is the concept of bringing somebody in and giving them the on-the-job training. We've gone through several economic downturns, and so what they do is they cut their department, and they don't develop people and bring them in.

**Matties:** *Which could be good news for your business.*

**Creeden:** Which is one of the reasons I created this business, because they are coming to SD-PCB, and I consider myself to be grateful!

**Matties:** *You've adopted that philosophy of training and mentoring.*

**Creeden:** Absolutely!

**Matties:** *Yes, I saw the youth here.*

**Creeden:** I have several designers who have 10 to 15 years in the business, and they're some of the best I've ever seen, and it's because we do operate as a team, so no one designer's ever on their own. Everyone is always mentoring or being mentored, and that's kind of a corporate philosophy that we hold too.

**Matties:** *You've given us a great tour of your facility here. It's a nice facility, and we'll share some of the photos. One of the things that you noted was the need to bring people out of their tunnel vision and act as a team, working together and communicating, because it is such a myopic function.*

**Creeden:** It is. We want a consistency, if more than one designer was to work on a project, and



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in today's ever-competitive world, schedules are always being compressed. So, therefore, designers need to put in more than eight- or a ten-hour shifts all the time. At some point, if you truly ran it around the clock, you're going to get some diminished hours. To be honest with you, we've seen that around 20 hours is what's productive. I don't care how you work it, or where you work it—you're going to get about 20 hours. I've seen people actually send designs all over the globe, but you're not getting eight hours of fresh blood from three people. You're getting two hours of lost communication, and it's watered down.

When you put two people to work next to each other, understand how they work, have a similar methodology, and a slight overlap in their schedules, the communication is stronger, and the overall productivity tends to be better. I value my designers' personal lives, so I'm eager that they do what they need to do. There's an old expression, "Would you die on that hill?" Every engineer wants you to die on the hill of completing their circuit, and I don't want to sacrifice any of my designers, because then they won't be there for the next time that engineer comes back. I value them, and the way I protect them is giving them a backup, and they train one another, and they work together.

**Matties:** *What do you think the greatest challenge is for a design service center today?*

**Creeden:** For a design service center today, the biggest challenge for me is taking care of the designers. If I do that, OK. And I take care of my customers, and I will develop them, and that development and that teamwork shows up in my customers' satisfaction. Why are they satisfied? They want a quality board, they want it on time, they want it within budget, and the simple rule is, an engineer wants to go back to the last place they got a good board designed,



so that creates the repeat business. But taking care of the designers, in my opinion, is our biggest challenge.

**Matties:** *How do you do that? Is it the environment, the tools? I understand it's a combination of all these factors...*

**Creeden:** It truly is, and it's esteeming them. The sentence that we use

within our corporate culture is, "You'll either view the designer as a liability or an asset," and in many corporations, they're viewed as a liability. "What can I get out of them?" Whereas, I think, "What can I give them?" I want them to have the best software, the best hardware, a good environment, and be non-competitive with their fellow workers. Why should they be competing against one another if they're on the same team? That's a different philosophy than what's being done elsewhere.

**Matties:** *It's interesting. I've talked to Managing Editor Andy Shaughnessy about the way everyone is always talking about DFM and all of the other "design fors." I said, "Andy, shouldn't we be talking about design for profitability, of DFP?" Because profit starts right here with the design, and if you design it right, you help increase the revenue or the value of the product, which increases the profit.*

**Creeden:** Along that line, I hope designers have the opportunity to take the DFX curriculum that IPC offers. I'm giving a little shameless plug for them because it's very well done. When you say "DFX," most people think you're saying "design for X," X being whatever, and I challenged IPC, because it's much more than "design for." It's "development for" assembly, fabrication, test, environment, all those different things. It's really a development thing; it's much more than design. But when you teach the Certified Interconnect Designer (CID) program, one of the main principles that we try to communicate at the very beginning is that quality will produce

a better yield, and when the yields go up, the price goes down. Conversely, when the yields go down, the cost is going up. People need to design for end usage. Is this going to be a one-time board? Build it with the highest quality, and you don't need to save money, because it's non-reoccurring. If it's a product, get your cost down. Design it for some monetary reasons, and design for the dollar sign.

**Matties:** *And with the attributes of reliability and still meets the functional requirement.*

**Creeden:** Right, but you need to know what the end need is, and what the end customers need; is it a Class 2 board, or a Class 3? Well, who designs Class 2 and Class 3? You ask that question, and most people don't know the answer. The answer is the end-customer. If it's NASA, they want a Class 3 board, because it's going to go in space and I cannot afford anything going wrong. If it's a medical device, it's life-critical. You're in a cockpit, you're flying in an airplane. Do you want the instrumentation in the cockpit to be Class 2 or Class 3? I'm going to go with Class 3.

**Matties:** *Depends on who I'm flying with.*

**Creeden:** Well, you were on the plane.

**Matties:** *That's what D.B. Cooper said, right? "I've got the parachute!"*

**Creeden:** And he lives in San Diego, I learned.

**Matties:** *Yeah, they just closed the case, I understand.*

**Judy Warner:** *What kind of focus does IPC's education for designers give on the manufacturing side? Is it part of the curriculum?*

**Creeden:** Absolutely. In the basics class, they teach you everything from the materials, the property of the material, through construction, the material, and how it affects the electromagnetic signature of traces. So you actually learn about the electromagnetic field by understanding the material, and they teach you about the

process. When I speak, I ask, "What are the tolerances of your CAD data?" Everyone starts thinking, and the answer is that there is no tolerance.

**Warner:** *I was going to say, it's zero.*

**Creeden:** It's true position data. Now, you're not going to build something that's exact. Why? Because there are manufacturing process allowances based on their process, their equipment, and the material. Those things are the variables that designers need to learn, and that the CID basics gives them from the ground up, and then the advanced module goes more into the electromagnetic and some HDI. It's very much taught in that curriculum.

**Matties:** *It's been interesting talking to you. Is there anything that we haven't discussed that we should share with people?*

**Creeden:** I appreciate the effort that you all put in, because *The PCB Design Magazine* provides an avenue of networking, communication, and education. I value education. I've committed much of my career to working with IPC, and working with Gary Ferrari, rewriting the CID and the CID+ manuals. I don't get paid for that. I do it because I value the education. You asked me earlier about where the next generation of designers will come from, because colleges are not producing them. I'd like to point out that just because you have a BSEE, it does not mean that you know how to design a PCB. So, whether you have a degree or don't have a degree, you're no more advantaged to designing a PCB. It's the education that IPC brings, and the education that you guys bring. You guys are constantly searching for what is current, and what is valuable in our industry. I'm grateful that you came by here today so we could share some of insights about what's going on in the industry.

**Matties:** *Thank you for those kind words.*

**Creeden:** My pleasure.

**Matties:** *We're driven to do this, for sure. Mike, thank you so much. PCBDESIGN*

# Conformal Coatings: Beware the Boards that ‘Bare’ All!

by Phil Kinner

ELECTROLUBE CONFORMAL COATINGS DIVISION

This month, I’m going to depart from my usual format of providing five essential facts about conformal coatings. Instead, I’m going to provide an account of a customer’s problem—no company names mentioned, of course—that brought into question the adhesion performance of a coating that they had been using successfully for some time.

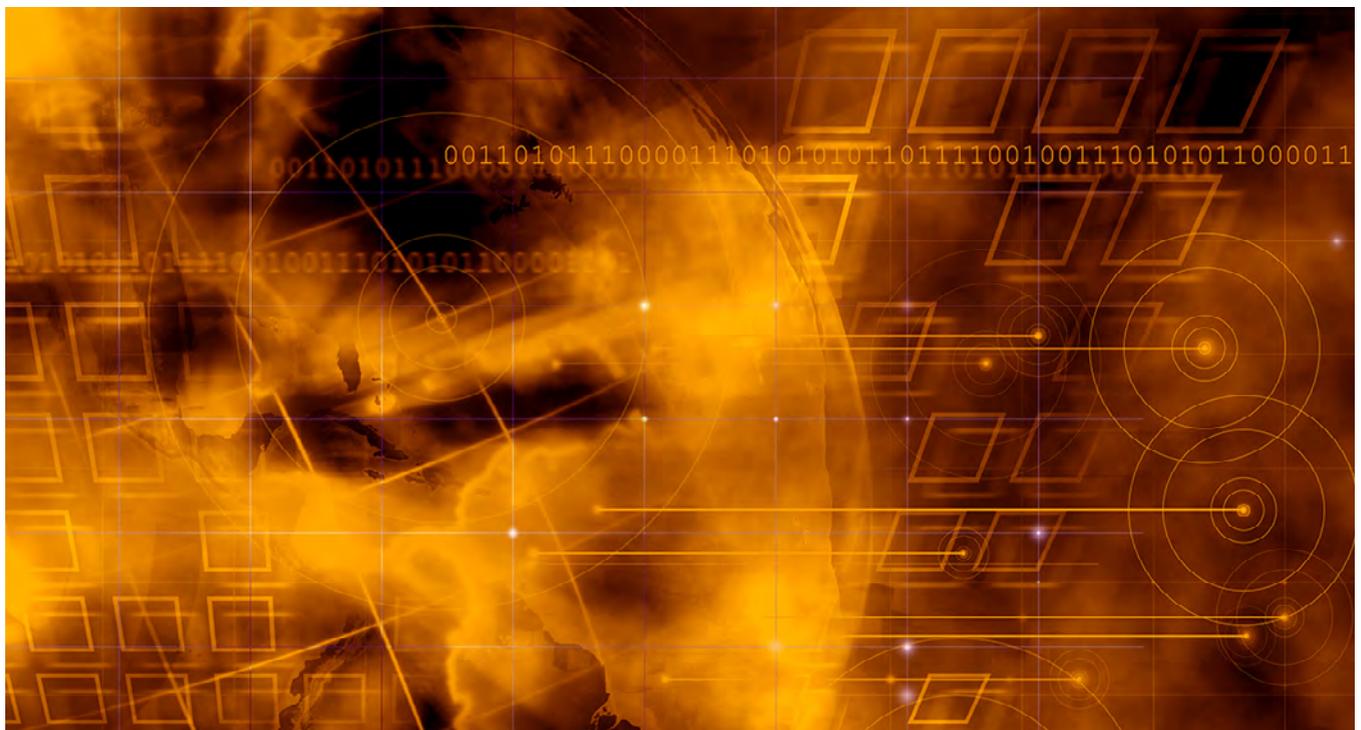
This problem, and its eventual solution, illustrates rather well how good record-keeping, batch traceability, and the auditing of suppliers for quality control compliance can go a long way to help resolve manufacturing issues.

Always up for a challenge, and not wanting to ignore any production-related issue that appeared to cast a shadow over the performance of our products, we donned our detective hats and, with spyglasses at the ready, set about to discover the causes of this particularly challeng-

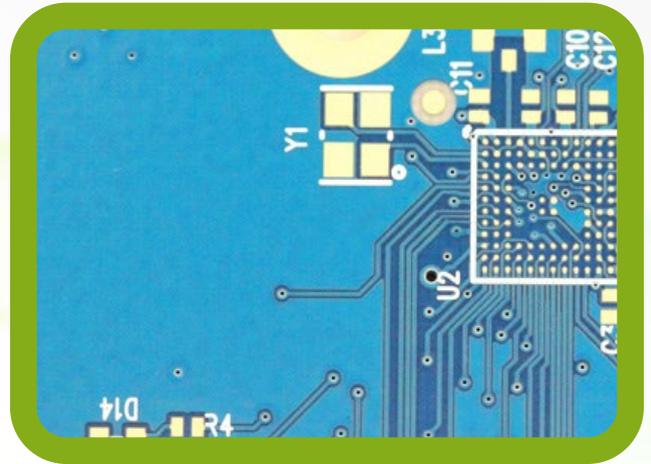
ing delamination problem. But first, let’s have a little bit of background.

Our customer—a multinational firm with sites around the world—contacted us about a coating they had been using without any problems for quite some time, but for some bizarre reason was “no longer sticking” to their boards. They reported that a newly delivered batch of this conformal coating, when applied, could be peeled from the solder mask areas in a single sheet. Our preliminary queries revealed that there had been no changes made to the coating process itself. So, was the coating at fault, or was there something else we were missing?

Delving a little deeper, we discovered that our customer was using this batch of coating material at several of its sites, both within the same country as the problem site, as well as sites located in other countries. It turned out these



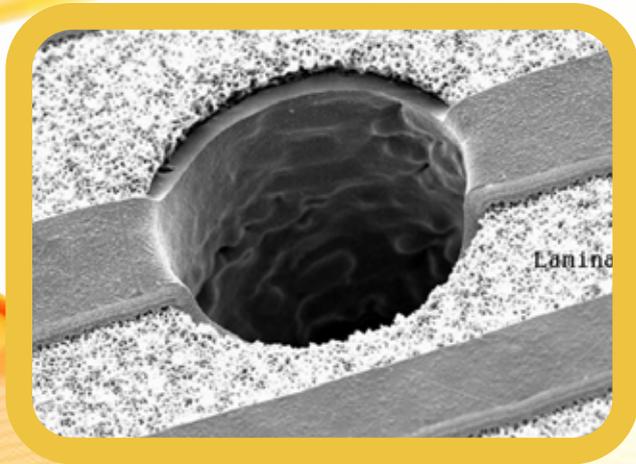
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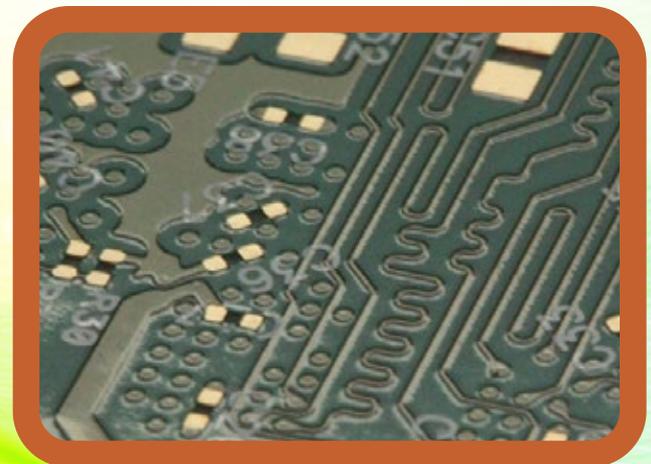


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other sites had no issues to report regarding the coating, and they confirmed that they were experiencing neither the delamination problems we were investigating, nor indeed any problems related to a lack of adhesion. It was time to check the records.

Following a search through their database, the customer discovered they had coated four different styles of boards using the same batch of conformal coating material. Significantly, however, all of the adhesion issues were confined to a single board style. Moreover, these adhesion issues were first reported and recorded at about the same time.

On checking the serial numbers of the coated boards, it became apparent that the adhesion issues all began on a batch of bare boards that had been obtained from a new vendor as part of a cost-cutting measure. Samples of these incoming bare boards were subsequently analysed and found to have a surface energy of 26 dyne/cm (i.e., much, much less than the 40 dyne/cm level recommended for good adhesion).

Our customer then decided that perhaps it was high time to audit the new board supplier. During this process, they found many corners had been cut to save time and money, but two things, in particular, stood out. Firstly, the board shop was performing multiple passes through a UV oven to “cure” the solder resist, instead of the single recommended UV pass and a secondary thermal bake. Secondly, the auditor noted a “shiny film” floating on the surface of the rinse bath during the final rinse process.

Indeed, each UV exposure was found to reduce the bare board surface energy by two dyne/cm, while the final rinse was found to contain significant amounts of oils and lubricants used during the manufacturing process. By eliminating the additional UV processes, implementing the recommended thermal cure and ensuring a clean final rinse process through careful monitoring, the supplier was able to produce boards with a requisite surface energy greater than 46 dyne/cm—enough to ensure excellent adhesion of the conformal coating.

Quite apart from the important role that good record-keeping played in this customer's problem-solving exercise, there are a number of lessons to be drawn from our customer's experi-

ence which, I hope, you'll take onboard when you embark on the search for new suppliers.

Firstly, incoming bare boards will provide an important determinant as to whether or not your coating achieves good adhesion. Remember, perfectly sound incoming boards can be made bad during the SMT assembly process, but bad incoming boards can never be made better!

Secondly, in your purchase specification, state the level of surface energy you require for incoming boards (generally greater than 40 dynes/cm) and TEST all incoming batches. REJECT any batch if it does not meet your specifications.

Thirdly, do not be afraid to audit new suppliers and, in particular, their manufacturing processes. This is the only way you will feel comfortable that they have a full understanding of what they are making, and how it might impact you should their manufacturing parameters drift out of specification.

Well, that's all from me for the time being and I hope you have found my columns on coatings helpful and of interest. Next month, my very able colleague, Alistair Little, technical director of Electrolube's global resins business, will be hosting this column.

Alistair's technical capabilities cover a broad range of related chemistries, including benzoxazine and phenolic resins for high-temperature applications; epoxy, epoxy meth/acrylate, urethane meth/acrylate, silane terminated polymer, polyurethane and unsaturated polyester systems. Alistair is also an expert in vinyl ester resin systems, and he is a member of the Royal Society of Chemistry, so rest assured the tips and tales from him will be expertly documented.

So, please do look out for his new column, which will focus on everything resin-related, including the types of products available, their special features and the issues that manufacturers might have to face when using them. Have a great summer and thank you for all your feedback. **PCBDESIGN**



**Phil Kinner** is global business/technical director of the Coatings Division at Electrolube.



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# Smaller Circuits: Material Properties and Thermal Issues

by John Coonrod

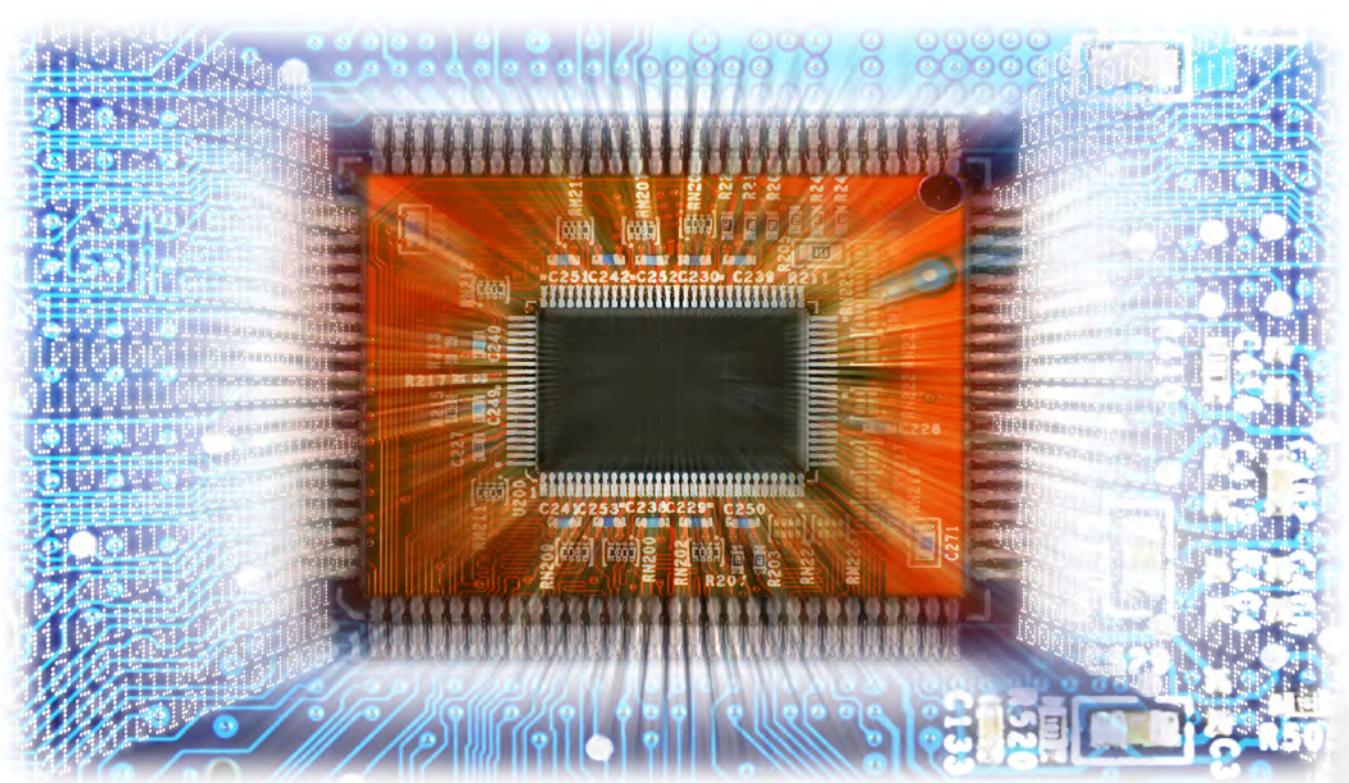
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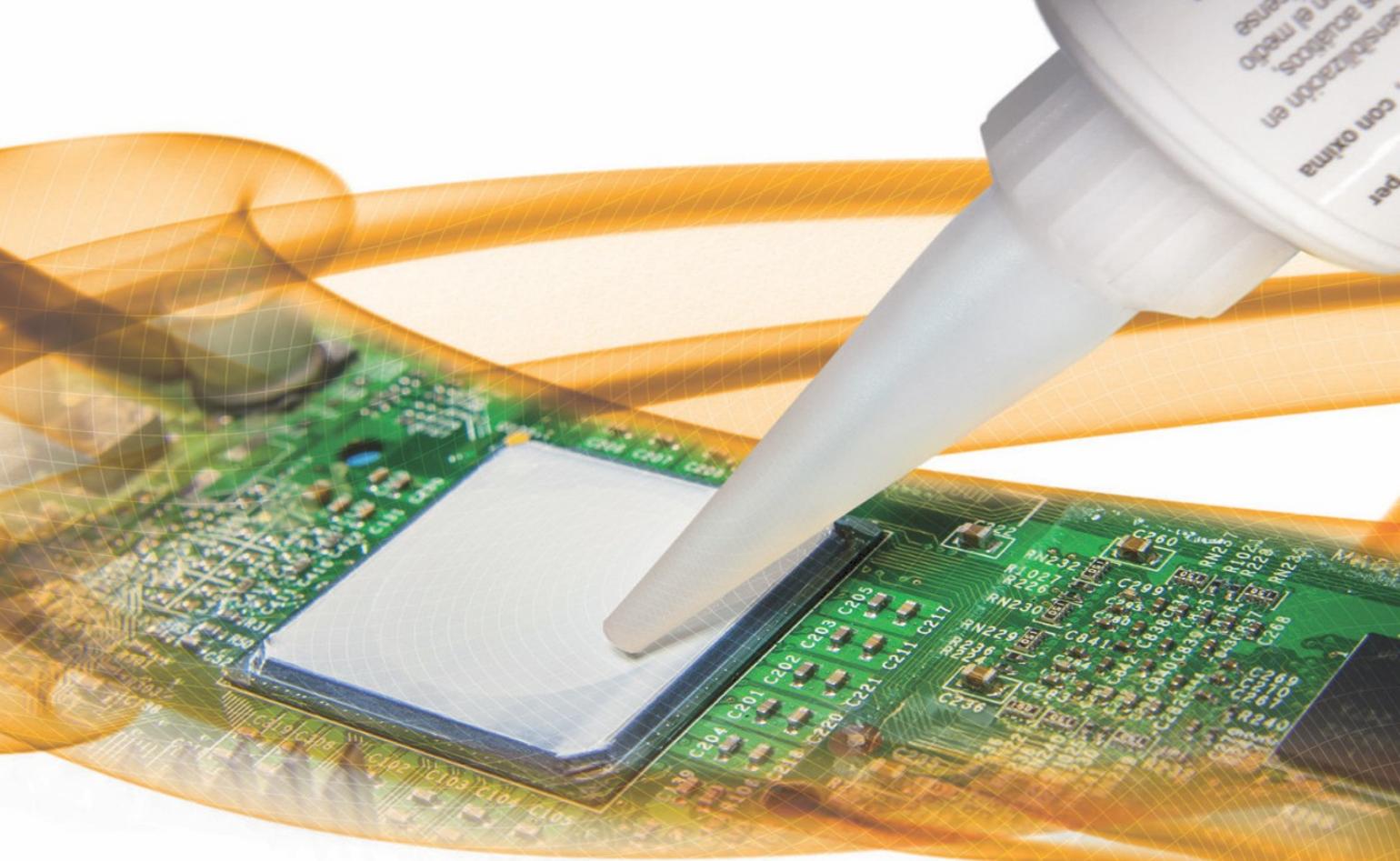
Many PCB applications experience thermal cycling as part of their normal end-use operation. Some PCB assemblies used in outdoor enclosures may see changes from 75–160°F in a single day, and over the course of several months, the temperature swing can be much greater. If the circuit design is optimized at room temperature around 75°F, then at 160°F, the electrical performance can be very different depending on the design and the circuit material used.

Some RF PCB designs may be more sensitive to thermal changes than others. For example, designs with small circuit features can be more sensitive to performance change due to thermal issues as compared to circuits with larger features. Since high-frequency circuits have small wavelengths, the circuit features are

also small. Also, with mmWave applications, a thinner circuit is needed in order to have proper wave propagation properties. Lastly, if a circuit has features which are tightly coupled, where a small space must be maintained between circuit features, that design can be more problematic for consistent electrical performance within a varying temperature environment.

Coefficient of thermal expansion (CTE) is typically considered for PCB reliability, but it can also have an impact on circuit performance for applications exposed to varying temperatures. Due to CTE, a circuit will change physical dimensions when the temperature changes. If the circuit has small features or tightly coupled features, the physical change of the circuit dimensions can cause a shift in electrical performance.





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Another material property which further complicates designing for significant temperature variation is temperature coefficient of dielectric constant (TCDk). The TCDk is a property that all materials have and is a measure of how much the material will change dielectric constant (Dk) with a change in temperature. One example: If a circuit is using a material with a high TCDk, such as 400 ppm/°C, the dielectric constant of the material will change 0.020 with a 46°C change in temperature. This temperature change is equivalent to the temperature range previously mentioned from 75°F, then at 160°F. The Dk change will impact the impedance, phase response and other circuit attributes. This

“An RF circuit using a material with a high TCDf will have more RF losses with an increase in operating temperature.”

impact would be in addition to the impact of the physical dimensional change of small circuit features which would occur over the temperature range if the circuit was designed for mmWave applications.

There are also issues associated with circuit attenuation or RF losses, due to thermal changes. The analog of the TCDk to dissipation factor is the temperature coefficient of dissipation factor (TCDf). Again, every material has this property and it is a measure of how much the dissipation factor (Df) will change with a change in temperature. An RF circuit using a material with a high TCDf will have more RF losses with an increase in operating temperature.

Another material issue is sometimes ignored. Copper increases resistance or is less conductive as it is heated. An increase in temperature will cause copper to have more conductor losses for a RF circuit. Conductor loss is one component of the overall insertion loss of a RF circuit. Conductor loss is frequency-dependent as well as

circuit thickness dependent. An increase in frequency will cause more conductor losses and a thinner circuit will be more sensitive to changes in conductor loss than a thicker circuit. As mentioned earlier, mmWave applications typically use thin substrates and are operating at very high frequencies. Due to this combination, PCBs used in mmWave applications are sensitive to conductor loss.

As the circuit increases temperature, the change in conductor loss worsens due to a decrease in copper conductivity. There is an additional loss which occurs as well and that is an increase in dielectric loss due to the TCDf of the material. An increase in temperature will cause the material to have worse Df and that combined with the conductor loss issue can be very troublesome for PCBs used at mmWave applications operating at elevated temperatures.

Some aging effects for substrates can be accelerated by extended elevated temperature exposures. Thermoset substrates which are used in the PCB industry will oxidize to some degree when evaluated over a long period of time. This assumes the substrate is in an environment with oxygen. The oxidation can cause a difference in the dielectric constant and dissipation factor of the material and the oxidation typically affects a relatively thin layer at the surface of the substrate.

When the dielectric material is protected by copper, oxidation cannot occur, and there may be some small amount of oxidation edge effect. The edge effect is more noticeable when the conductor width is narrow and the oxidation can migrate under the conductor from the edge next to the conductor where the substrate is exposed. RF performance with edge-coupled circuits which use an exposed substrate can be influenced by the oxidation more than circuits which are transmission lines and stubs where the copper protects the substrate. **PCBDESIGN**



**John Coonrod** is a senior market development engineer for Rogers Corporation. To read past columns or to reach Coonrod, [click here](#).

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# MilAero007 Highlights



## **[TTM Technologies Recognized by Raytheon Integrated Defense Systems](#)**

TTM Technologies Inc. announced that three facilities, Santa Clara (SC), Sterling (STE), and San Diego (SD) under its Aerospace and Defense/Specialty Business Unit were recognized by Raytheon Integrated Defense Systems on June 7, 2016 in two award categories for outstanding service, partnership, and excellence in engineering collaboration.

## **[Today's MilAero Options: Outsourcing—'Everybody's Doing it' Not so True Today](#)**

There was a time, not so many decades ago, when that most commonly-stated mantra ("lower labor costs") behind offshoring printed circuit fab (and some assembly) operations, still had some case-by-case validity.

## **[FTG Secures Licensing Agreement With EarthOne Circuit Technologies Corporation](#)**

Firan Technology Group Corporation announces a licensing agreement between FTG and EarthOne Circuit Technologies Corporation, whereby FTG will license the eSurface technology owned by EarthOne for use in the manufacture of printed circuit boards.

## **[Teledyne Completes Sale of Printed Circuit Technology Business](#)**

Teledyne Technologies Incorporated announced today the successful completion of the sale of assets of Teledyne's printed circuit technology business (Teledyne PCT) to FTG Circuits Inc., a California corporation and subsidiary of Firan Technology Group Corporation (FTG), for US\$9.3 million in cash.

## **[Consultants to EU Publish Recommendations on RoHS Exemptions](#)**

The Oeko-Institut e.V., Institute for Applied Ecology and Fraunhofer-Institut IZM for Environmental and Reliability Engineering, consultants to the European Union (EU) Commission (Commission) recently published their recommendations on 29 requested renewals of RoHS exemptions.

## **[Designing with Tighter Tolerances](#)**

David Ledger-Thomas is a PCB design engineer with Honeywell Aerospace. He's spent decades designing PCBs for a variety of applications, including defense, aerospace, computers, and high-performance audio. I asked David to share some of his thoughts on designing high-tech boards with increasingly finer spaces, traces and pitch.

## **[Setting a Satellite to Catch a Satellite](#)**

The target is set: a large derelict satellite currently silently tumbling its way through low orbit. If all goes to plan, in 2023 it will vanish—and efforts against space debris will have made a giant leap forward.

## **[OKI and Avio Ink Agreement on Transfer of PCB Business](#)**

The two companies will start negotiations on technologies and facilities transfer and a range of certifications from October 1, 2016 with a view to completing the business transfer by March 31, 2018.

## **[Zentech's Matt Turpin on IMPACT Washington, D.C.'s Benefits](#)**

At the recent IMPACT Washington, D.C. 2016 event in Capitol Hill, Matt Turpin, CEO of EMS firm Zentech discusses with I-Connect007's Patty Goldman his expectations on the event, its importance, and how, so far, it has helped the electronics manufacturing industry in the United States.

## **[OrbitOutlook Integrates Largest and Most Diverse Network of Space Sensors Ever to Help Avoid Collisions in Space](#)**

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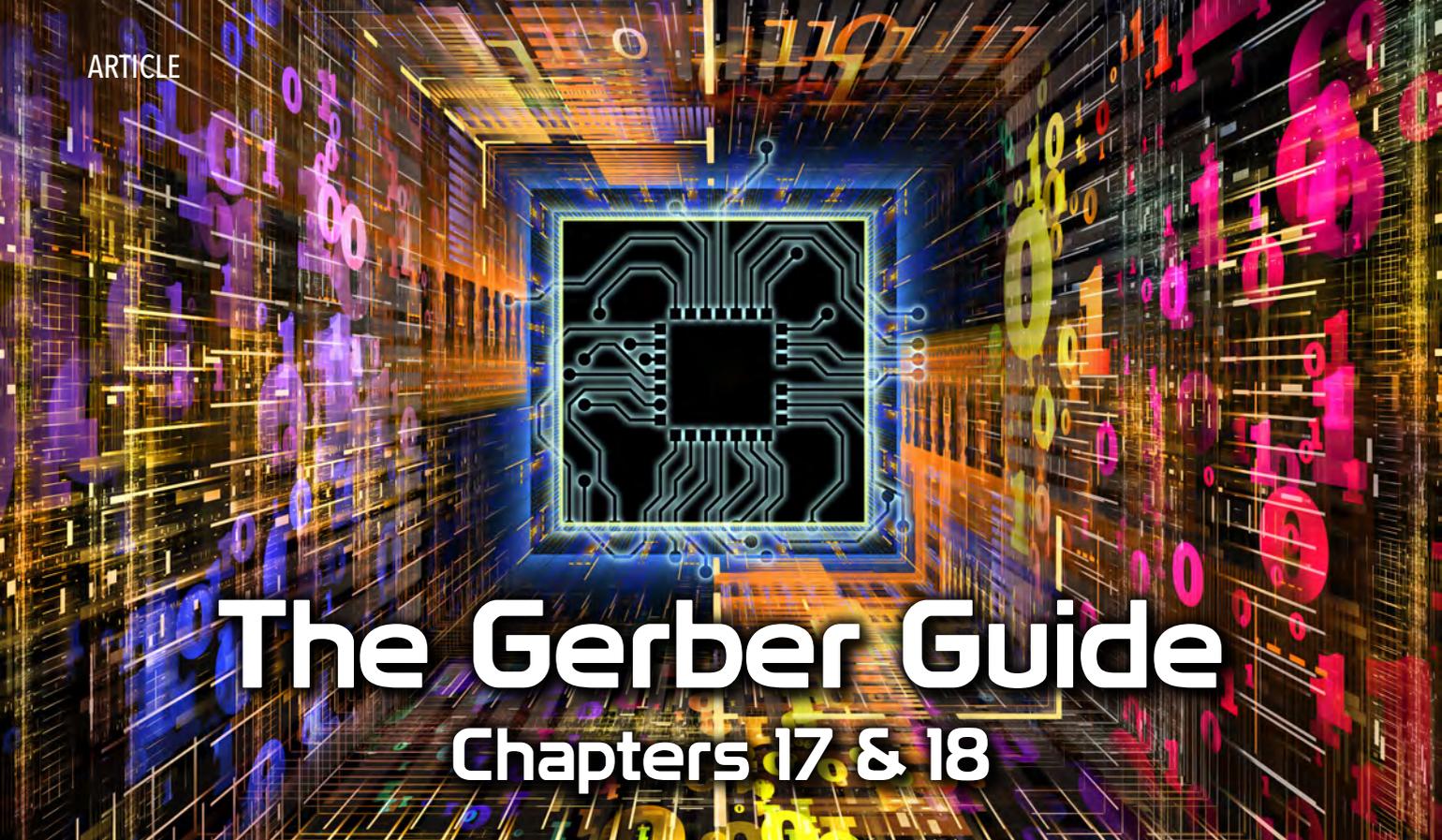
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# The Gerber Guide

## Chapters 17 & 18

**Karel Tavernier**  
UCAMCO

It is possible to fabricate PCBs from the fabrication data sets currently being used; it's being done innumerable times every day, all over the globe. But is it being done in an efficient, reliable, automated and standardized manner? At this moment in time, the honest answer is no, because there is plenty of room for improvement in the way in which PCB fabrication data is currently transferred from design to fabrication.

This is not about the Gerber format, which is used for more than 90% of the world's PCB production. There are very rarely problems with Gerber files themselves; they allow images to be transferred without a hitch. In fact, the Gerber format is part of the solution, given that it is the most reliable option in this field. The problems actually lie in which images are transferred, how the format is used and, more often, in how it is not used.

Each month, we look at a different aspect of the design to fabrication data transfer process. In this monthly column, Karel Tavernier explains in detail how to use the newly revised Gerber data format to communicate with your

fabrication partners clearly and simply, using an unequivocal yet versatile language that enables you and them to get the very best out of your design data.

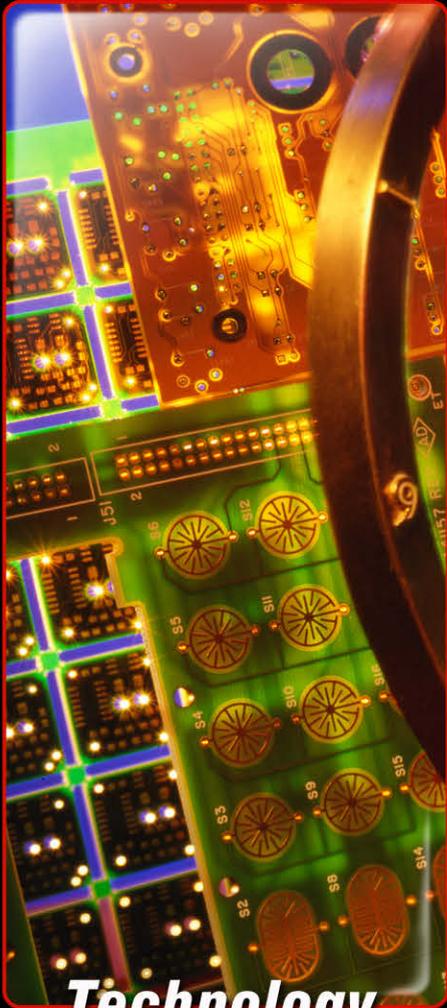
### **Chapter 17: Pads on Copper Layers**

The main function of copper is to conduct, but pads also have other functions: SMD, component, connector and test pads on outer layers provide electrical access to the circuit via the solder, paste and platings that they carry; thermal relief pads confine heat; and via pads, as well as providing electrical connections between the track and the barrel, also provide mechanical support for the barrel, and create room for drill positioning tolerances.

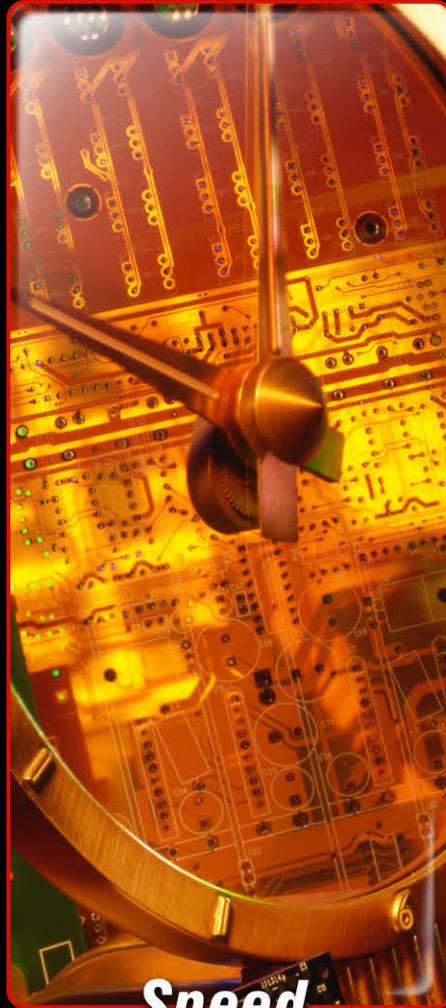
It is essential that pads be identified individually during the design and CAM stages so that they can be treated appropriately during the production processes: Via pads on soldermasks need a different treatment from SMD pads, and connector pads that are to be gold plated need a special gold mask for the plating process. And for electrical test, the test probes will only do their work properly if the location, size and shape of all pads is known. It is also important to realize that copper pads must be differentiated from other copper features when compensating for

# We Take the Time to do it Right

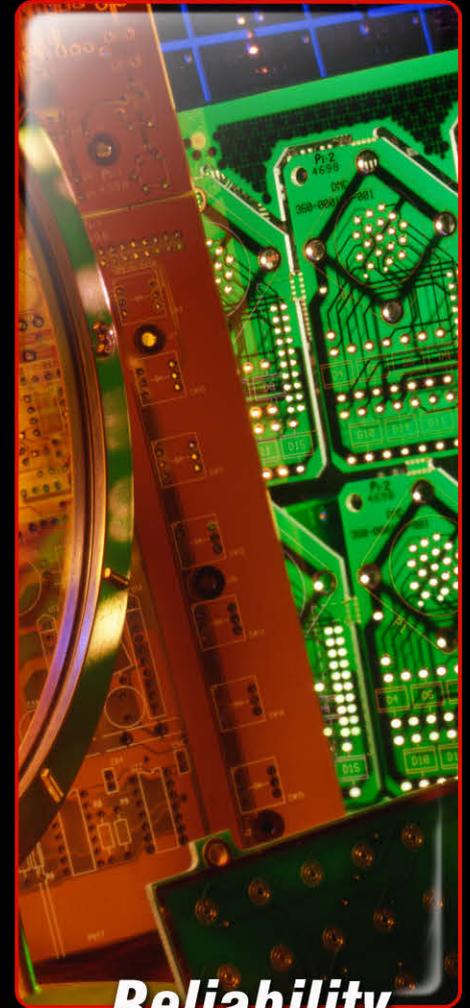
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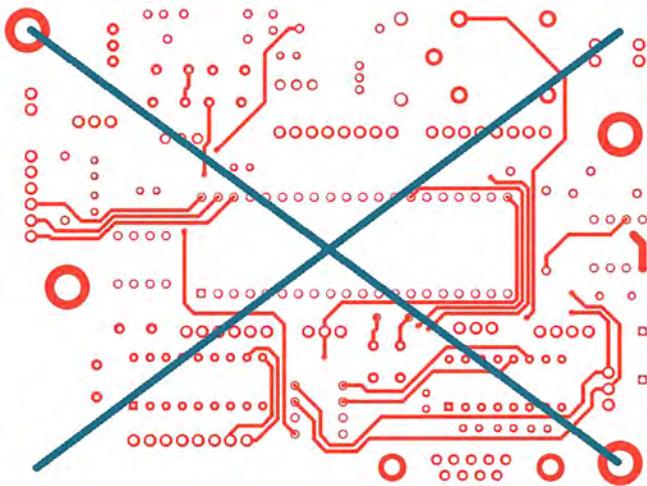


Figure 1: All donut pads—very confusing.

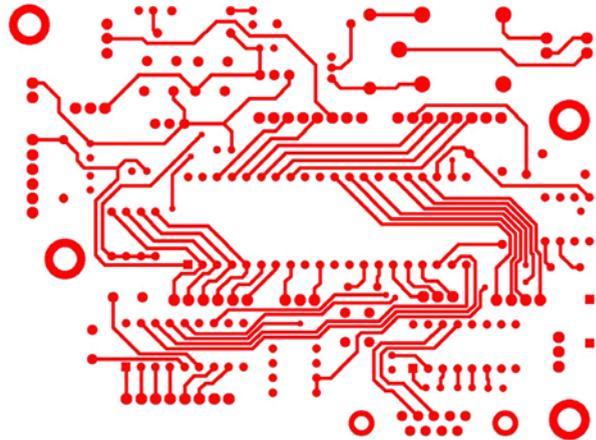


Figure 2: Proper pads—everything is clear.

production tolerances, as tolerances on pads are often tighter than those on conductive copper.

Thus CAM needs to know not only where and what the pads are, but must also be able to edit them efficiently. Consequently, pads must be differentiated from other copper features, but they must also be classified separately by type, size and function so that they can be modified separately.

The way to do this in Gerber is simple: All pads are represented using the flash of an aperture, with different apertures representing different types of pads, even if they are similar in size and shape. So a component pad and a via pad that are the same size will have different aperture numbers, making them easy to select and treat according to their different needs. Pads should only be made using flashes, and flashes should only be used to make pads.

Painted (stroked) pads are evil because they are so hard to edit. If a Gerber file served merely as an image, painted pads would be fine. However, a Gerber file must also be editable, which, as we said, is not possible for painted pads.

Remember: All pads must be flashes, and all flashes must be pads.

### Further Notes on Copper Pads

#### *Always flash embedded pads*

Embedded pads are pads that are fully within a bigger copper area (e.g., a via pad in an

SMD pad, or an SMD pad on a copper pour). Image-wise these pads have no effect; whether they are present or absent, the image remains the same. However, CAM must know where and what the pads are, and a valid Gerber file will convey that information. The embedded pads must be present in your Gerber file; don't "optimize" your output by removing them!

#### ***Do not use donuts!***

Sometimes pads on a plated hole are represented by a donut rather than a solid pad (Figure 1). Presumably, this is to make room for the drill hole or to indicate that copper will be removed. And it is true, copper will be removed. However the donut is very impractical because it does not fit how the copper is removed. The copper is not removed by imaging. First a solid pad is created by imaging, and then the pad is drilled. Consequently, CAM must laboriously replace all the donuts with solid pads to prepare for imaging. Furthermore with non-plated pads which typically truly are donuts, plated donuts are confusing. Drill plated pads must be solid (Figure 2). Whatever you want to express by using a donut is better expressed in another way.

### Chapter 18: The contents of the fabrication data set

All files in a fabrication data set are stored in an industry standard archive format (e.g., rar, zip, 7z). The archive should only contain data

pertaining to *one single* PCB. Putting more than one PCB in an archive is confusing; even if you use a clever file naming scheme or comprehensive explanatory note, you are potentially creating a lot of confusion by putting different PCBs in the same archive.

Remember: one PCB, one archive.

The question is what must and must not be included in the fabrication data set. Obviously, the archive must contain all data needed to fabricate the board, in a standard and unequivocal format and manner. Less obviously, the archive must not contain other files, superfluous data or duplicates. The reason is that the manufacturer must check each file to see if it contains relevant instructions. Superfluous files waste his time and increase the risk that he misses something essential. Aperture list files are superfluous, for example, as all the required aperture information is in the Gerber files. CAD data is also useless as it requires CAD software to handle it. Duplicate information is even worse as the fabricator must compare the different files to check whether they contain conforming instructions, and conflicts raise questions about what is now valid. Duplicate image information (e.g., in Gerber and ODB++ format) is especially aggravating as images are complex and hard to compare—which tolerances apply?

It is mandatory that *one single* Gerber file should be provided for *each* patterned layer (copper, solder mask, legend, etc.) and for each drill sequence present.

This rule is violated every time that only one solder mask is provided “because top and bottom are identical.” This obnoxious habit may save a few bytes but then questions arise about whether a mask was forgotten and which masks must now effectively must be on the board. Confusion. The space saving is illusory anyway as the first thing the CAM operator must do is to create two masks from the single file. A bigger archive is better than a confusing archive, and when both masks are present, even if they are identical, everything is clear.

Also mandatory are all fabrication drawings—in Gerber format—and fabrication instructions such as finishes, ROHS etc. If it is not mandatory, it must not be there.

Finally, and even if this seems like a superfluous duplication of data, the CAD netlist should always be included ([Chapter 8](#) in this series). This genuinely original data provides a powerful and essential checksum on the data, and is far better than a netlist generated from the image data, which is only a reverse-engineered approximation.

Make the fabrication data set as simple as possible, but no simpler. **PCBDESIGN**

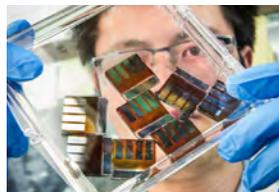


**Karel Tavernier** is managing director of Ucamco.

## NREL Technique Leads to Improved Perovskite Solar Cells

Scientists at the Energy Department’s National Renewable Energy Laboratory (NREL), in collaboration with researchers at Shanghai Jiao Tong University (SJTU), devised a method to improve perovskite solar cells, making them more efficient and reliable with higher reproducibility.

The research, funded by the U.S. Department of Energy SunShot Initiative, involved hybrid halide perovskite solar cells and revealed treating them with a specific solution of methyl ammonium bro-



mide (MABr) would repair defects, improving efficiency.

The scientists came up with a better method, using what’s called the Ostwald ripening process. The process involves small crystals dissolving and then redepositing onto larger crystals. The researchers were able to induce the Ostwald ripening process by treating the perovskite with a MABr solution.

The perovskite cells treated with MABr were shown to be more efficient than those without the treatment.

# TOP TEN



## Recent Highlights from PCBDesign007

### 1 **Beyond Design: Mastering “Black Magic” with Howard Johnson’s Seminars**

Barry Olney recently reviewed Dr. Johnson’s High-Speed Digital Collection, a total of 36 hours of viewing time. The picture that Howard paints leaves a lasting impression on how electromagnetic fields propagate and how they induce voltages and current (crosstalk) into nearby signals. Here is a section-by-section discussion of the course contents. You will be on the edge of your seat.



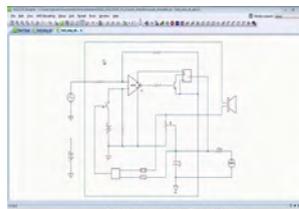
### 3 **EMA Acquires Accelerated Designs for its Extensive Part Library and Expertise**

EMA Design Automation has acquired Accelerated Designs, a company known for its dominance in EDA part library content and solutions including a 7.2-million-part database and its specialist library tool Ultra Librarian.



### 2 **Mentor Graphics Extends the PADS PCB Product Creation Platform**

The vast majority of today’s electronic products contain analog content which must be designed and validated in the context of the overall system, making analog/mixed signal simulation critical for product creation. To address this need, the new PADS AMS Cloud, a cloud-based circuit exploration/simulation environment and user community, is free to all PADS users.



### 4 **Software Bytes: Having Fun With Impedance**

About a year ago, I was assigned a new project: become an expert in impedance, more or less. I had no idea how much this research would bring out the nerd in me. I’m still not an impedance guru, but I’ve learned a lot about how impedance requirements affect PCBs. Even if you don’t typically design controlled-impedance circuit boards, you probably will eventually.



## 5 IPC Designers Council OC Chapter Meeting Features Julie Ellis of TTM

Last month, Judy Warner attended the Orange County chapter of the IPC Designers Council. Once again, the room was packed with over 70 PCB designers and electronics professionals. This “lunch-and-learn” meeting featured a presentation by Julie Ellis of TTM, “Printed Circuit Board Cost-Adders.”



## 6 EDA Industry Revenue Up 4.5% to \$1.96B in Q1 2016; PCB up 2.8%

The Electronic System Design (ESD) Alliance reports that EDA industry revenue increased 4.5% in Q1 2016 to \$1.96 billion, compared to \$1.87 billion in Q1 2015. PCB/MCM revenue of \$166 million in Q1 represents an increase of 2.8% over Q1 last year.



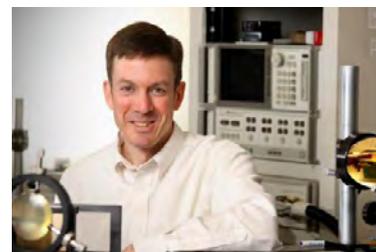
## 7 Designing for Profitability: Don't Over-Materialize

John Bushie, applications engineering manager at ASC, spoke with Barry Maties recently about ways that designers can avoid over-materializing. He also outlined the benefits of designing for profitability.



## 8 UVA Teaches PCB Design With NI AWR Tools

“Using NI AWR software in my RF and microwave classes and labs has given my students strong hands-on experience, as well as a better view of how and why components interact as they do,” said Scott Barker, professor at UVA. Barker teaches a class on RF and wireless circuits, using NI AWR design tools.



## 9 Designing With Tighter Tolerances

David Ledger-Thomas is a PCB design engineer with Honeywell Aerospace. He's spent decades designing PCBs for a variety of applications, including defense, aerospace, computers, and high-performance audio. I asked David to share some of his thoughts on designing high-tech boards with increasingly finer spaces, traces and pitch.



## 10 Cadence Reports Revenue of \$453M in Q2 2016

Cadence reported second quarter 2016 revenue of \$453 million, compared to revenue of \$416 million reported for the same period in 2015. For the third quarter of 2016, the company expects total revenue in the range of \$440 million to \$450 million.

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# Events



For IPC Calendar of Events,  
[click here](#).

For the SMTA Calendar of Events,  
[click here](#).

For a complete listing, check out  
The PCB Design Magazine's  
[event calendar](#).

## [IPCA EXPO 2016](#)

August 18–20, 2016  
Delhi, India

## [NEPCON South China](#)

August 30–September 1, 2016  
Shenzhen, China

## [PCB West Conference and Show](#)

September 13–15, 2016  
Santa Clara, California, USA

## [Medical Electronics Symposium](#)

September 14–15, 2016  
Marylhurst, Oregon, USA

## [24th FED Conference](#)

September 15–16, 2016  
Bonn, Germany

## [ICT Evening Seminar](#)

September 20, 2016  
Newtown House Hotel, Hayling Island, UK

## [EDI CON](#)

September 20–22, 2016  
Boston, Massachusetts USA

## [EIPC Workshop on Reliability](#)

September 22, 2016  
Tamworth, UK

## [IPC India/electronics India 2016/ productronica India 2016](#)

September 21–23, 2016  
Bengaluru, India

## [IPC Fall Committee Meetings](#)

September 24–30, 2016  
Rosemont, Illinois, USA

## [SMTA International 2016](#)

September 25–29, 2016  
Rosemont, Illinois, USA

## [electronicAsia](#)

October 13–16, 2016  
Hong Kong

## [TPCA Show 2016](#)

October 26–28, 2016  
Taipei, Taiwan

## [Electronica](#)

November 8–11, 2016  
Munich, Germany

## [FUTURECAR: New Era of Automotive Electronics Workshop](#)

November 9–10, 2016  
Atlanta, Georgia, USA

## [Printed Electronics USA](#)

November 16–17, 2016  
Santa Clara, California, USA

## [International Printed Circuit & Apex South China Fair \(HKPCA\)](#)

December 7–9, 2016  
Shenzhen, China

## [DesignCon 2017](#)

January 31–February 2, 2017  
Santa Clara, California, USA

## [IPC APEX EXPO 2017 Conference and Exhibition](#)

February 14–15, 2017  
San Diego, California, USA

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