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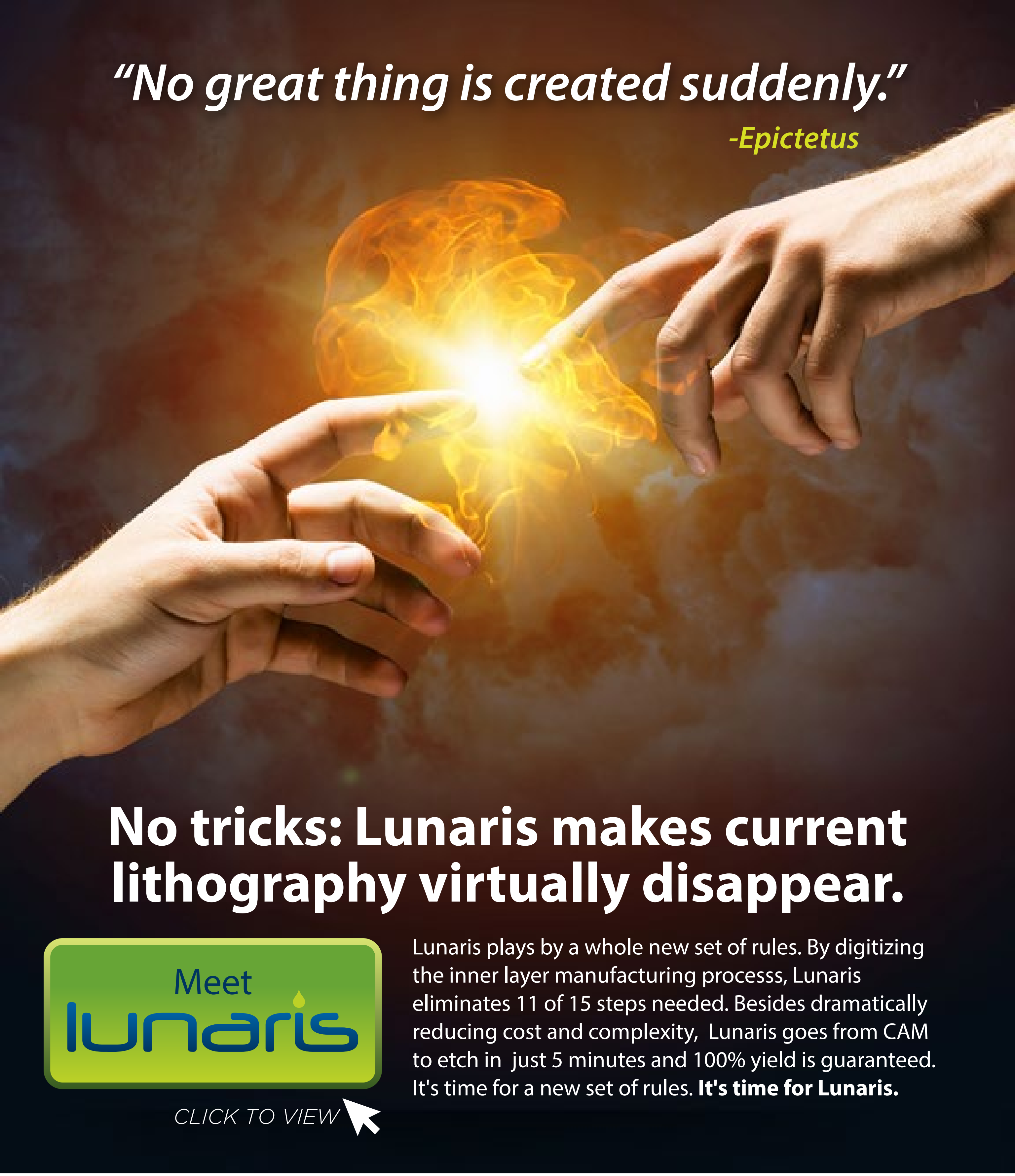
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HDI

Sustainability—What and Why?

by Joe Fjelstad
VERDANT ELECTRONICS

In 2013, Earth welcomed roughly 140 million new citizens, replacing approximately 60 million who passed away, netting a growth in the world's population of 80 million people—a number which happens to roughly match the population of Egypt. The Earth's population now stands at more than 7.2 billion. (For those interested, real-time statistical estimates for population and other subjects of significance including health and environmental matters can be found at www.worldometers.info.)

The numbers are staggering and border on the incomprehensible. They also present an ongoing challenge to us all to find ways to make certain that those just joining the human race have a chance to realize their potential. Without question, it is a huge challenge we collectively face. Presently and throughout history, there has existed a great divide between more advanced and exploitative cultures and nations and the many still developing peoples and nations of the world that coexist on this, our little 'blue marble' in space, or as futurist and visionary Buckminster Fuller aptly called it, "Spaceship Earth." He asserted, and rightly so, that we are all astronauts and as its crew, we needed to maintain the delicate balancing act to assure that Spaceship Earth will allow us to survive future trips around our sun.

The resources of our planet are unquestionably limited and thus are diminishing as we continue to unleash and ramp up a seemingly never-ending flow of products to both serve and amuse us with output of the global electronics industry likely to be nearing the top of the list of "offenders." In that regard, we are becoming victims of our own success, to one degree or another. For better or for worse, the engine of economics runs on the fuel that the consumers' wants must always exceed their needs. Moreover, product developers and promoters are putting forth their best effort to make sure that as many of their products as possible can be perceived as needs rather than simple wants. Presently, their focus remains targeted on those of us who inhabit the top of the world's economic pyramid and our numbers exceed 3.5 billion people. A substantial market to be sure and already there is evidence that we are, or soon will be, stretching the limits of natural resources. This leaves half of the world's population on the outside looking in. It would seem that, if

we are going to satisfy the expectations of those billions of people not fortunate enough to be born in the right place at the right time, we are going to have to make some adjustments in our approach to the design and manufacture of future products. In short, we are going to have to look very seriously at what we might need to do to create a truly sustainable electronics manufacturing industry in the future.

This begs the question: "What is a sustainably manufactured product?" Unfortunately this is not a simple question, and without surprise one finds that the answer is not simple either. That said, there are think tanks out there where people grapple with the problem. One such is the Lowell Center for Sustainable Production. They have created a reasonably comprehensive checklist for those seeking to make an effort to create products and processes that are sustainable. Following is a condensed summary of their "litmus test" checklist[1].

Sustainable products are:

1) Safe and ecologically sound throughout life cycle and:

- designed to be durable, repairable, readily recycled, compostable, or easily biodegradable
- produced and packaged using the minimal amount of material and energy possible

2) Processes that are designed and operated such that:

- wastes and ecologically incompatible byproducts are reduced, eliminated or recycled on-site
- substances or physical agents and conditions that present hazards to human health or the environment are eliminated
- energy and materials are conserved, and the forms of energy and materials used are most appropriate for the desired ends
- work spaces are designed to minimize or eliminate chemical, ergonomic and physical hazard

The above checklist is succinct but it also offers the user targets, which are reasonably clear and measurable. This is important for as every scientist and engineer knows, until you can apply numbers to any effort you have no way of knowing how well you're doing. The one thing that appears to be missing from the list in the view of this writer is a statement about the need for greater reliability. If we can make products that will last indefinitely, we don't have to make them again. This may fly in the face of the sensibilities of product marketers today who seek to have a new product on the shelf every 12–18 months, if not sooner. However, such product marketers have little or no appreciation of the situation of the peoples who inhabit much of the developing world. If one is making as little as two dollars a day, the products they purchase must be durable, for they cannot afford to replace them on a whim.

Fortunately, the CEOs of corporations large and small are beginning to appreciate the importance of sustainability even as they wrestle with the challenge of addressing it. This is evident based on results of a recent and broadly cited Accenture study on sustainability wherein 1,000 CEOs in 27 different industries were questioned about the importance of sustainability on the future success of their businesses. The answers to the questions were promising. A total of 93% of CEOs affirmed the importance of sustainability for the future of their company. And 80% felt the sustainability would offer them competitive advantage, while 78% felt that pursuing sustainability would enhance innovation and growth within their companies. Unfortunately, as pragmatists, only a third of them felt that the global economic situation was on track to meet targets or making the kind of effort required to address the sustainability challenge. Moreover, they seemed conflicted as less than half of them believed they can quantify their efforts and perhaps more importantly, they felt that sustainability efforts will likely always take a backseat to profitability.

"Therein lies the rub" as the Bard of Avon so nicely phrased it. Given there is no clear-cut and well-defined path to sustainability, given the wide range of electronic products being developed and sold as well as the myriad materials and processes used in their manufacture, it appears we are somewhat living the parable of the blind men describing an elephant. Here again for emphasis is repositioned the nagging concern that most of the attention of our electronics industry is focused on serving the needs of just half of the world's population—the top half. We have a long way still to go to meet the needs of those on the bottom, but as the philosopher Edmund Burke observed, "The greatest mistake that one can make is to do nothing because one can only do a little." Making the effort to build truly sustainable products seems a reasonable objective; but do we have the will?

The elimination of solder, which is the primary cause of defects and failures, seems to be a likely target, but who in the developed nations will be the first to embrace such a radical concept? If coupled with the use of aluminum as a substrate, the impact provides immense benefits to those whose birthplace did not do them a favor. Sadly, most corporate leaders today are more akin to sheep and lemmings than to the bold thought leaders of earlier eras. They speak of boldness, but their actions are anything but. Given their self exclusion as agents of change, it will be left to the younger readers of this appeal to deliver the promise because it seems certain that it will not come from those about to retire or hanging around to enjoy the perks.

In closing, I am reminded of a senior engineer who sat behind me during my tenure at Boeing more than 30 years ago. He tried to calm me when my much younger self expressed deep frustration at the pace of progress with the implementation of some of our process improvements, by saying this: "Joe, you need to keep in mind the simple fact that everyone wants to go to Heaven but nobody wants to die." It was and still is the truth. So it goes...

Next time, an unflinching look at the dark side of solder. **PCB**

Reference

1. Lowell Center for Sustainable Production

Verdant Electronics Founder and President Joseph (Joe) Fjelstad is a four-decade veteran of the electronics industry and an international authority and innovator in the field of electronic interconnection and packaging technologies. Fjelstad has more than 250 U.S. and international patents issued or pending and is the author of Flexible Circuit Technology.

Smarter Smartphone with "Deep Learning" Innovation

Researchers are working to enable smartphones and other mobile devices to understand and immediately identify objects in a camera's field of view, overlaying lines of text that describe items in the environment.

"It analyzes the scene and puts tags on everything," said Eugenio Culurciello, an associate professor in Purdue University's Weldon School of Biomedical Engineering and the Department of Psychological Sciences.

The innovation could find applications in "augmented reality" technologies like Google Glass, facial recognition systems and robotic cars that drive themselves.

The concept is called deep learning because it requires layers of neural networks that mimic how the human brain processes information. Internet companies are using deep-learning software, which allows users to search the Web for pictures and video that have been tagged with keywords. Such tagging, however, is not possible for portable devices and home computers.

"When you give vision to machines, the sky's the limit," Culurciello said.

Lead-Free Reflow for High-Layer-Count PCBs

by Happy Holden, RETIRED
and Michael Carano,
OMG ELECTRONIC CHEMICALS, LLC.

This article is an update of the Holden-Carano article originally published in the February 2013 issue of The PCB Magazine.

Abstract

One of the most difficult printed circuit boards to adapt to Pb-free assembly processes is the high-layer count multilayer. Often, these multilayers have through-hole and hand-soldered components, and requirements for two or more rework cycles. The higher reflow temperatures and slower wetting of lead-free solders place an enormous strain on the laminate and copper-plated hole barrel. In many cases, the boards cannot be assembled reliably even with newer, higher thermal performance FR-4s.

One solution to this problem is to redesign the multilayer using current design rules and newer innovative fabrication technologies. This article will review four of these new and enabling technologies:

- Laser-drilled microvias
- Routing BGA using channels
- Contribution of new SMT connectors
- Layer assignment changes (architectures)

Microvias offer the most significant opportunity to reduce not only the layers and thicknesses of multilayers, but also their cost while improving their electrical performance and density. Several examples will illustrate these new opportunities. Since blind vias are surface phenomena, to get the maximum benefit from them, layer assignment for signal, ground and power need to be reviewed and alternative constructions considered. These blind vias, by reducing

the number of through-holes, contribute to increase routing density that allows the lower layer usage. Finally, by replacing through-hole connectors with surface mount connectors, higher connector density and improved electrical performance can be realized.

The resulting new multilayers are not only thinner, cheaper, and easier to design, but are less costly and suitable for lead-free assembly.

Challenges of Lead Free

Environmental regulations are placing increased requirements upon printed circuits. The European Union's Restriction of Hazardous Substances (RoHS) and Waste Electrical and Electronic Equipment (WEEE) directives will significantly affect the requirements placed upon base materials. Among other elements, RoHS restricts the use of lead (Pb). Tin/lead (Sn/Pb) alloys have been used for many years in the assembly of printed circuits. Eutectic Sn/Pb has a melting point of 183°C and temperatures during assembly commonly reach 230°C. The primary alternatives to Sn/Pb are tin/silver/copper (Sn/Ag/Cu or "SAC") alloys. These alloys have melting points near 217°C with typical peak assembly temperatures reaching 255–260°C. This increase in assembly temperature coupled with the possibility of multiple exposures to these temperatures requires the base materials to have improved thermal stability. Recent technical papers have illustrated important data on the effect of Pb-free assembly on base materials[1,2]. While there are many important properties to consider, there are a few that deserve special attention in light of current trends and the resulting need for improved thermal performance. These include:

- The glass transition temperature (T_g),
- Coefficients of thermal expansion (CTEs),
- Decomposition temperature (T_d)

"Experience is showing that the decomposition temperature is a critical property, and appears to be at least as important, if not more important than the glass transition temperature when planning for Pb-free assembly conversion."

Effect on Laminates

As the temperatures to which printed circuits are exposed increases, as in Pb-free assembly processes, the decomposition temperature of the material becomes a much more critical property to understand[4]. The decomposition temperature is a measure of actual chemical and physical degradation of the resin system. This test uses thermogravimetric analysis (TGA), which measures the mass of a sample versus temperature. The decomposition temperature is reported as the temperature at which 5% of the mass of the sample is lost to decomposition. Experience is showing that the decomposition temperature is a critical property, and appears to be at least as important, if not more important than the glass transition temperature when planning for Pb-free assembly conversion. While the definition of the decomposition temperature uses a weight loss value of 5%, it is very important to understand the point at which 2–3% weight loss occurs, or where the onset of decomposition begins. In examining soldering reflow profiles, traditional Sn/Pb assembly processes can reach peak temperatures of 210–245°C, with 230°C a very common value. In this range, most FR-4s do not exhibits significant levels of decomposition. However, if you examine the temperature range where Pb-free assembly processes are operating, you can see that the traditional FR-4 materials exhibit a 2–3% weight loss. Severe levels of degradation can result from multiple exposures to these temperatures. This problem is increased when there are 20+ layers, resulting in thicker boards, and many are power or ground planes.

Consequences for Multilayers

While the simplest steps to comply with Pb-free assembly may be changing the base laminate and replacing the tin-lead finish, this may not be suffiecient for thick, complex, high-layer-count multilayers. These multilayers have a much higher thermal mass as well as increased through-hole parts and copper planes. With the possible increased need for rework of complex parts and hand-soldering, the total thermal environment may exceed what any FR-4 is capable of. When this occurs, the remedy is to reduce the thermal mass by reducing the mulitlayer's layers. Four main alternatives that can be used are:

- Laser-drilled microvias
- Layer assignment changes (architectures)
- Routing BGA using channels
- Contribution of new SMT connectors

Moving to Microvias

Microvias are nearly 30 years old now, having been used in high-volume by OEMs like Hewlett Packard for their first 32-bit computer—the FOCUS chip—in their HP9000 m845 desktop computer starting in 1983. They employed laser drilling of blind vias in an 8-layer PTFE dielectric with copper used as the core layers for cooling (termed "finstrate" for this feature). Other OEMs like IBM and Siemens also developed microvias technologies for their computers, but the technology did not really take off until the need for miniturization in portable products like cellular phones increased. Today it is the fasting growing segment of interconnect packaging, used in portable products, IC and ASIC packaging and in large complex multilayers for telecom and servers. Figure 1 shows the rapid growth of microvias during the early 2000s.

Multilayer Cost-Density Tradeoffs

In designing classical PWBs, there is a wiring barrier created by the size of component lands, traces and vias. If you look at a square inch of PCB real estate, there are only so many SMT land patterns, traces connected to the land and vias connected to the trace that you can put in that one square inch before it is full. Depending on the SMT land size, this barrier is called the TH wiring barrier[3].

HDI microvias provide the opportunity to reduce the number of layers of traditional

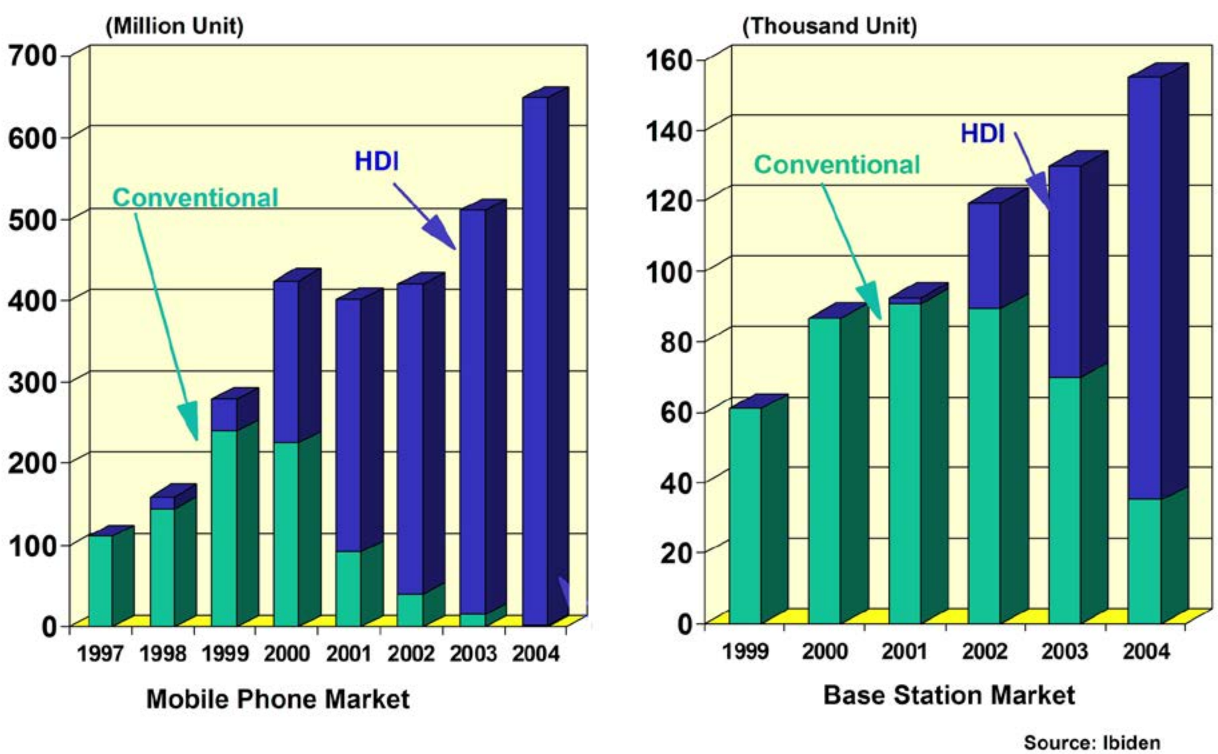


Figure 1: The rapid increased use of microvias has been fueled by the popularity of cellular phones and the need to make them as small and as light as possible. Now, all products use microvias.

through-hole boards. Typically, microvias are 6 mil with 12-mil pads, while TH vias are 13 mils with 24-mil pads. This obvious increase in space is multiplied by the fact that a blind via only goes from the surface down to the second or third layer. This opens up additional channels on the rest of the innerlayer to route additional traces. The other opportunity with HDI is the reduction of trace widths to go along with the reduction in dielectric thicknesses. Three mil (0.003") are not uncommon as well as 3.5-mil lines and spaces. This provides the opportunity to route 80–100 traces per square inch.

This increase in density is illustrated in the cost-density tradeoff chart (Figure 2). The first column (A) is traditional TH boards from 4–40 layers. The prices (RCI) have all been adjusted to a basis of the cost of an 8-layer TH board from China. The DEN is the average density of the stackup in pins per square inch. To find the equivalent of a particular TH board, move diagonally, following the dashed lines.

For example, if you had a 22-layer TH multilayer (RCI=6.67), the HDI type II (D) would be a 14-layer board (RCI=3.32); the type III (E) would be a 10-layer, RCI=2.30. These all have approximately the equivalent DENsity, but the HDI boards are less costly by 50% for the type II and 65.5% for the type III.

THRU-HOLE VS. STAGGERED MICROVIA HDI: COST & PIN DENSITY

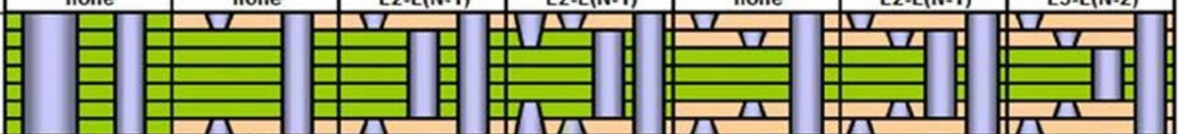
ID	A		B		C		D		E		F		G	
Type	THRU-HOLE		1 BUILD-UP Blind		1 BUILD-UP Blind & Buried		1 BUILD-UP Blind & Buried		2 BUILD-UP Blind		2 BUILD-UP Blind & Buried		2 BUILD-UP Blind & Buried	
Stackup	N		1+N+1		1+bN+1		1+bN+1		2+N+2		2+bN+2		2+bN+2	
Micro Vias	none		L1-L2		L1-L2		skip via L1-L3 stagger L1-L2, L2-L3		stagger L1-L2, L2-L3		stagger L1-L2, L2-L3		stagger L1-L2, L2-L3	
Buried Vias	none		none		L2-L(N-1)		L2-L(N-1)		none		L2-L(N-1)		L3-L(N-2)	
Stackup & Via Models														
Signal Layers	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN
4L	0.6	20	0.8	40	1.1	40	1.3	40	1.4	135	- -	- -	- -	- -
6L	0.8	20	1.0	60	1.2	60	1.5	60	1.6	180	1.7	220	1.9	240
8L	1.0	30	1.2	100	1.5	100	1.7	100	1.9	240	2.1	240	2.3	300
10L	1.3	40	1.5	200	1.8	180	2.1	180	2.3	300	2.5	300	2.7	400
12L	1.7	60	1.9	210	2.3	220	2.6	220	3	350	3	500	3	500
14L	2.2	70	2.5	220	3	250	3	260	4	400	4	600	4	600
16L	3	80	3	260	4	300	4	300	5	500	5	800	5	800
18L	4	100	4	300	5	330	5	350	6	600	6	1000	7	1000
20L	5	105	5	360	6	380	7	400	8	700	8	1200	9	1200
22L	7	110	7	400	8	425	9	450	10	800	10	1300	11	1300
24L	9	125	9	460	10	480	11	500	12	1000	13	1400	14	1400
26L	11	130	11	500	13	550	14	600	15	1200	16	1500	17	1600
28L	13	135	14	540	16	620	17	700	18	1300	19	1600	29	1800
30L	16	140	17	580	18	690	20	800	21	1400	22	1650	23	2000
32L	18	145	19	620	21	770	23	900	24	1450	25	1700		
34L	21	150	22	660	24	900	26	1200	26	1500	27	1800		
36L	23	160	24	700	26	1000					30	2000		
38L	25	180	26	740	RCI = Relative Cost Index									
40L	26	200			DEN = Density: Pins/Square Inch						© Happy Holden 2006-2011			

Figure 2: The price-density matrix compares the relative prices (RCI) of through-hole (TH) boards to their equivalent HDI-microvias boards, along with average density (DEN) of pins per square inch[3].

Layer Assignment (Architecture)

Blind microvias are a surface feature. In order to help reduce the number of layers of a traditional multilayer with microvias, more work needs to be performed on the three surface layers of each side of the board. This is illustrated in Figure 3.

First priority is to reduce and eliminate through-vias. These block routing channels on the innerlayers. By eliminating 25% of the TH, two to three times as many traces can be routed on the innerlayers. One way to do this is to move the ground-plane (usually on layer 2) to the surface and use the microvias as via-in-pad (VIP) or near-via-in-pad (NVIP). This eliminates the most abundant vias on the boards—the ones to ground. In non-critical areas, this surface ground pour can be connected to other ground layers. The second most abundant vias are to power, so by moving this plane to layer 2, a blind via can connect SMT pads to this plane and not be very deep. Signals will start on layer 3, and depending on line-width, these skip-vias will not be very deep and will have a conventional aspect ratio and land size.

If higher wiring density is required, then layer 2 and 3 should be signals. If fine lines are used (~3 mil), then skip vias will allow X-Y connections, otherwise, buried vias (type II) or buried microvias (type III) are required to connect the two signal layers.

Routing BGAs Using Channels

Noting the importance of using the blind microvias to eliminate TH, a second important function, especially on large boards that have high I/O BGAs, is where the microvias are placed. Historically, the blind vias were placed around the perimeter of the BGA. This works well for BGAs with <400 pins, but for the new BGAs, like FPGAs, which contain 300 to more than 1700 pins, the blind vias are placed differ-

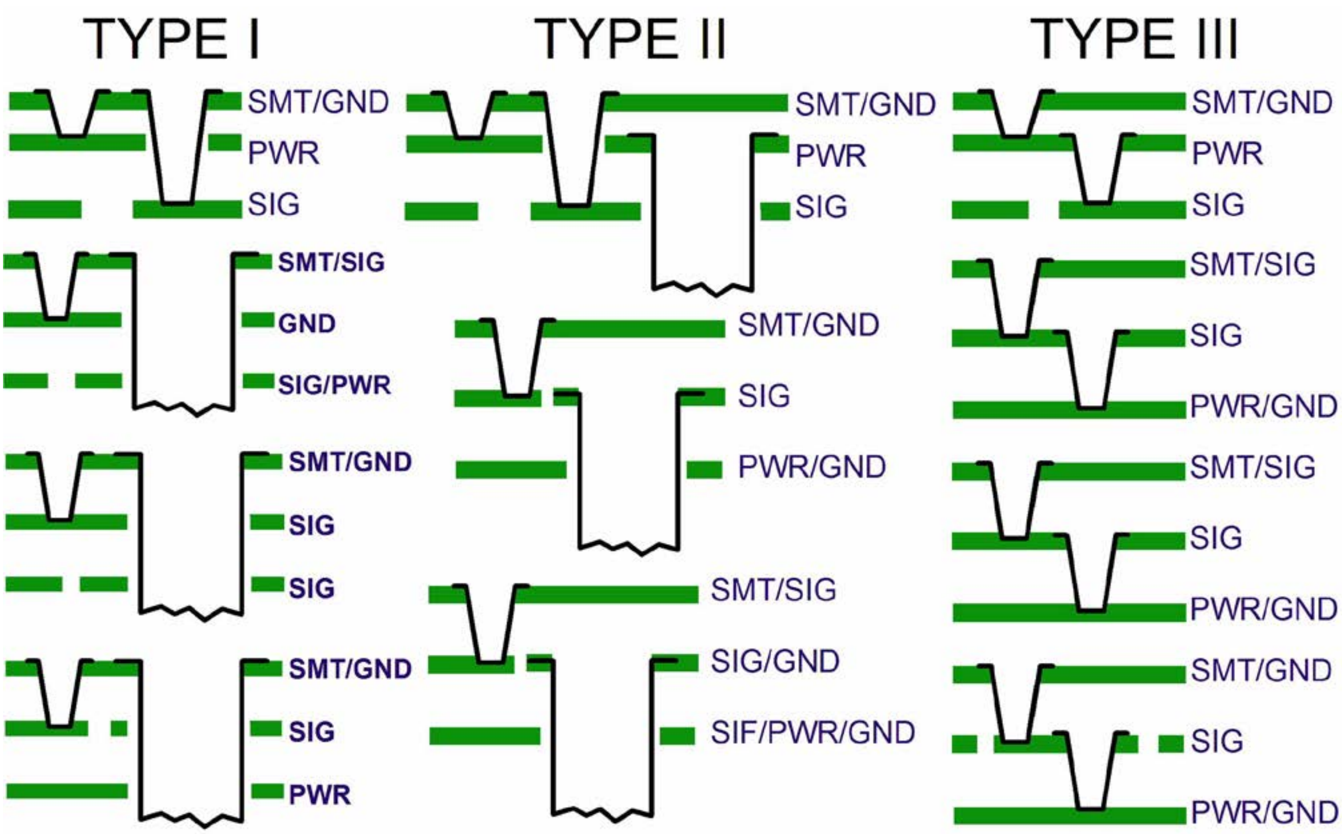


Figure 3: Various layer assignments available when using HDI and microvias. The goal is to remove as many TH as possible to free up routing space on the innerlayers.

ently. In theory, take a 1153 pin (34x34) BGA. It will have 132 possible routing escapes per layer (one trace between vias) plus 20 traces in the channel (five traces). This means that eight layers would be required (plus five plane layers) to connect this BGA to the rest of the circuit. The TH vias create a "fence" that makes routing very layer- intensive.

If we create more routing channels on the innerlayers by placing the blind vias on the surface, we connect more traces per layer and reduce the total layers. Channel routing uses blind microvias to form four or more additional cross-shaped, L-shaped or diagonal channels in a BGA fanout pattern. These new channels allow up to 48 extra connections per layers for this BGA (8x6 traces). Four routing layers and four plane layers can be eliminated in this example.

In some cases, the channel is not to escape the inner-pins of a BGA but to allow access to an adjacent BGA. The blind vias can be via-in-pad, near-via-in-pad or traditional dogbones. If working with a FPGA where pin swapping is possible, then the channels should be assigned to ground and power first.

Contribution of New SMT Connectors

Press-fit connectors require the use of through-holes. For thick boards, this might necessitate the use of back-drilling (Figure 4a) to reduce the inductance of these vias. Because of the sensitivity of high-speed circuits to parasitic inductance, even SMT connections might require their through-holes to be reduced to blind-via stubs (Figure 4b). But by using microvias, either in pad or off-pad, the need for larger through-holes is reduced as well as the resulting parasitic inductance, as seen in Figure 4c. Figure 5 shows the reduction in overall insertion loss due to the use of BGA connectors and blind-microvias instead of through-holes. If BGA connectors are used on the backplane or midplane, a 33% reduction is possible. If blind-microvias are used, then a 67% reduction can be realized. This also facilitates higher-density routing and fewer signal layers and their reference layers.

High-frequency, controlled-impedance SMT matrix-connectors are now becoming available. These are BGA types. Typical is the header for a backplane or midplane daughter card. These are remarkable for helping to reduce the thickness of multilayers.

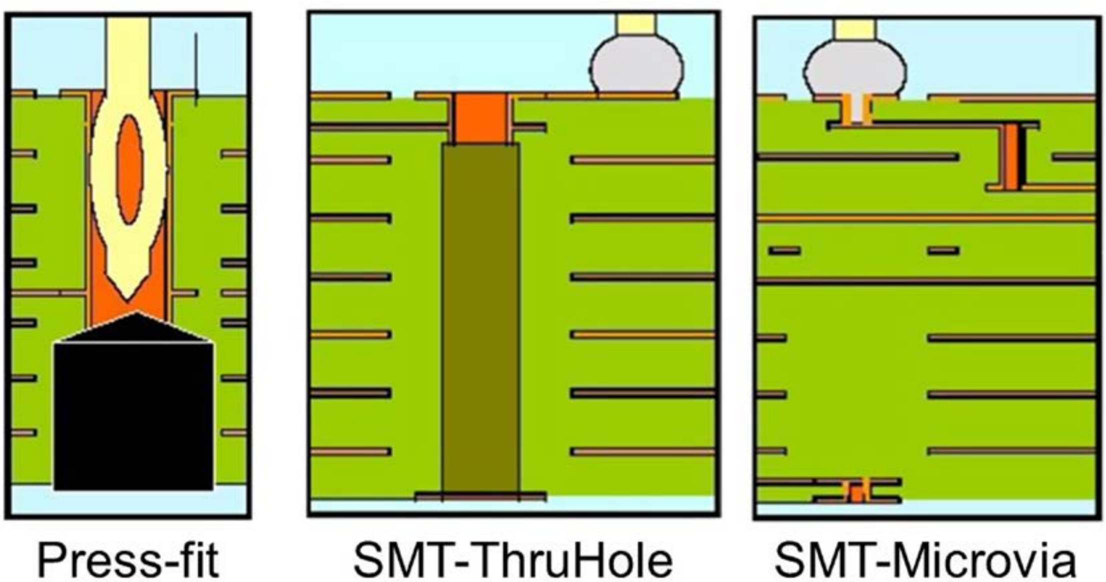


Figure 4: Press-fit connectors create a need for thick boards that require higher reflow temperatures and durations. (a) Many times, the increased inductance require backdrilling. (b) Even with surface-mounting, the through-hole plating may have to be eliminated. (c) Microvias increase density, reduce thickness and reduce inductance [5].

The Role of Reliable Blind Vias

At the end of the day, one must develop core competencies at the fabrication side of the supply chain, for the process chemistry side. Keeping in mind one is ultimately working to build long-term reliability in the printed wiring board. While many of those competencies have been discussed in this paper, it would be wise to expound on the critical success factors and process competencies required to build reliaibility into the microvia.

Key Processes

Several processes must be implemented in order to ensure success with blind vias and the overall goal of reducing the number of layers in the package. These are:

- Desmear
- Metalization
- Electrodeposition and via filling
- Half-etching process

This issue becomes increasingly complicated as HDI migrates into designs containing both through-holes and blind vias.

Desmear

Consider the need to ensure a clean and active capture pad and its importance on via reliability. Any residue remains on the capture pad will at the very least impact plating adhesion (Figure 6).

The residues could be from incomplete ablation with the laser or inadequate performance from the desmear chemistry (either alkaline permanganate or plasma). It is wise to ensure that the alkaline permanganate (if used) must be optimzed for the type of resin in the particular HDI build-up. Care must be talken to avoid aggressive attack of the resin at the interface of the via wall and capture pad.

When processing resin materials that formulated for lead-free assembly, the engineer must be cognizant of the fact that these Pb-free designed resins are more resistant to alkaline permanganate chemistry than the lower Tg resins. It would be wise to consider alternative desmear protocols such as combinations of plasma desmear and alkaline permanganate. A second options is to use newer generation solvent swell chemistry, which is better designed to effect penetration into the resin-polymer matrix.

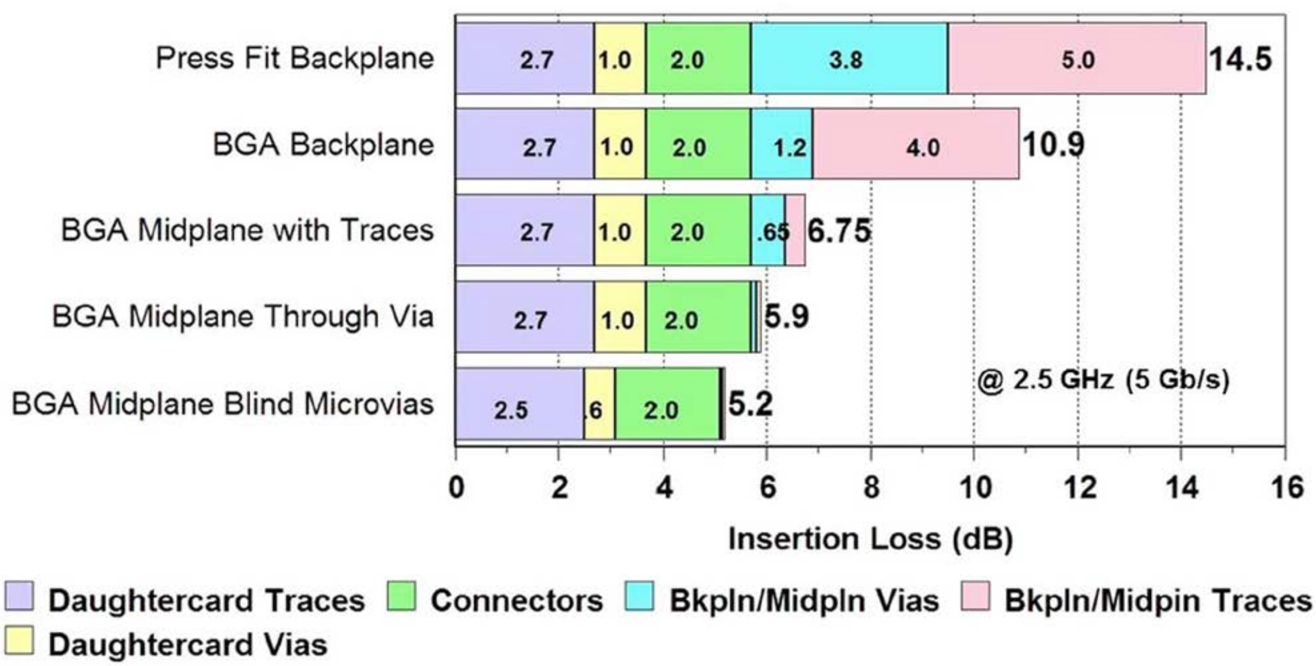


Figure 5: Total insertion loss from backplane-daughter cards' architecture from various contributors like traces, connector and vias[6].

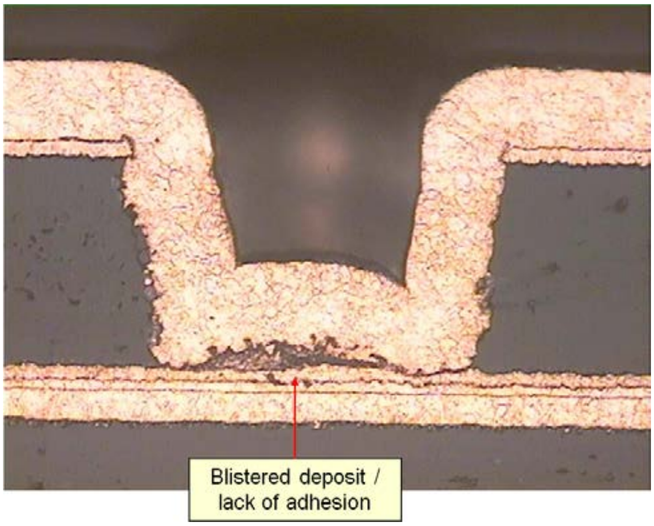


Figure 6: Debris on capture pad preventing adhesion of plated copper.

Metalization

After the desmear process, the task now is to insure a continuous, conductive and void-free deposit on the via walls and capture pad. Today, there are several processes that can be utilized to render vias conductive, including:

- Conventional electroless copper
- Palladium based direct metallization
- Graphite
- Carbon black
- Conductive polymer

These metalization processes (also known collectively as "making holes conductive" or MHC) are well developed for both plated through-hole and blind-via metallization. Direct metalization in particular is applicable to horizontal processing, although vertical systems can also be used. These processes typically involve the deposition of a conductive coating (palladium, conductive polymer, graphite, carbon black). This step is then followed by electrolytic copper. Thus, the actual electroless copper step is eliminated.

These processes have been presented and thoroughly discussed elsewhere[7], while direct metalization processes may reach certain limitations for use with very high-aspect ratio rigid circuit boards, these processes are highly efficient and effective for HDI. Direct metalization systems primarily function by coating the substrate, as opposed to a true chemical reaction type process such as electroless copper. Contrarians of direct metalization point to sheet resistance measurements of the direct metalization coatings versus electroless copper. Yet while the DM films are somewhat less conducitve, most of the DM processess have resistances in the neighborhood of 5–25 ohms square. This is more than sufficient to promote electroplating propagation in blind vias and mid- to high-aspect ratio plated through-holes.

Another advantage that DM processess have over conventional electroless copper is the ability of these DM films to render higher-performance material conductive without overly aggressive desmear tactics. It is well known that electroless copper requires sufficient roughening of the resin to promote palladium adsorption and to ensure adhesion of the subsequent copper deposit. However, most direct metalization processess require only minimal resin roughening to promote adhesion. This is because the more popular systems commercially available today rely on coating technology. And with the use of special polymers, these DM materials bond and adhere to a wide variety of resin materials with relative ease[8].

Another critical advantage of direct metalization is the ability to conveyorize the system. Of course this is possible with conventional electroless copper. However, the capital outlay for horizontal electroelss copper equipement that can match the productivity of most direct metalization systems is considerably greater. This is particularly evident when a fabricator is processing HDI designs that require multiple sublamination steps. If each HDI layer must be metalized, direct metalization offers a much faster and more effective means to achiev ethe productivity required.

Electrodeposition of Copper

After the vias are rendered conductive, the subsequent acid copper depostion step is required to further enhance the conductvity of the vias and to build reliability into the package. With respect to HDI and blind vias, the fabricator has two plating options available. The first involves what is known as conformal plating (Figure 7). The second option is known as superfilling of the vias with electroplated copper (Figure 8). In the former, the plated copper simply conforms to the via wall and capture pad. Ideally, one strives to minimize any overplating on the surface while ensuring good throwing power into the blind via. When HDI designs require via stacking, generally complete filling of the blind via is indicated. Even if there are no stacked vias, it is usually necessary to completely fill the blind vias either with copper plate or a via fill plugging paste[9]. Copper is more thermally conductive than these polymeric pastes and thus provides an excellent means to transfer heat through the package. There are several other reasons to superfill blind vias. These are:

- To increase the density and frequency for PCB
- To minimize signal delays and avoid effects of electron migration
- To make a smooth surface layer and avoid indentations
- To enhance the I/O number of package substrates
- To avoid incomplete fill of microvia hole filled by dielectric or conductive materials
- To solve the differences in coefficient of expansion of metal and resin
- To improve fine line design, via-on-via and interconnect reliability

As high-density designs depend on the maintenance of of fine lines and spaces, concern arises over the loss of circuit conformity due to overetching of the circuit pattern. One way to prevent this situation is to minimize plated copper on the surface while enhancing throwing power into the via. This can be accomplished with either DC (direct current) or PPR (periodic reverse plating).

However, with recent developments in new pulse plating rectifiers, special organic addition agents and analytical control methods, PPR plating is becoming the method of choice for HDI. PPR plating tends to produce better throw into small holes and blind vias at higher current density than is practical with DC plating. As with DC, the current density used may need to be reduced as the work becomes more difficult, but there is usually a significant advantage for PPR, particularly when plating very small blind vias (e.g., less than 6 mil/150 micron diameter). PPR with proper plating parameters is able to increase the plating thickness in blind vias and high aspect ratio through-holes while helping to reduce the plated thickness on the surface. This aids in reducing undercut of the fine circuit traces during the etching operation. For maximum advantage in throw, the current density, pulse waveform and brightener concentration used should be optimized for the individual application, but "middle ground parameters" can often be found where most types of work will give acceptable results.

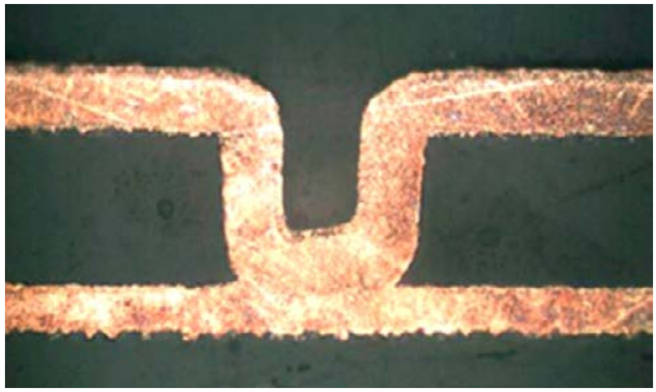


Figure 7: Example of conformal acid copper plating in a blind via.

Superfilling of Blind Vias

While a conformal copper plating technique works well for blind via HDI applications, many fabricators have migrated towards the superfilling of the blind vias. This is especially useful if stacked via designs are employed.

This type of design is benefical in that the designer gains significant routing space and increased wiring density. A key requirement of superfilling or bottom-up filling as it is often referred to is to deposit copper at a faster rate from the bottom, as opposed to the surface. This is referred to as the RDR or relative deposition ratio. A critical aspect of this process is the interaction of the various components of the organic addition agent. In this scenario, the brightener componet of the additive package se-

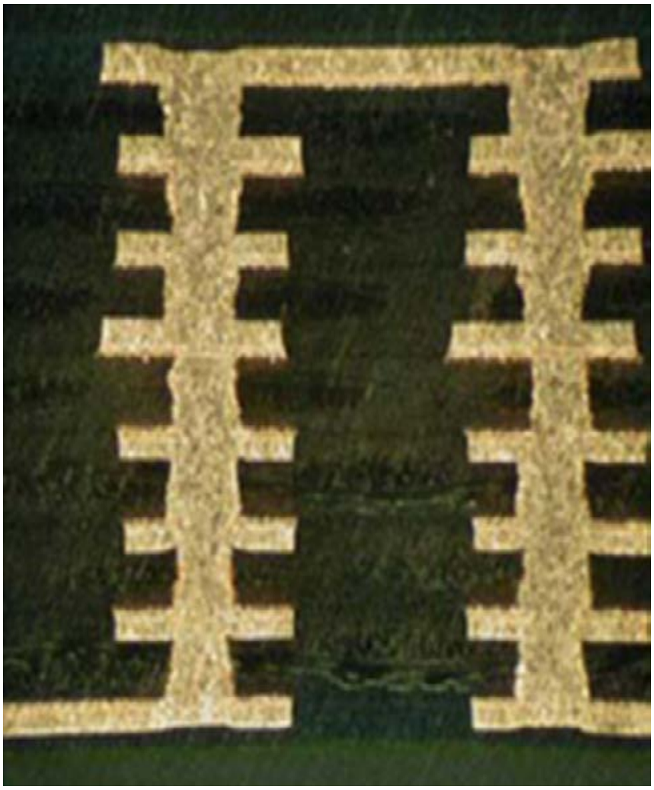


Figure 8: Superfilled and stacked vias.

lectively accerlates the deposition of the copper from the bottom, up, while the carrier and leveler componets of the addition agent package work to minimize overplating on the surface. Certainly, other parameters play a role in this as well. Generally, higher copper/lower acid ratios of the electrolyte benefit bottom-up filling, as does direct impingement solution movement as opposed to air agitiation. Secondly, several fabricators have enjoyed improved RDR results by using a dual step DC plating current density. As an example, plate the first 45 minutes of the cycle at 10–12 amps per suqare foot (ASF), then ramp up to 20–25 ASF[9].

Filling Blind Vias and Through Holes with Non-conductive Materials

OEMs and circuit board designers are also driving the use of via filling polymeric materials for blind, buried and in some cases through-holes. In addition, these formulations are of a non-conductive nature that provides a high quality plugged via, and is also cost effective. The requirements for these non-coductive via filling paste materials are:

- Good adhesion between copper and paste even under temperature influences
- Good adhesion of copper, dielectrics or photo resist
- Solvent free, one pack system
- No air inclusions in the paste
- g > 140 °C
- CTE < 40 ppm (below T_g)
- No shrinkage during curing
- Easily planarized

A 100% solids content of the paste material with the thermally cross-linkable epoxy resin and specially designed ceramic fillers ensures a low coefficient of thermal expansion. Interestingly, the coefficient of thermal expansion must remain in the 40–60 ppm range in order to ensure that no cracking occur in the filled via. In addition, it is critical that Z-axis expansion be minimized in order to prevent the plated cap from lifting (Figure 10).

Half-etching

Part and parcel to implemenation of HDI manufacturing is the ability to provide finer lines and spaces. The issue here is that when subtractive etching is employed to define the circuitry, there is a signifcant risk of excessive undercut and loss of line width. Again this is

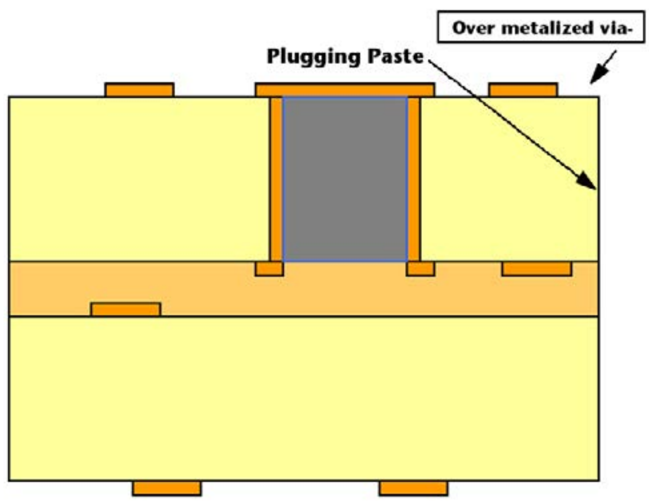


Figure 9: Via-in-pad overmetalized and filled via.

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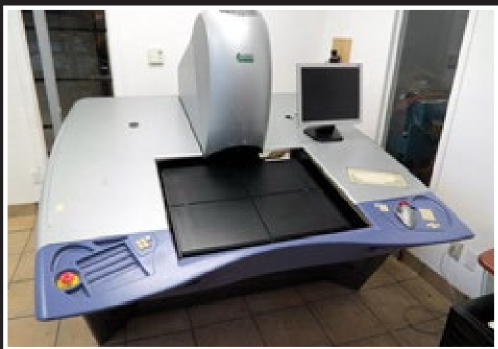


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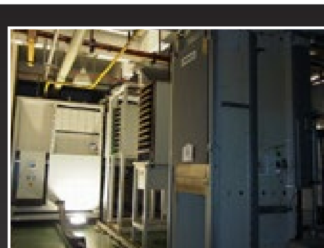

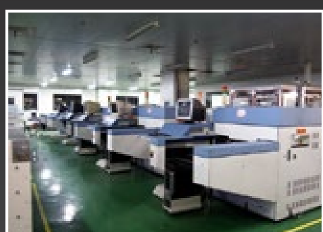


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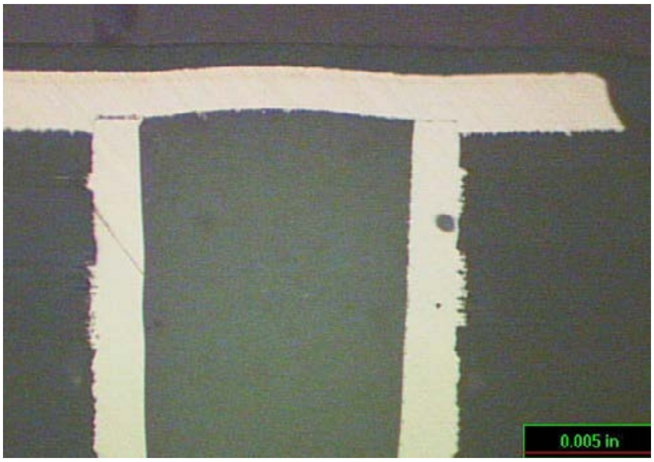

Figure 10: Excessive CTE leading to plated copper lifting from filled via.

all about the drive to sub 35 micron lines and spaces. And the half-etch process is one way to achieve this goal. The basic concept of half-etch is to remove a set amount of copper from the surface in as uniform a fashion as possible. By etching the copper foil down to a lower thickness, the etch factor and resulting undercut is greatly reduced. Consequently, minimal copper is lost from the circuit trace. To insure this operation is successful, both chemistry and equipment configuration designs are critical. First and foremost, etching chemistry should etch down in the Z-axis as fast as possible. Secondly the etching equipment must be designed to move the solution across the copper foils uniformly. By reducing for example 1 ounce copper foil (35 microns) down to ½ ounce or ¼ ounce, one maintains the adhesion of the original foil. In addition, the fabricator is presented with a much thinner substrate foil that can be easily etched during the final etch process. There are several good reasons for this approach:

- Minimize undercut and increase fine line yields
- Ease of handling as opposed to working with ultra thin copper foils
- Adhesion of the half-etched foil is usually greater than the adhesion of the ultra thin foil to the resin materials as well as the plated copper in the SAP (semi-additive process)

With respect to the half-etch process, the etching chemistry should be designed to remove the copper in a controlled fashion, imparting minimal roughness to the remaining copper. This author has found that the desired etch rate on the copper foil (whether HTE or ED foil) for the half-etch process is 0.10–0.25 microns per second (4–10 µin per second or 240–600 µin per minute). One can achieve higher etch rates if desired. However, there needs to be a balance between chemical consumption, etch equipment compatibility and overall process control. Removing copper too fast could cause the heat to rise in the etching chamber. In addition, it is beneficial to process the innerlayer foils through an acidic cleaner that will remove chromate and mild soils prior to actually etching the copper. This helps to ensure a clean virgin copper surface that permits the etching chemistry to remove copper uniformly.

Example of Telecom Redesign

A major telecommunication company recently experimented with this concept. They took a recent 22-layer, TH optical-input board (0.127" thick) and redesigned it to a 14-layer HDI board of 0.063" thickness (1+12+1), without moving or changing any part locations. Figure 9 shows the old 22-layer stackup compared to the new 14-layer HDI stackup. The boards were 8.50" by 14.34" with 702 parts (mostly BGAs and actives), having 8,759 pins on the PRI side and 2,036 parts (mostly passives) having 4,206 pins on the SEC side. There were orignally 12,610 drilled TH in the original version, but only 3,887 in the HDI version; the rest were laser-drilled microvias.

Conclusion

One of the more difficult type of multilayer to get to accept a lead-free assembly process is the thick, high-layer count PCB with through-hole parts and multiple PWR/GND planes. HDI techniques can help in the reduction of thickness and number of layers for these types of boards, resulting in thinner multilayers, but also reducing the costs by 50% and improving the high-frequency performance and reliability. Further, the fabricator can enhance the overall relaibility and manufacturability of

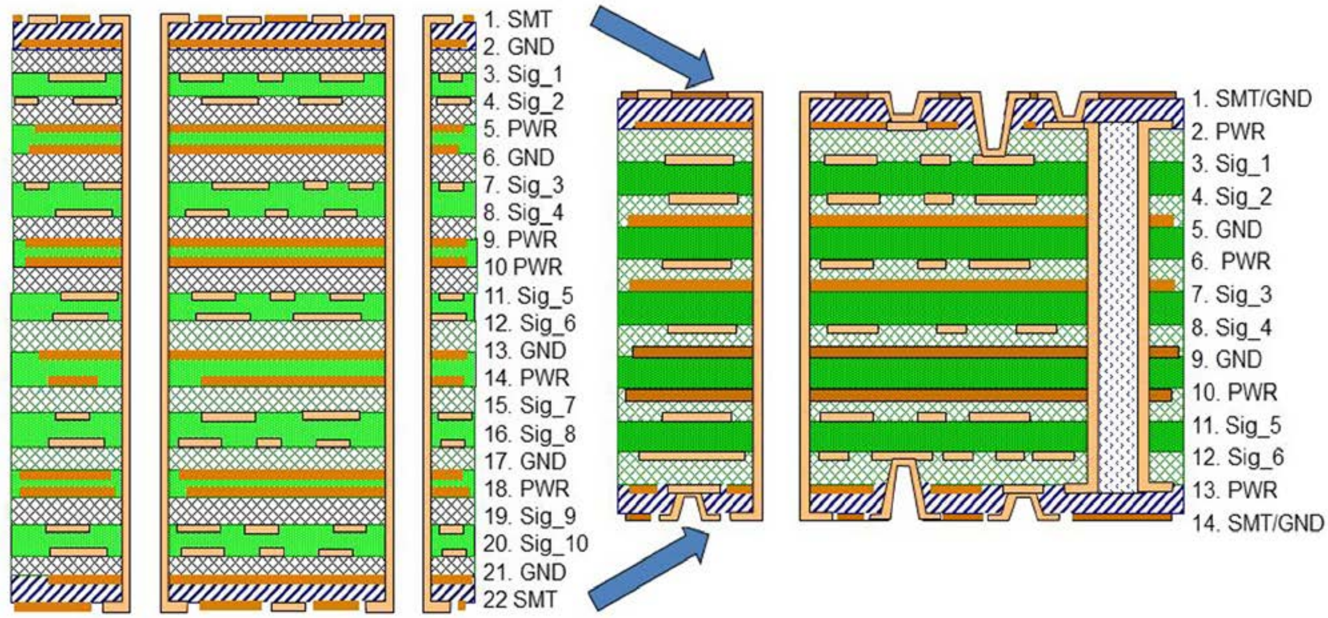

Figure 11: Conversion of a 22-layer TH multilayer to a 14-layer HDI (1+12+1) in order to reduce its thickness from 0.127" to 0.063" to gain reliability in LF SMT assembly.

HDI substrates by adopting direct metalizaton and new technologies in electroplating such as copper super fill and periodic reverse copper plating (PPR). These processess aid in building reliability into the vias that lead-free assembly requires. **PCB**

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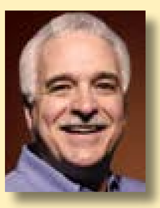
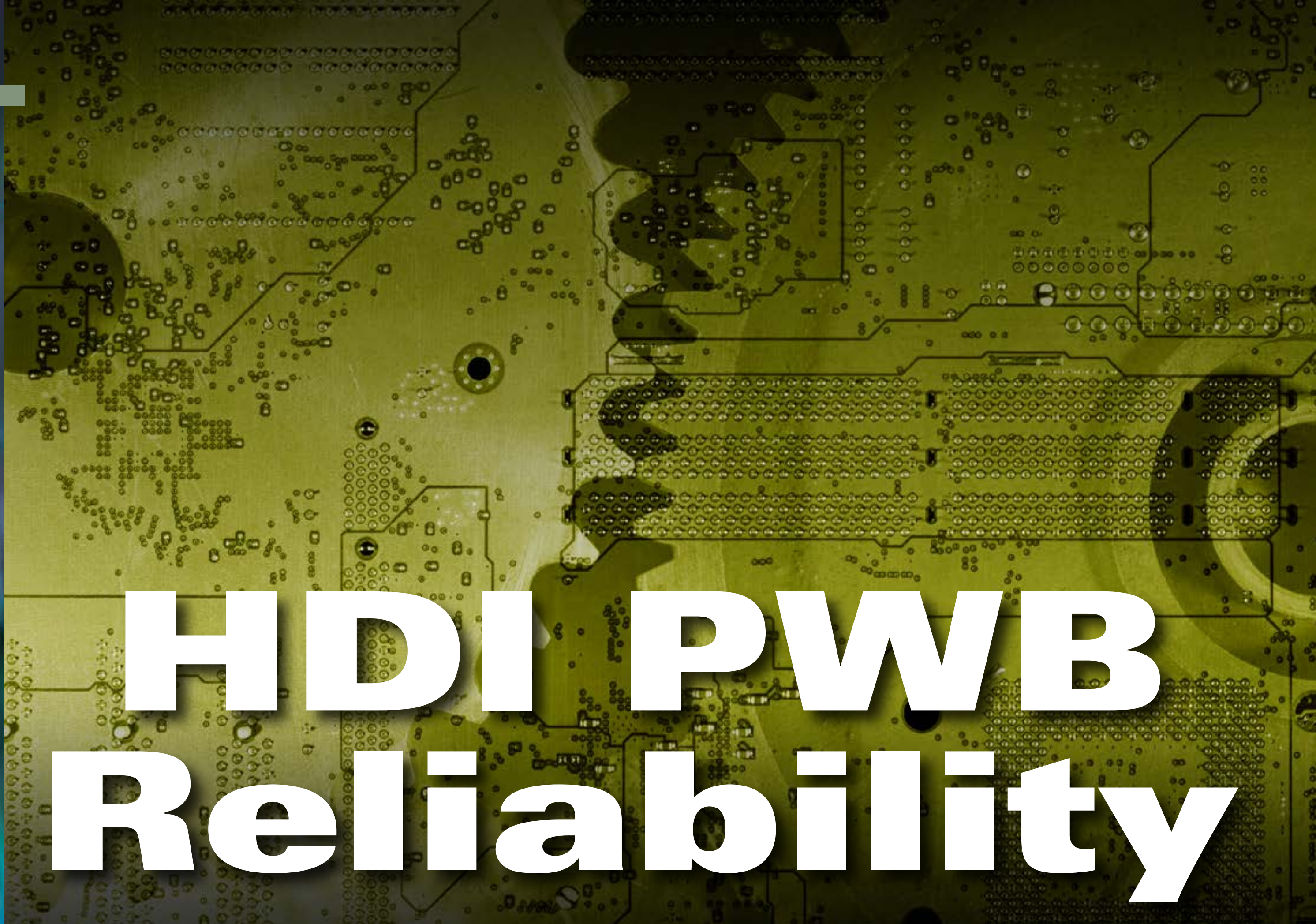


Michael Carano is with OMG Electronic Chemicals, a developer and provider of processes and materials for the electronics industry supply chain and regular columnist for The PCB Magazine. To contact Carano, click here.



FEATURE

HDI PWB Reliability

by Paul Reid

An HDI PWB may be defined as a PWB with a higher wiring density per unit area than conventional PWB. They have smaller lines and spaces, smaller vias and capture pads and higher connection pad density than employed in conventional PWB technology. HDI PWBs utilize microvias, buried vias and sequential lamination with insulation materials and conductor wiring for higher density of routing. HDI PWB is an alternative to high layer-count and standard laminate or sequentially laminated boards.

HDI PWBs are characterized by high-density attributes including laser microvias, fine lines, smaller grid sizes and high performance thin materials. This increased density enables more functionality per unit area. Higher technology HDI PWBs have multiple layers of copper-filled, stacked microvias, which create a structure that enables even more complex interconnections. These very complex structures provide the necessary routing solutions for today's large pin-count chips utilized in mobile devices and other high technology products.

When it comes to HDI reliability of PWBs, what we must do is consider two parts: the copper interconnects and the base material. What one can do is test the reliability with thermal cycling using Interconnect Stress Test (IST) coupons. The IST coupon tests the copper interconnection and checks for material damage. The coupon is fabricated on the production panel with the PWBs and has all the attributes of the PWB. So the coupon has the same construction, copper weights, hole sizes, grid sizes, and copper plating as is found in the corresponding board. The test thermal cycles the IST coupon, for typically 500 cycles, or until the coupon fails with a 10% increase in resistance due to cracks that develop in copper interconnections as a result of thermal cycling.

By measuring capacitance change between ground planes we can determine if there is any significant material damage in the coupon. What one does is to measure the capacitance in picofarads between adjacent ground planes be-

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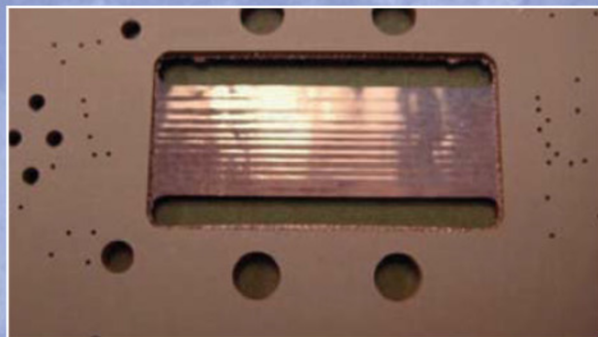

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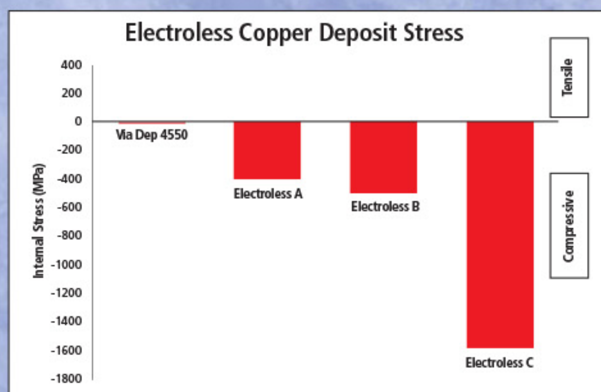

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fore testing (to establish a base line), after preconditioning (a simulation of assembly and rework) and at the end of test. We then compare the measurement after preconditioning and at the end of test to those original readings. A -4% change or greater indicates significant material damage and a cross section is processed to confirm or refute this finding.

The major problem is the implementation of lead-free soldering that requires assembly temperatures of 260°C. The FR-4 material is at its limit to withstand the heat when exposed to 260°C. The Z-axis expansion is at its highest at this temperature, putting extra strain on the copper interconnects.

The most common type of failure of a robust interconnection is a barrel crack that occurs in the central zone of the plated through hole (PTH). When tested using thermal cycling to 150°C, this is a wear-out type of failure that happens over hundreds of cycles (500+ cycles). Surviving 500 cycles without any significant increase in resistance is considered a robust coupon.

In a weak coupon, the failure before 350 cycles may relate to a process problem, with the most common problem being thin copper plating. With thin plating, the barrel cracks may still be the cause the failure but it would be failing in less than 350 cycles. The PTH may also fail for corner cracks or interconnection separation.

Weak buried vias fail typically for barrel cracks in the center zone of the structure simi-

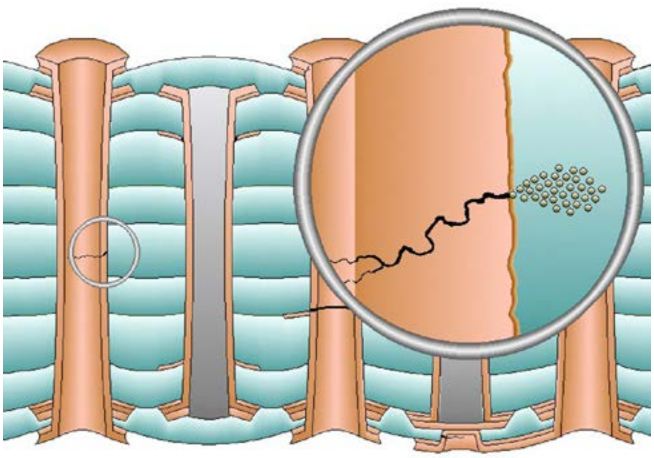

Figure 1: Barrel crack due to metal fatigue.

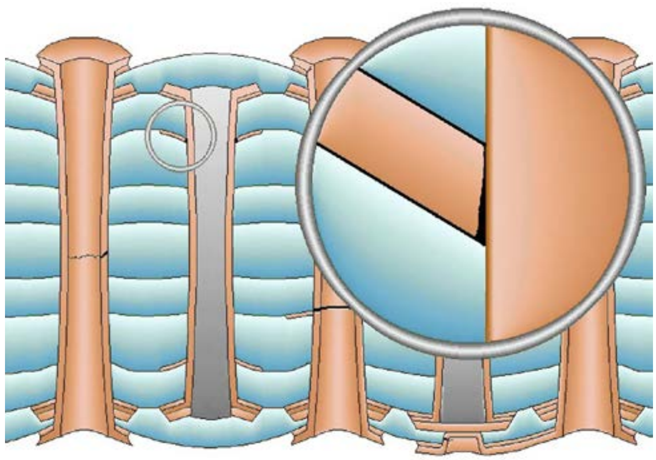

Figure 2: Interconnect separation.

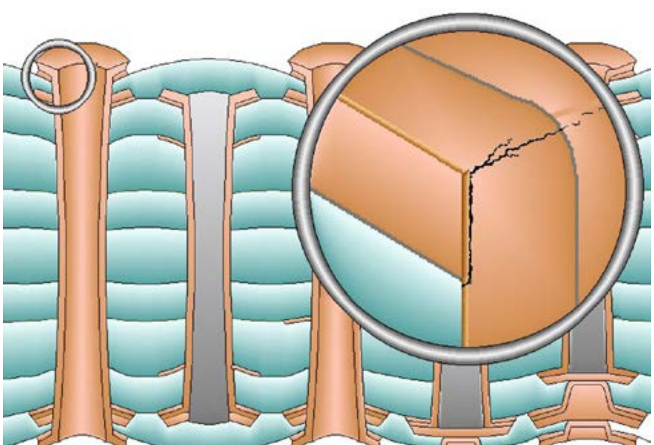

Figure 3: Corner or knee crack.

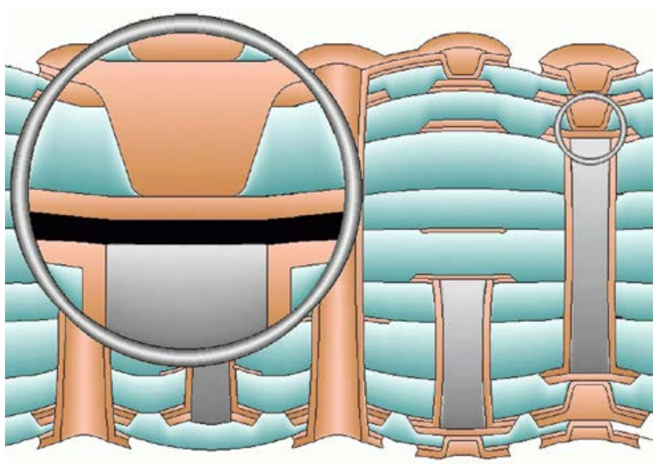

Figure 4: Lifted copper cap on buried via.

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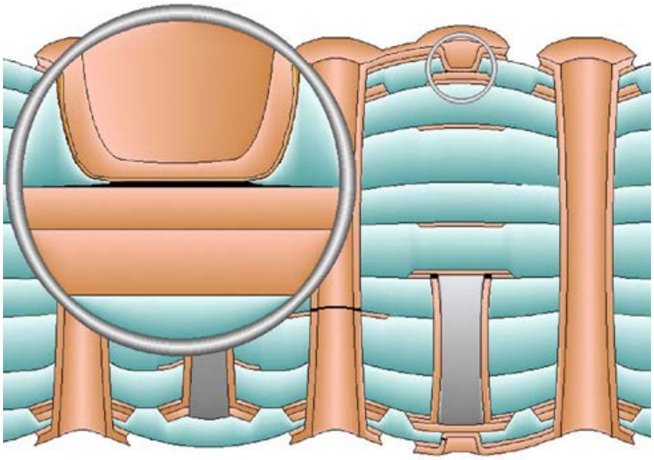

Figure 5: Microvia separation.

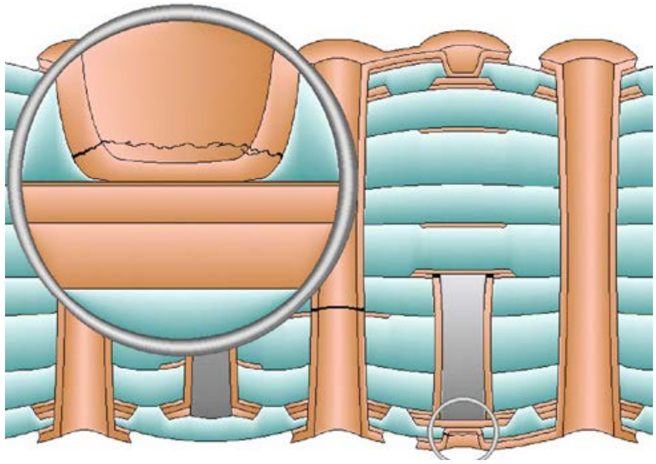

Figure 6: Microvia barrel crack.

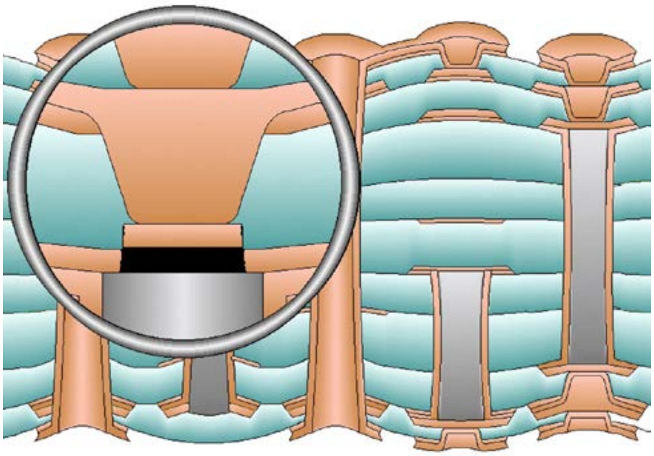

Figure 7: Microvia pull out failure.

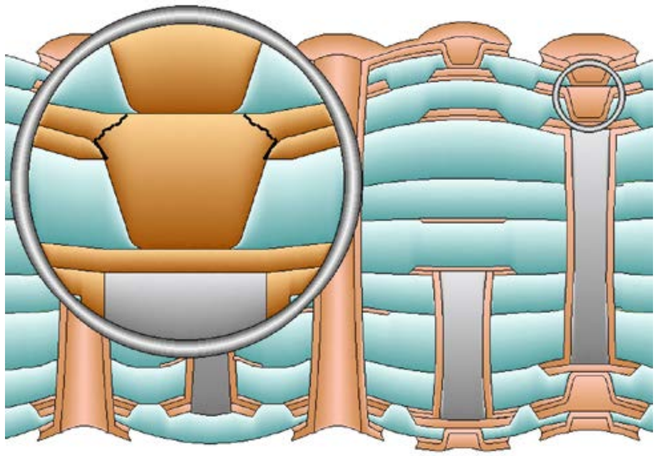

Figure 8: Microvia corner crack.

lar to PTHs and, less often, for corner crack or interconnect separation. One of the HDI structures includes microvias stacked on buried vias. In order to have a microvia stacked on top of the buried via what we have to have is a conductive cap on the top of the buried via, which can also fail. There may be a separation of the copper cap from the top of the buried via or a crack in the cap of the buried via (Figure 7).

Microvias are typically the most robust type of interconnection. Because of their robustness they are tested at 190°C. When tested at 190°C robust microvias will survive 500 cycles while weak microvias will fail before 500 cycles. The most common cause of microvia failure is a separation between the base of the microvia and the target pad. The second most common cause of microvia failure is a barrel crack toward the base of the microvia. Other failure modes include corner cracks (seen in copper-filled microvias) and pull out types of failures where the target pad cracks around the base of the microvia.

In HDI PWBs one must also consider construction. One may produce multiple microvias structures as either stacked or staggered. Microvias that are stacked are about four times more vulnerable to failure than the same structure in which the microvias are staggered. Well fabricated one- and two-layer microvias do not usually fail prematurely. Three- and four-stacked microvias tend to fail before 500 cycles when tested at 190°C and are a fabrication challenge.

The material damage is monitored in an IST coupon by measuring changes in capacitance between ground layers in the coupon. First, measure the capacitance between two flooded ground planes in the coupons in the as-received state and then again after the coupon has undergone preconditioning, and at the end of test. If there is significant material damage then a -4% or greater drop in capacitance is seen. To confirm the drop in capacitance is indicative of material damage, one or two of the coupons are subjected to a microsection to check for the presence of material damage.

The major types of material damage found are adhesive delamination, cohesive cracks, and crazing. Adhesive delamination is typically between two laminated surfaces like the b-stage, c-stage and copper interfaces. On occasion, adhesive delamination is seen between the glass bundles as a group and epoxy of the dielectric. This type of failure is found typically on a 1 mm (.040") grid or greater.

The most common type of material damage is the cohesive crack, which is a crack that goes through the b-stage, c-stage and glass bundles. The cohesive failure is a breakdown of the epoxy system due to high temperatures of assembly. This type of failure is found typically on a 0.8 mm (.032") grid.

Crazing is the separation between glass fibers and the epoxy system. It looks like silver sheen on the glass bundles due to an envelope of air around the glass fiber. Crazing provides a pathway for conductive anodic filament (CAF) formation. This type of failure is found typically on a 0.5 mm (.020") grid.

In conclusion, the use of HDI PWB reliability in lead-free applications is a dual-edged sword. The copper interconnections are more prone to a breakdown and the material is more prone

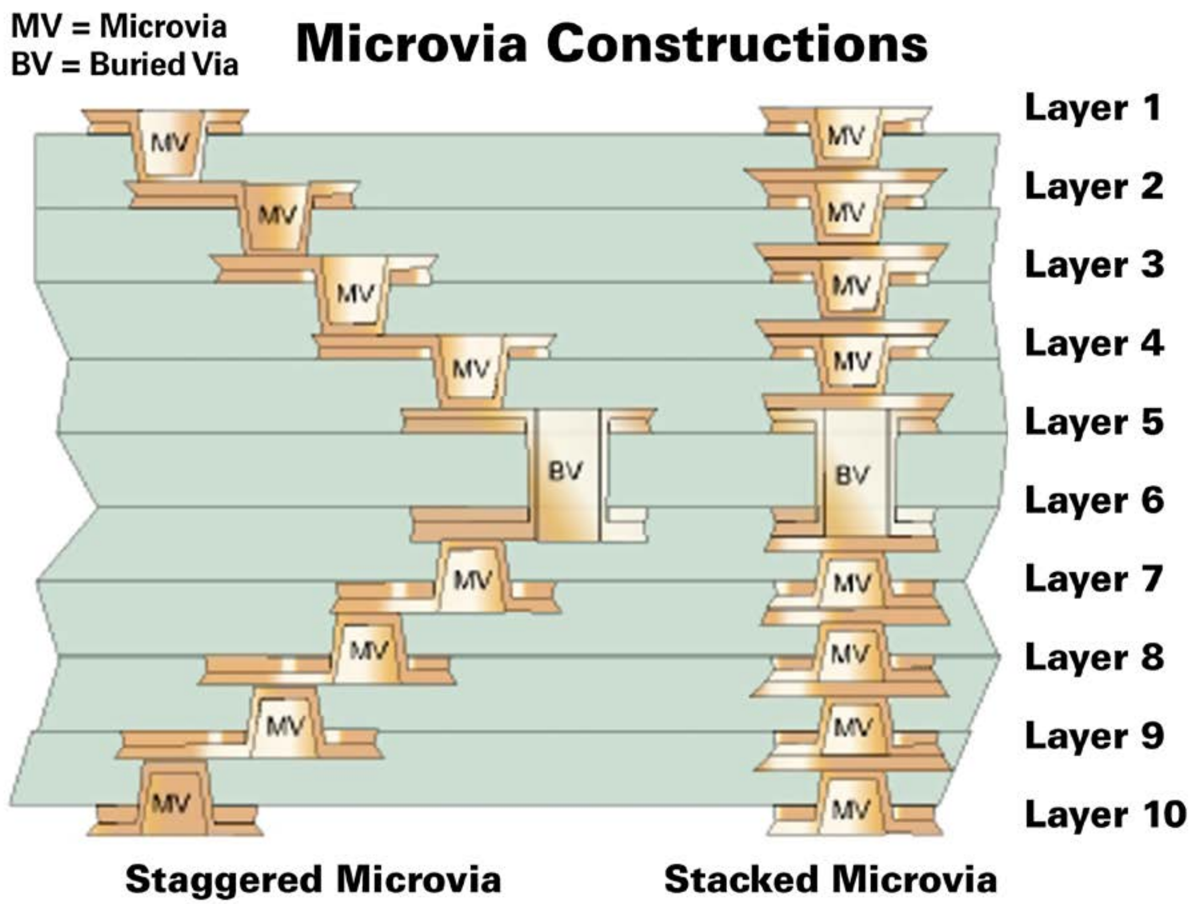

Figure 9: Staggered vs. stacked microvias.

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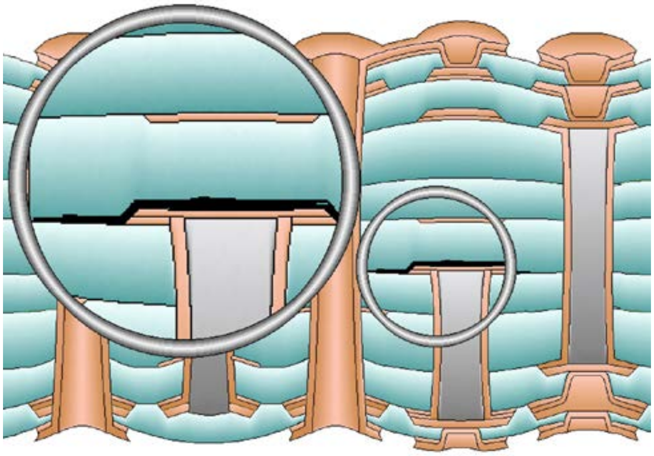


Figure 10: Adhesive delamination.

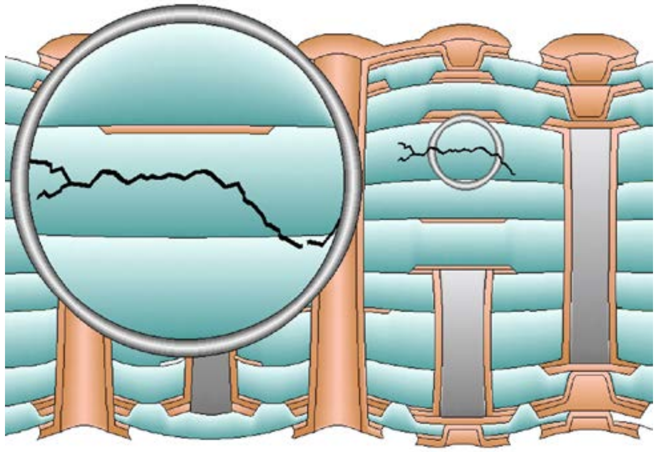


Figure 11: Cohesive crack.

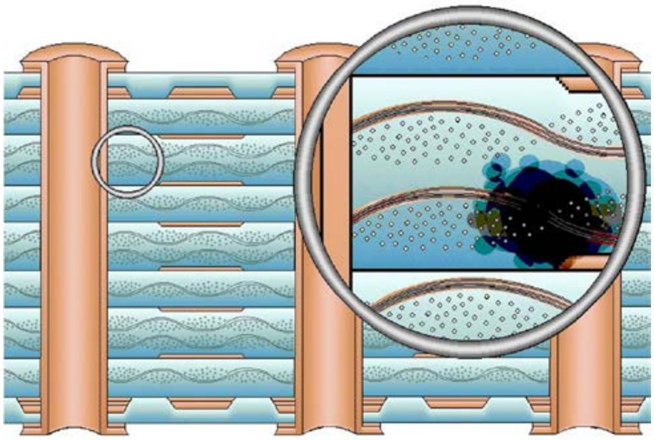


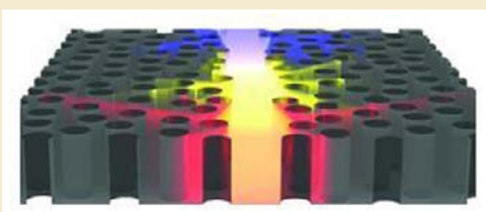
Figure 12: Crazing with a CAF failure.

to damage. That is not to say that robust PWBs cannot be made, but there is a challenge in producing them. One must test the interconnect and the material in order to confirm robustness in a given application. **PCB**

Paul Reid's career in PCB fabrication and reliability testing spans 35 years. One of his specialties is producing technical animations of failure modes induced by thermal excursions, giving him insight into the mechanisms of circuit board failure. Reid is now retired. To contact the author, click here.

Unavoidable Disorder Used to Build Nanolaser

Researchers are working to develop optical chips, where light can be controlled with nanostructures to be used for future circuits based on photonics instead of electronics. But it has proved to be impossible to achieve perfect photonic nanostructures: They are inevitably a little bit imperfect.



Now researchers at the Niels Bohr Institute in collaboration with DTU have discovered that imperfect nanostructures can offer entirely new functionalities. They have shown that imperfect optical chips can be used to produce "nanolasers," which is an ultimately compact and energy-efficient light source. The results are published in the scientific journal Nature Nanotechnology.

The nanolaser is based on the disorder in the pattern of holes in the photonic crystal. The light source is built into the clear-as-glass photonic crystal, and light is reflected and channeled into the crystal's middle lane, then thrown back and forth. Due to imperfections is intensified and spontaneously turns into laser light.

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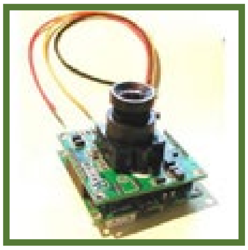

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From Single-Sided to HDI: *The "Three Phone Call Method" Works!*

by Dan Smith
RAYTHEON

One experiences both extreme joy and anxiety when watching a prototype PCB being powered up for the first time. The test bench surrounding the new board resembles an operating room, with probes attached everywhere to an array of oscilloscopes, multimeters, and other indicators. All eyes of the project team surrounding the test bench watch the darting eyes of the main electrical engineer, frantically reading each monitor/display for its analysis. More times than not, the silence is broken by this electrical engineer when he erupts with the exclamation, "Wow! The circuit works!"

To all PCB fabrication process engineers who are not present at that moment, but whose skills and knowledge base over the years have made those words possible, I want to begin by thanking you for all that you have done to advance the quality and integrity of the electronics industry. Your dedication to continue to fabricate high-quality boards and panels ever since Paul Eisler (the father of PCB fabrication) made his first radio with a PCB needs to be recognized by all in our industry.

In my first score of years in electronics, I had the good fortune of learning PCB fabrication in creating single and double-sided prototype boards as an R&D technician in a crude, but effective PCB fab lab. I learned first-hand about raw materials, photo-imaging, etching, plating and drilling by fabricating prototypes for new design concepts to address our customer's product needs. Although I was never able to add the soldermask or silkscreen layers to these boards because we only did the proof-of-concept, I did come to better understand the materials' characteristics and design challenges when I changed careers from being a technician to a PCB designer.

Early in my design career, every time I had the chance to tour a local fabrication shop, I would somehow find out who the main process engineer was, and then spend time with that person at the end of the tour. I would question him relentlessly about everything I saw that I did not understand. To my amazement, every fabrication process engineer understood my quest for knowledge, and succinctly answered every question about fabrication I posed to them. To this day, I cherish those meetings, and now share all of that information I have assimilated when I teach the PCB design process.

My favorite process engineer was someone I only interacted with via telephone, because the fabrication house that I sent my prototype designs to was more than 1,000 miles away.

We'll call this engineer Tom; his name is changed in this story only to protect him from future phone call bombardment. Tom came highly recommended by a program manager for which I designed prototype boards for more than six years.

In our initial conversation about the first prototype design I was about to send him (a six-layer multilayer design with just through-holes),

I meticulously explained all of the electrical and physical details of the board (e.g., multiple impedance needs, test coupons, milling challenges). I asked him to please get back to me at first convenience with a) a preferred layer stackup, and b) trace widths and spacings for the impedance trace groups for all involved signal layers. He ended this brain-dump of mine with both a compliment to my thoroughness and a question as to how I became so prepared in identifying all of these design needs. When I told him of my history in PCB fabrication, he again thanked me for being prepared to talk with him, and offered his time to answer any future fabrication technology question I had going forward. Two days later, Tom called me back with all of the fabrication information I needed for routing and documenting the design. During the next six weeks, I finished everything on the design, and after the final design review, I called Tom to tell him that we were about to send the fabrication build package to the shop. When Tom asked me if there were any deviations to what we discussed in the first phone call, I answered no; everything was exactly as per our first discussion.

When Tom's first prototypes arrived back to our team, they were tested unpopulated (continuity tested for potential shorts between power potentials), and then sent on to our in-building assembly shop. Less than a week later, the first fully populated board was received, and all of the verification probes and instruments were attached. Now came the very moment to power up the board. "Wow! The circuit works!"I said, feeling a huge rush of relief. I called Tom immediately and thanked him for supplying a great product.

The time finally came when our high pincount BGAs could no longer be successfully routed with just through-hole vias. My co-worker "Little Dave" attended an HDI workshop taught by Happy Holden (who I eventually partnered with on many HDI education collaborations), who brimmed with new design ideas to help us catch up to and stay ahead of the ever-changing interconnection technology challenges.

> *"You and I have developed a process where it only takes three phone calls to prepare me for fabricating your prototypes."*

When I found out I was to start working on my first HDI design the following week, I called Tom to ask him if he had ever fabricated HDI designs. When he said yes, he also said "We need to talk about this in detail." For the next 30 minutes, Tom did a brain-dump on me of designer "dos and don'ts" and the current costs associated with the complexity of fabricating HDI boards if we were going to continue to be successful. When I called him the following week regarding the first HDI design (an IPC HDI Type I) I was sending to his shop, I found myself using the very vocabulary that Tom had instilled in me the week before. After my usual litany of design details, he said, "Yes, I can fabricate that design for you. I look forward to seeing your design in our shop." That design, like all of the others I had sent him before, came back perfect.

As the design complexity grew into IPC-II and IPC-III HDI types, as well as other fabrication challenges, that first phone call to Tom about prototype designs always gave me the reassurance that with Tom as my number one and only fabricator, I truly had a fabrication partner.

One day, when I called Tom about another prototype that I was about to send him, he chuckled while asking me a question, "Should we just assume we'll use our three phone call method in this design, too?" Tom truly caught me off-guard, and I asked him to explain his whimsical humor.

He said, "You and I have developed a process where it only takes three phone calls to prepare me for fabricating your prototypes. Call one: You tell me what you need. Call two: I call you back and tell you what materials and stackups are required. Call three: The design is on the way. When I get your third phone call, I get your prototype immediately into our production schedule because there are no surprises between us." We both laughed that we had created a "virtual fabrication design process," but both realized it was based on fabrication process knowledge and complete respect for each other's expertise.

In my second score of my years in electronics,

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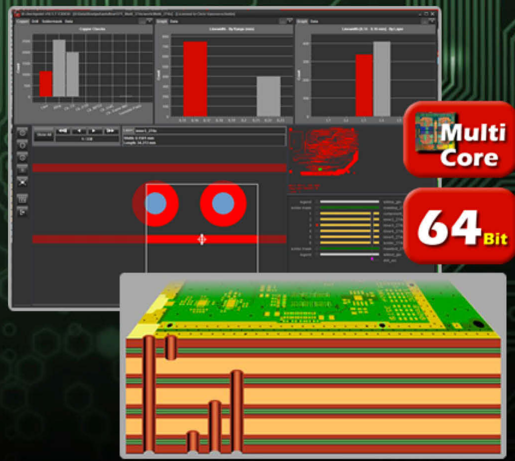

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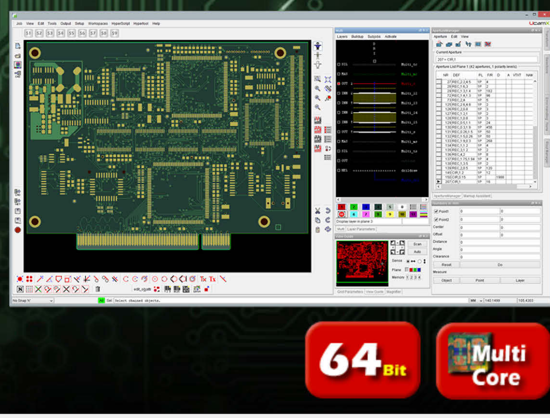

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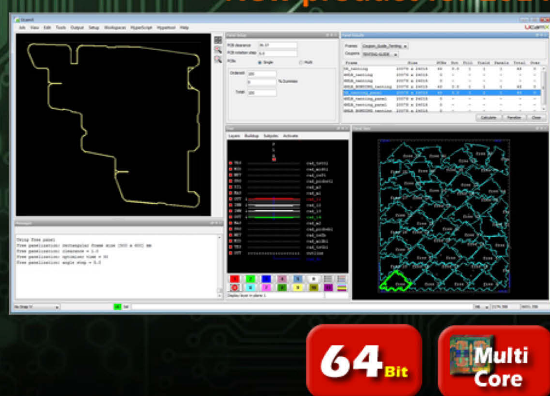

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I have advanced from creating PCB designs into the EDA tool world, but I have created software programs and other inventions based on those first years with my electronics industry mentors. When asked what I miss most about designing, more times than not, I say "I miss the three-phone-call method, because it always worked on every prototype design I was given.'"

I still believe in the process Tom and I co-developed. In this day and age where design information is just thrown over the wall from the design house to the fabrication house, I would be curious to hear if there are still human-to-human interactions, and if there are similar, and hopefully, better ideas on how both the design and fabrication community can, should, or do interact in reducing the overall time required in the concept-to-manufacturing electronics design process. Please feel free to contact me via e-mail.

In summary, thank you again to every fabrication process engineer who has contributed your time and knowledge to those of us who seek your expertise. Personally, I have been truly blessed and have grown by your collective wisdom. **PCB**

Daniel J. Smith is a principal technologist for Raytheon Missile Systems. He has taught multiple aspects of the PCB design process internationally, and he has authored several PCB-related patents, articles, and standards over the past 30+ years. To contact Smith, click here.

FEATURE VIDEO INTERVIEW

New Dimension in Pinless Multilayer Registration

by Real Time with...productronica 2013

At productronica 2013, I-Connect007 Technical Editor Pete Starkey caught up with Victor Lázaro Gallego, R&D manager at Chemplate Materials, S.L., to discuss the new pinless registration process from Chemplate. In Victor's words:

"The new development is called InduBond PLR (pinless registration). This machine simply measures every layer (front-to-back image registration and layer shape) and uses that information to align or register automatically, layer-to-layer during the multilayer building up process of the stackup. This machine guarantees the best fit possible of the layer-to-layer registration while compensating for any dimensional distortion caused by scaling, shrinkage or image registration. Once the layers are registered, the machine holds that relative position by using induction bonding technology. The machine has been developed in a modular way that allows it to be fully automated depending on the options."

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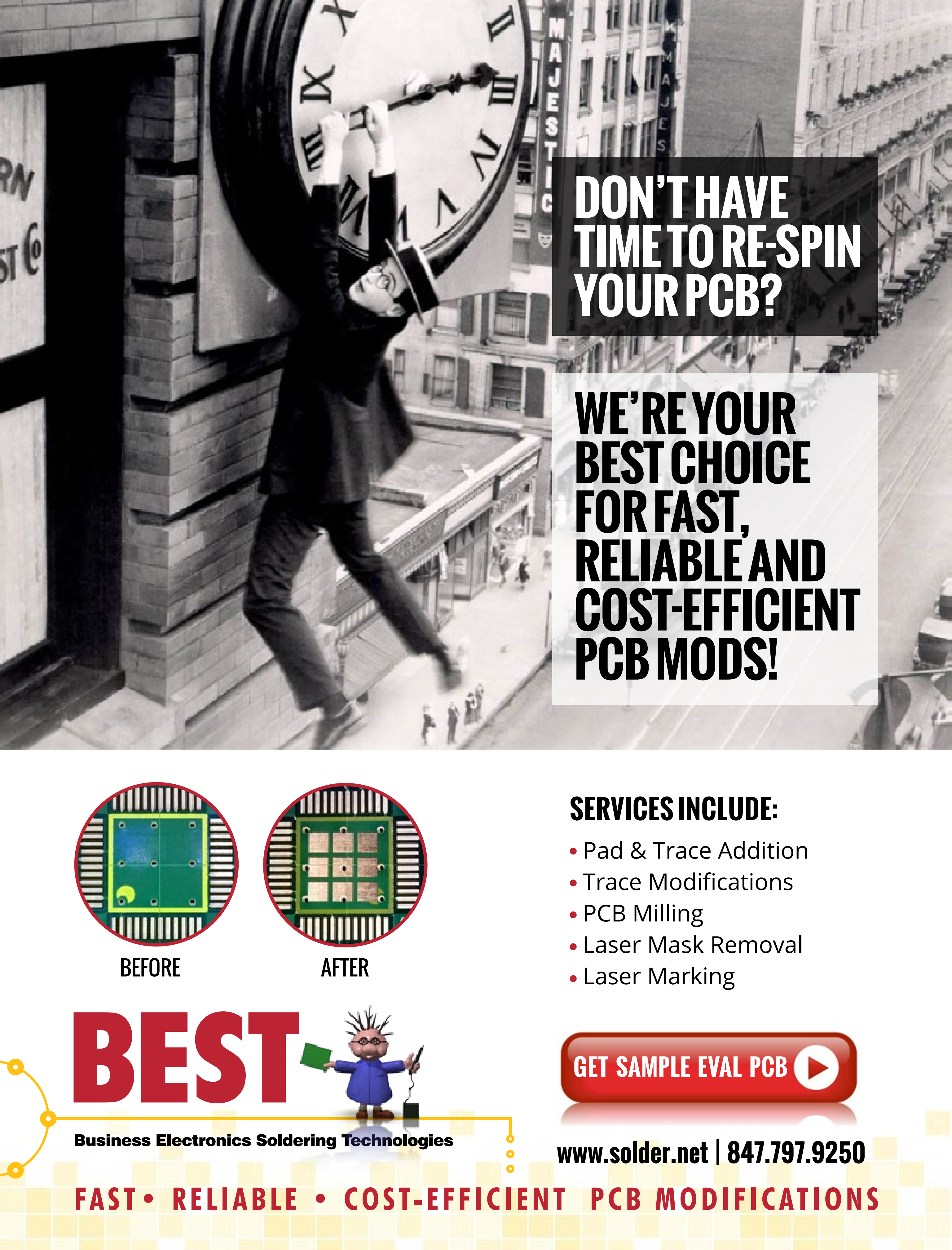
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IPC APEX EXPO 2014: The Opening Keynote Session

by Peter Starkey
I-CONNECT007 TECHNICAL EDITOR

Images contributed by Michael Weinhold

We will rock you! A grand Las Vegas opening to the 2014 IPC APEX EXPO included a spectacular show by dance troupe Speed of Life, complete with silver paint, angel wings, rollerblades and stilts. The approximately five-minute performance heralded the appearance of IPC President John Mitchell, who welcomed a packed house in the Mandalay Bay Convention Center, and declared the event's theme: New Ideas for New Horizons.

John Mitchell

Steve Pudles

Mitchell began by taking a few minutes to commend the success of the new IPC Validation Services initiative, and to present a certificate to IEC Electronics as the first company to be admitted to the Qualified Manufacturers Listing. After acknowledging the winners of the Best Technical Papers awards, Mitchell handed off to IPC Chairman Steve Pudles, who took the stage to introduce the keynote presenter, Dr. Peter Diamandis, co-founder and chairman of the X-Prize Foundation and co-founder of Singularity University.

Dr. Diamandis' provocative and inspirational presentation, "Creating a World of Abundance: Exponential Technologies Causing Disruptive Innovations," contained some sometimes frightening observations on the potential for future technology and other emerging market forces to dramatically influence living standards. Compared with human society's historical "local and linear" process of communication and development, where progress happened one step at a time, and the transfer of knowledge was limited by the distance a man could walk in a day, we are now in a world where progress is happening exponentially, and knowledge can be transferred anywhere in the world in a split second. He demonstrated how, in a company, these changes were accelerating disruptive stress—or disruptive opportunity depending on management's attitude to innovation. Agility is critically important. Companies commonly have experts who effectively block innovation by finding lots of ways an objective could not be achieved, and Dr. Diamandis despaired of organisations that start off with a mission and then back off because they decide it is too risky.

Nominating Kodak as the definitive example of a company worth billions that failed to recognise the disruptive opportunity presented by the digital camera in 1996—actually invented by one of its own people—and found itself overtaken by new technology and bankrupt in 2012, Dr. Diamandis noted that in contrast, in 2012, Facebook made a multi-billion-dollar takeover of Instagram, a young company of 13 employees. The life-span of a typical company is now of the order of 15 years, and he predicted that 40% of existing Fortune 500 companies would be out of business within the next 10 years.

Returning to the theme of local-and-linear thinking, Dr. Diamandis explained the philosophy of Singularity University in the study of exponential technology—with the example that thirty linear steps would gain a distance of thirty metres, whereas thirty exponential steps would circle the world twenty-six times. And Moore's Law exemplified the exponential growth in computing power, to almost inestimable levels in the future.

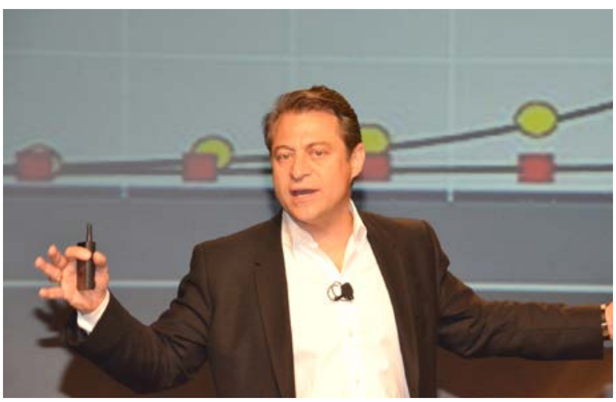
Near-infinite computing power could open up new dimensions in artificial intelligence—the ability to look beyond plain logic, even recognise the subtleties of irony, cynicism and humour, and understand what answer is relevant. Couple this with robotics, where a paradigm change is well underway, and truly intelligent machines are already a reality, as demonstrated in Dr. Diamandis' video of the view from the passenger seat as Google's autonomous car negotiated a slalom course at high speed. 3D printing is another area of exponential development, with amazing engineering capabilities. Breakthroughs in genome sequencing have enabled developments in synthetic biology to the extent that printed DNA molecules have been produced.

It was clear that the rate of innovation is exploding, and innovation is coming from everywhere. True breakthroughs generally come from unexpected directions. Dr. Diamandis made it plain that any company relying only on innovation from within was probably going nowhere and that to limit risk was to accept a future of, at best, incremental improvement.

Diamandis is a great believer in crowdsourcing. Lindberg flew the Atlantic to claim a $25,000 prize. Diamandis had a longstanding ambition to get into space. How? By throwing out the challenge to the world and offering a $10 million X-Prize as the incentive, which resulted in 26 teams spending a total of $100 million. "Set a target and challenge the world to solve the problem. Winner takes all—no second prizes!" He believes the world's biggest problems present the world's biggest business opportunities.

A question from the floor related to schoolchildren having little interest in taking up careers in science and engineering: How to inspire them? Dr. Diamandis suggested the answer was to make the scientists and engineers the rock stars, and to encourage the young people to perceive them as role models. The question he posed was, "How about a competition for the youngest person ever to travel to the space station?"

What is the next X-Prize challenge? Healthcare—to develop a hand-held universal medical diagnostic device. And after that, to achieve global literacy, even in the most impoverished areas.



Dr. Peter Diamandis

Dr. Diamandis' closed by declaring, "The only constant is change, and the rate of change is increasing. The next twenty years are going to be transformational. There's lots of change ahead, and the rate of change is increasing beyond our ability to project it!"

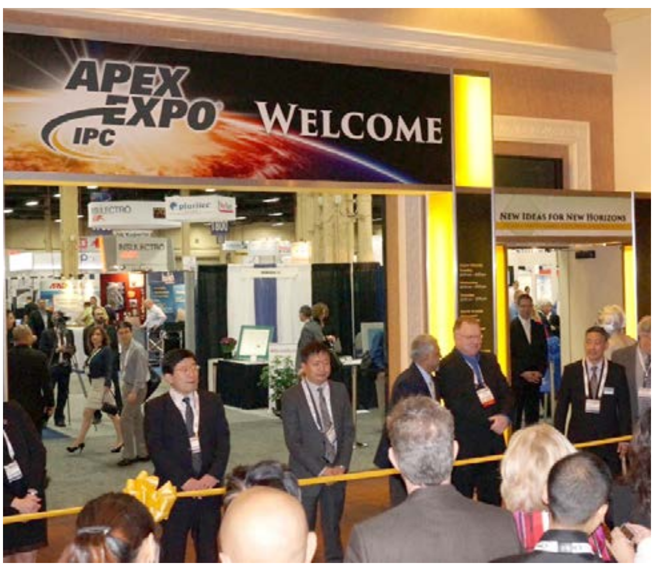
IPC APEX EXPO 2014: Publisher's Report

by Ray Rasmussen
I-CONNECT007

A sold-out show, record conference attendance and solid floor visitors made for a good show and conference at this year's IPC APEX EXPO in Las Vegas.

Here are some of my highlights.

Mentor introduced a major new software suite designed to remove the information barriers created by disparate systems. The software streamlines the design-to-fab-to-assembly information flow. Not being a user of software for design, fab or assembly, I can't speak to the software's effectiveness but, conceptually, it's a great idea and one that's been talked about for years. In fact, IPC hosted a meeting over a decade ago, which was well attended, and dealt with the communications issues in the supply chain. Think of how far along we'd be if that effort had gained traction. It's definitely a move in the right direction.

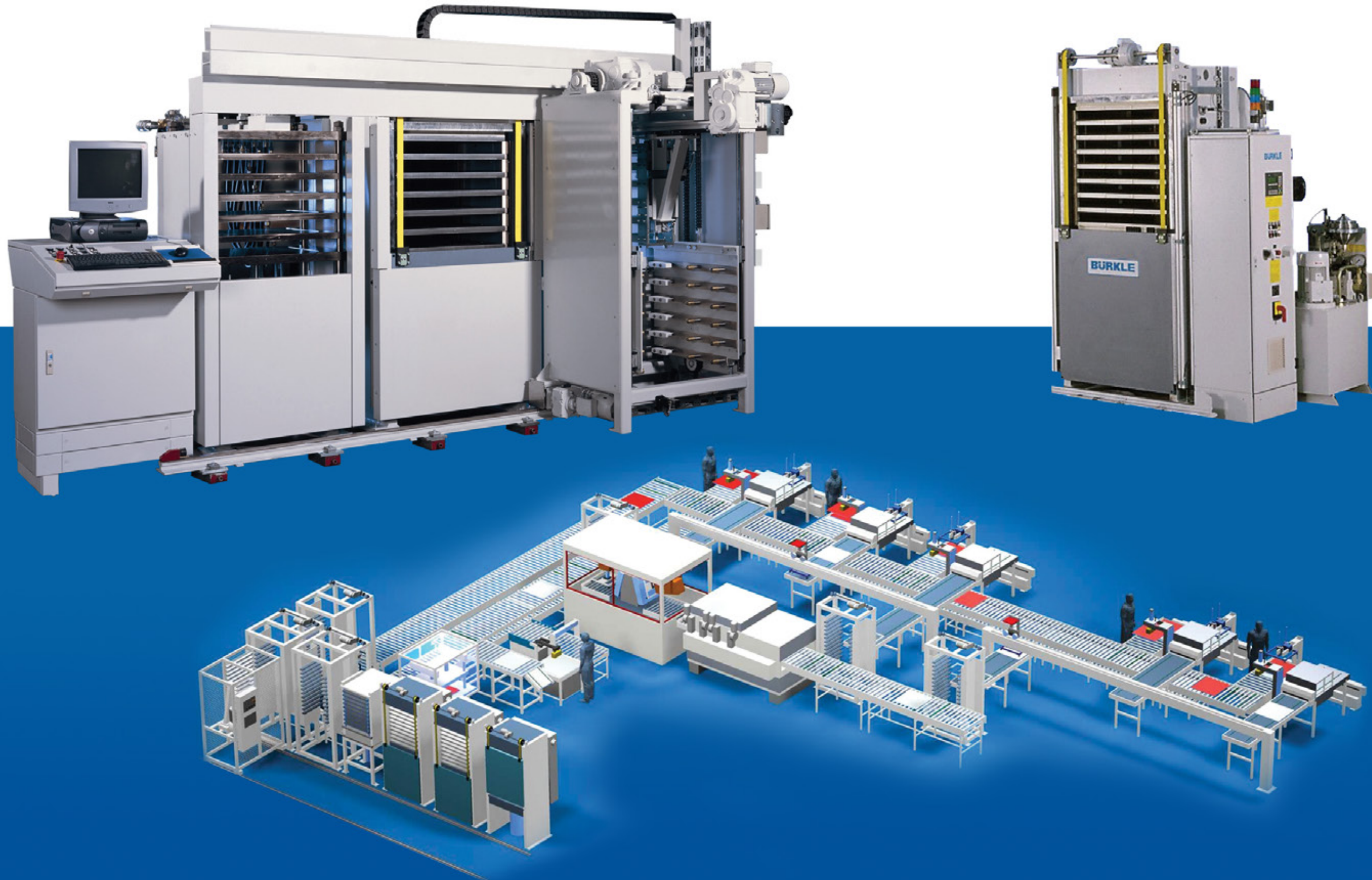


The *Printed Circuit Handbook, 7th Edition* is in the works. Editor Clyde Coombs came out of retirement to tackle the latest update of the PCB industry bible. First published in 1967, Coombs says this edition will likely contain up to 20% new content with all chapters getting significant updates, as needed, from some of the industry's leading experts. It's a labor of love for Coombs, who spent much of his career at HP in their PCB facilities. He says the book effort helps him stay connected with the industry.

Printed electronics, in its first-ever all-day session at an IPC event, offered a series of presentations from materials suppliers as well as PE makers, demonstrating the interest this technology is generating. In addition to the conference, an entire day was dedicated to standards development efforts. Marc Carter stated that IPC is working with organizations around the globe to develop the standards needed for this rapidly evolving industry. Currently, all of the standards IPC is working on are co-authored with JPCA. At this point in time, IPC is a leader in the development of PE standards for PE materials.

Walt Custer gave quite an upbeat assessment in his state-of-the-market report. All indications point to a year of good industry growth for most regions. The U.S. should see solid growth while Europe may see some growth, but will likely remain flat. Of course, one area of concern is the situation in the Ukraine. Although not big electronics industry players (Ukraine and Russia), the crisis could rattle markets around the world.

The sold-out show itself was very good; exhibitors were pretty happy. Their feelings were likely a direct result of the conference attendance, which translated into solid show-floor attendance. It will be interesting to see how it goes next year when we're back in San Diego.


BÜRKLE

Editor's Notes IPC APEX EXPO

by Lisa Lucke
MANAGING EDITOR, *THE PCB MAGAZINE*
CO-MANAGING EDITOR, *SMT MAGAZINE*

If you attended IPC APEX EXPO 2014 in Las Vegas last week, you'll know that it was a packed house for the most part, and offered something for everyone, from equipment on the show floor (many with "SOLD" signs) to technical conferences, standards meetings and of course, our *Real Time with...* video program. Our I-Connect007 team churned out more than 130 interviews with industry leaders, reps, fabricators, and designers, along with a handful of panel discussions that featured a moderated format aimed at generating lively discussion on key issues facing the industry, like onshoring, data file formats, the future of flex, and more. If you haven't seen it yet, check out our *Real Time with...* video index by clicking here. Most of the video interviews and panels are viewable now, and in the coming days, weeks and months, these videos will be featured in our newsletters and monthly magazines, and of course on our website. To subscribe to any of our publications, click here.

See you in San Diego in 2015!

Designers Step up at Design Forum

by Andy Shaughnessy
MANAGING EDITOR, *THE PCB DESIGN MAGAZINE*
CO-MANAGING EDITOR, *SMT MAGAZINE*

After two years in San Diego, the Design Forum was back on familiar turf this year as IPC APEX EXPO returned to Mandalay Bay Hotel and Convention Center in Las Vegas.

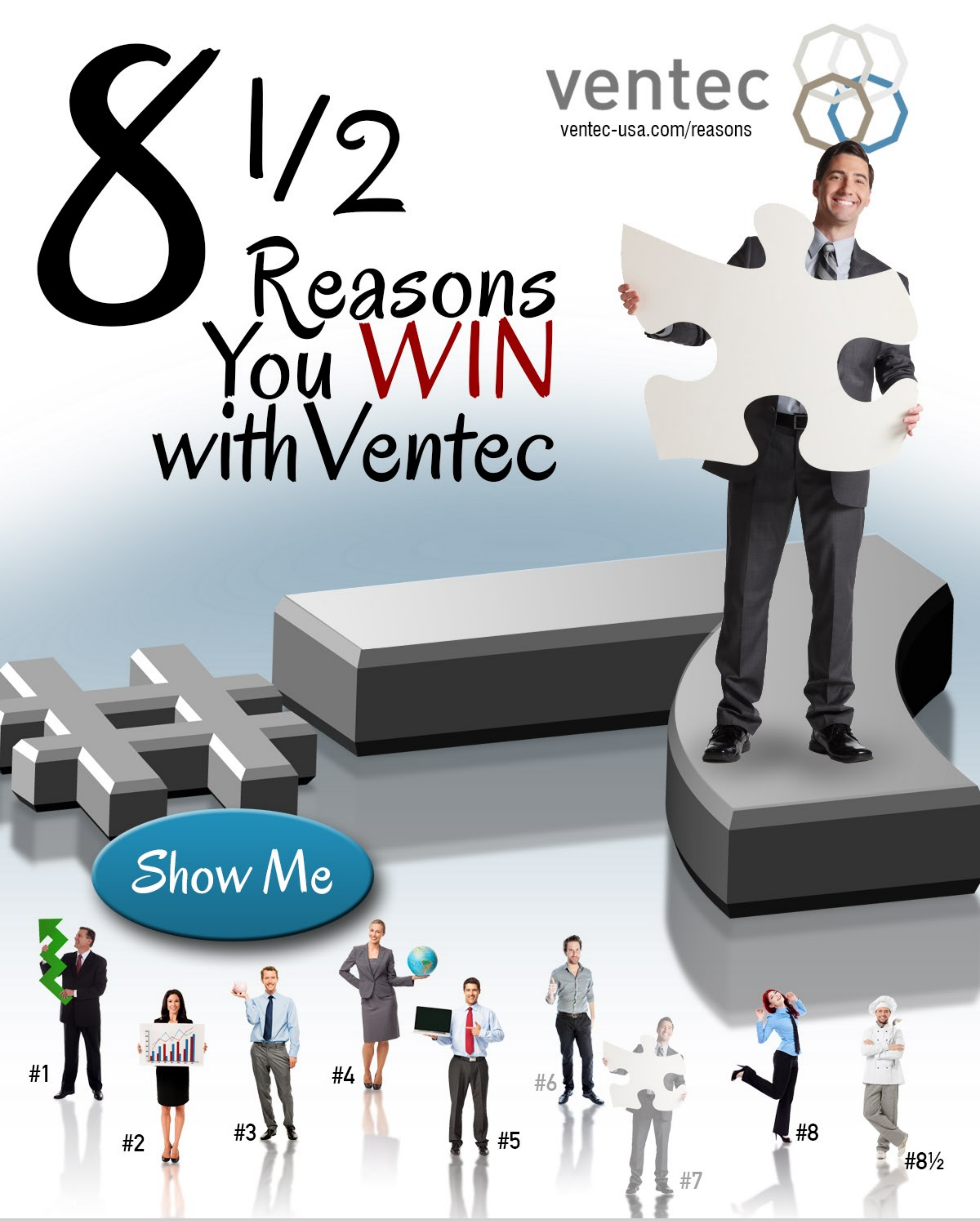
Forum speakers included Greg Munie of IPC, Karen McConnell of Northrop Grumman, Gary Carter of Fujitsu, Dieter Bergman of IPC, Mark Laing of Mentor Graphics, Humair Mandavia of Zuken USA, and Ben Jordan of Altium.

Although busy doing our *Real Time with...* video interviews much of the time, I managed to catch some of the sessions. Carter's discussion of the IPC-2581 data transfer standard was well received, and, of course, it led to some good back-and-forth during the Q&A period.

While sitting in on the Design Forum, Guest Editor Kelly Dack met first-time attendee Halil Yaslak, a PCB designer with Aselsan, a defense company in Ankara, Turkey. We talked him into doing a video interview. Yaslak was one of the younger designers at the Design Forum, but he's a heavy hitter; he took home first place honors at the 2012 Mentor Technology Awards for a 26-layer HDI board. He's definitely someone to watch and we look forward to seeing him next year if he's able to make the long journey again.

When the forum was over, most speakers and attendees trooped over to Rainer Thuringer's Professional Development class on optimizing high-speed design. Thuringer is chairman of the FED, a German organization that represents electronics designers and manufacturers. With a Ph.D. in physics, Thuringer has a unique viewpoint. He stresses the critical demand for finding "new blood," as well as the EMS community's need to focus upstream, on the challenges facing PCB designers and design engineers.

Altium's Ben Jordan also moderated our panel discussion on data transfer standards, which is always a contentious topic. As Ucamco's Karel Tavernier joked beforehand, "No daggers?" Tavernier's company owns the Gerber standard, and he joined Mentor's Dave Wiens, who represented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Designers Step up at Design Forum *Continues*

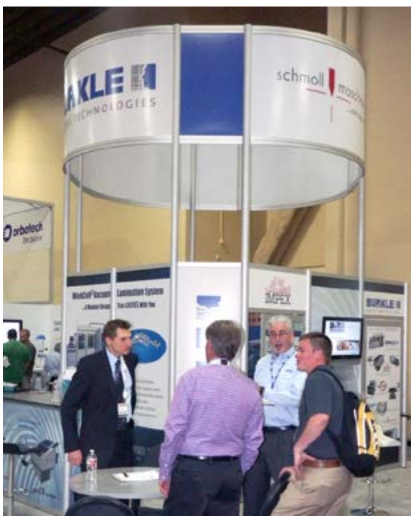
ODB++, and Hemant Shah of Cadence Design Systems, who is active in developing the IPC-2581 standard.

These panelists kept the marketing to a minimum and addressed the facts surrounding this hot-button issue. We shot a variety of these panels, but the data standard panel drew the biggest crowd; each format attracted its own entourage. But no panelists were injured during the filming of this panel.

In other news, Rick Hartley announced that he is really, truly retiring from L-3 Avionics this year. But he'll continue to teach design classes and stay active in the PCB community. He just won't have to get up to an alarm clock anymore, which sounds like a plan.

Overall, the Design Forum and IPC APEX EXPO went off without a hitch. Our booth was packed all week, with interviews set for every 15 minutes. And we saw solid traffic in the aisles the first two days, and OK traffic on the last day. Next year, the show moves back to (hopefully) sunny San Diego. See you in the Gaslamp Quarter!

Ben Jordan and Andy Shaughnessy



IPC APEX EXPO 2014
Show Review
LAS VEGAS, NEVADA

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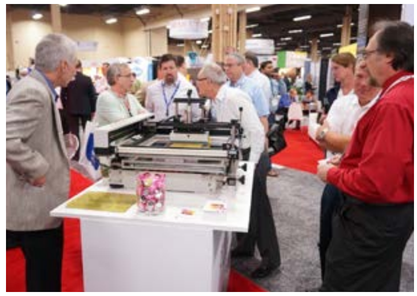

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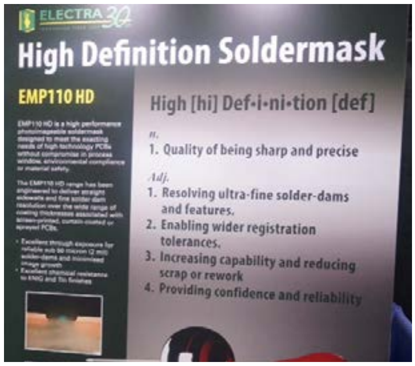

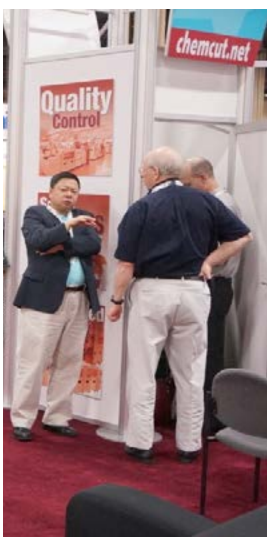

Is Your DAM Job Killing You?

by Gray McQuarrie
GRAYROCK & ASSOCIATES

"Our jobs are killing us!"
—Simon Sinek

If you have worried about whether your job is killing you, I want you to do something right now. I want you to admit that you are not competent to do everything your job entails in the time it is required. And I want you to say it out loud (perhaps out of anyone else's hearing range). This is a presumptuous thing for me to request, but let's see if I can justify my position so that I am not banished from writing this column.

The first step in getting better is to admit to the root reality of the true problem. The reality is our jobs have become so demanding and complex that even if we had superhuman powers we would not be able to satisfy everyone all of the time. We likely fail in some way every single week (a multitude of times) or maybe even every single day (at least once). When you can admit this, you will likely experience a brief moment in which you feel less stressed; your body and muscles relax, and your pulse slows. This is very healthy.

Let's take this further. Imagine if you could admit you aren't perfect to your boss and coworkers in an environment where everyone understands, supports you, and has your back? Would this be better for you? Is this the way your work environment is today? These are rhetorical, because we would all want this. Let's go deeper and see how you behave. How do you contribute to a positive, healthy work environment? For example, what do you say and how do you act toward a subordinate when you discover they have made a mistake? How often do you talk badly about someone behind his back? These are vitally important questions, because what you are doing and how others are behaving may not only be sapping your company of productivity and performance, but be killing you too. As

I said in my DAM books, "work is social, our behaviors lead results, and our behaviors are governed by our thinking."

There is a myth that what motivates us is purely self interest. In fact, this myth seems to be the operating principle behind capitalism. But is it true? Simon Sinek explains in this video on YouTube that our brains aren't wired like that. He also explains anthropologically, how the chemicals described in Table 1 are part of a system that has been essential to our survival for the last 50,000 years. Sinek explains that part of our brain is wired for selfish interests (utilizing endorphins and dopamine), and part of us is wired for social interests (utilizing serotonin and oxytocin). Finally, another part of our brain is wired to respond quickly and suddenly to danger (cortisol). When these chemicals are properly balanced, we are in balance, and we are healthier and have a greater chance to live longer.

Unfortunately, in our industry, most of us work in an environment that is extremely competitive, judgmental, and harsh. This stresses us out and we respond in very unhealthy ways to avoid the stress and the pain. In order to understand what is happening, so that we can fix it, we need to understand the chemical substances that are at the root of our behavior.

Chemical	Type	What it Does
Endorphin	Selfish	Masks pain. Allows us to run prey down without feeling the pain. Think of a runner's high.
Dopamine	Selfish	Creates pleasure. We feel good about completing stuff. We will eat even if we aren't hungry (because we get a hit of dopamine), which was good for survival, but problematic today. Dopamine is highly addictive.
Serotonin	Social	A natural mood regulator that curbs cravings (such as overeating). It is also our "status" chemical that helps us feel good about our place in the social hierarchy. We enjoy the success of those that we feel a close connection, as if it was our own. We can artificially trick serotonin with unearned social status.
Oxytocin	Social	The "love" or "trust hormone." When we hug someone we feel close to, we get a boost in oxytocin. This is why we feel a sense of safety in numbers when we are within a group we trust. It is why a social conversation is often better than an email when you need to be understood or influence another to action.
Cortisol	Stress	"Run Forest, run…" Cortisol is the stress hormone. It causes hyper vigilance and awareness in the face of danger (real or perceived). In fact, if one person in our group is fearful and their cortisol levels spikes, we too will become fearful and our cortisol will spike. If the fear is chronic we will have chronically high levels of cortisol in our body, which depletes our immune system, leave us open to heart disease, certain cancers, and so on. Chronically high levels of cortisol can kill us.

Table 1.

Endorphin and dopamine are the selfish chemicals. Endorphins kill pain. When I ride my bike thirty or so miles I get saturated with endorphins, which feels great, until they wear off. This quality of making physical work feel good motivates us to go out and do more hunting. This was a great survival mechanism long ago. Today, endorphin provides a way for us to numb pain we might also be experiencing in the workplace. But if we work out (or work) too much, and don't allow our bodies and minds to rest and recover, cortisol is elevated, which is a killer. There is a famous quote, "any great endurance athlete is running away from something." What about dealing with the real problem that is at the source of the pain? Typically, a chronic emotional problem requires admitting to the problem and seeking out other people who can help. When we aren't allowed to, or choose not to do this, we get sick even if we are working out and trying to be healthy.

"Understanding the next two chemicals, the "social" chemicals, could be life changing for you, particularly if you believe that most, if not all, people are motivated by self interest only. By the way, there is a name for people that behave this way and they are called psychopaths."

Dopamine is the most well-known chemical on our list. It is our feel-good chemical and it is the reason why addictions are so hard to break. But it is also the chemical that gets released when we accomplish something and feel good about it. So dopamine isn't all bad. For example, before we knew how to farm, raise live stock, and create an abundance of food, dopamine motivated us to eat even if we weren't hungry. This isn't good for us today.

A dopamine high is something we all selfishly want. Unfortunately, we can get it in very dangerous ways. When we take drugs, we get huge spikes in dopamine. Dopamine is also affected by how we choose to treat the people at work, because one way or the other, we will get it.

Understanding the next two chemicals, the "social" chemicals, could be life changing for you, particularly if you believe that most, if not all, people are motivated by self interest only. By the way, there is a name for people that behave this way and they are called psychopaths. Unfortunately, when you talk to companies that describe what they are looking for in hiring a new leader much of what they describe are many of the traits of psychopaths or more formally known as antisocial personality disorder[1]. If you think I am kidding check out this quote from an article by journalist and entrepreneur Brian Basham: "Beware of corporate psychopaths—they are still occupying positions of power…At one major investment bank for which I worked, we used psychometric testing to recruit social psychopaths because their characteristics exactly suited them to senior corporate finance roles."

Is it any coincidence that we have had the spectacular rise and fall of companies like Enron, WorldCom or Tyco? What about the banking crisis? Were investment firms deliberately hiring psychopaths? Is it still going on? How about closer to home with our own experiences at work? How many of us can recall a time when we were berated or shamed, collectively or individually, by the so-called leader? There are an encyclopedia's worth of examples I can recall, but I will share just one. A general manager of a very large board shop at the time (now defunct) told me in the hallway that I was too smart for my own good. How was that statement going to help me, help him? Did it make me feel important or did it make me feel ashamed? Did it calm me down or stress me out? Did it build or kill trust? Was it meant to harm or help? There is a study that supports this selfish, psychopathic behavior as being bad to the financial results of a business.

Here is the reality, and here is the truth: As healthy people, we aren't wired to be motivated by self-interest only. The social chemicals serotonin and oxytocin prove that. Serotonin is the "status" chemical. We get a dose of it when we accomplish something and are appreciated by others. If we merely accomplish something without recognition, we may or may not get a hit of dopamine, but for sure we don't get any serotonin. When appreciated, we not only get a hit of dopamine, but also a hit of serotonin. We get a dose of serotonin when we see a friend or family member do something important. Serotonin creates strong feelings of belonging, confidence, and pride. We need it, and we will do all sorts of things to get it. It's why designer jeans sell! Is also explains why none of us like working for a dictator or like being treated like slaves. When companies can provide multiple ways of achieving status for employees at every level, they have a maximally engaged work force. This was true when Honda gave workers the authority to shut the line down—it raised quality. If you order workers to just follow procedure they will undermine you, because their defiance raises their sense of importance, and their level of serotonin.

This is the key, by the way, to reducing your scrap rate. Scrap is a behavior problem, which I described in Can Scrap be Beaten? (December 2013).

Did you know that humans get extremely depressed and will likely die if we aren't allowed physical contact with people? Oxytocin is a strong reason why our social connections are vital to our survival. The only way we can receive the pleasurable feelings oxytocin gives us is from a hug, a kiss, or even a hand shake. If we have low levels of oxytocin, we don't trust, and we aren't generous. Moreover, if we didn't have oxytocin and truly lived only for our own self interest our species would have been extinct long ago. So there is an important survival component to oxytocin. The downside of oxytocin is it leaves us vulnerable to con men. They understand our instinct to want to do good and they exploit this fact to rip us off. For example, we may think our credit card number is helping a child in Africa, when in fact it might be just lining the pockets of some unscrupulous cons.

Finally we get to cortisol. Long ago, when an important manager at Photocircuits told me that if I didn't get my line problem fixed I would be fired in two days, what happened to me? My heart rate increased, my immune system buckled, blood sugar surged through my blood stream, my muscles tensed, and I lost all cognitive higher-order brain functions. These are just some of the effects of cortisol. They are great when you need to run away from an animal that wants to eat you, but not so great when you have to solve a complex problem. Fear is not a way to motivate people. Fear is a way to kill people. The problem on the line went away on its own, but I got sick and had to take a couple of days off from work, because the prolonged high level of cortisol wreaked havoc on my immune system. This manager, by the way, wound up dying in his early sixties from a sudden heart attack. I liked him as a friend, but he worked in and amplified fear as a motivator within the work environment, which he believed was essential and good. Unfortunately, he didn't understand how we are truly wired and just how unhealthy a lifestyle soaked in fear could be.

When I visit board shops, many of the general managers aren't in the best of health and appear stressed out, with little time to relax and just enjoy time with friends and family. The conversations always drift to pressure and sacrifice and often shift to some recent health problem. It's as if sublimely we all see the problem—a problem that we are fond of denying. The fact is we will never be globally competitive, where everyone can give their best work, in a work environment of fear. Do you want to live longer? Do you want to change? Do you want your company to be maximally competitive? Are these rhetorical questions? Then "just do it." Changing this doesn't cost much money, but it may require asking for some help. You can stop your job from killing you. **PCB**

References

1. Diagnostic and Statistical Manual of Mental Disorders (DSM).

Gray McQuarrie is president of Grayrock & Associates, a team of experts dedicated to building collaborative team environments that make companies maximally effective. To read past columns, or to contact McQuarrie, click here.

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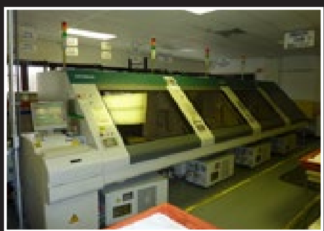

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Friday, May 2nd
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Preview:
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Tuesday Apr. 29
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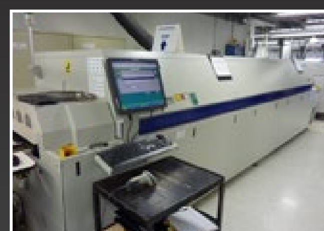

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PC BOARD FABRICATION

- (2) Hitachi ND-1V284E-4 Pod Ind. CNC Drilling Systems, 160k RPM
- Numerous Orbotech Discovery AOI's
- Numerous Orbotech Veriwide Verification Stations
- (2) Orbotech DP-100 LDI's
- Circuit Automation DP2500 Vertical Solder Screen Printer
- Lorr Herrmann LH 305 SMCNC Scoring Machine

SMT EQUIPMENT & TEST

- 2011 Universal Genesis GCI, 4 Lightening Head/Beam
- 2011 Universal Genesis Series III GX, Lightening Heads
- (4) Universal GSM Genesis as late as 2005; Various Heads
- (2) 2011 Cyber Optiic SE500-X In-Line Auto Solder Inspection
- (54) Gold DL 8 Universal Feeders
- (684) Pneumatic Universal Feeders

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Mil/Aero007 News Highlights

Dragon Circuits Implements Drone Program

Texas-based PCB fabricator Dragon Circuits announces the inception of their latest R&D and manufacturing unit, Dragon Drones. With the assistance of two state-of-the-art 3D printers and scanners, engineers will be able to conduct the rapid prototyping needed to test theories and designs at a competitive pace.

Army Must be Prepared for Threats to Energy Sector

Cybersecurity threats to the United States' energy industry and infrastructure are rising and require increased preparedness by the U.S. Army and Department of Defense, according to a new paper from Rice University's Baker Institute for Public Policy.

Asia to Become Aerospace Manufacturing & Engineering Hub

"The industry's push into Asia might have started off slowly compared to other sectors, but demand today for aircraft in the region is surging," says Alastair Swift. "Aircraft manufacturers such as Airbus and Boeing have projected that over a third of worldwide aircraft deliveries will go to Asia in the next two decades. By 2031, Asia Pacific's fleet is expected to triple to about 13,500 aircraft."

DARPA's Excalibur Program Expands Capability

The Excalibur program successfully developed and employed a 21-element optical phased array (OPA) with each array element driven by fiber laser amplifiers. This array was used to precisely hit a target 7 kilometers (more than 4 miles) away. The OPA used in consisted of three identical clusters of seven tightly packed fiber lasers, with each cluster only 10 centimeters across.

Small UAV Market at $582.2 Million by 2019

According to the new market research report Small UAV Market by Trends (Mini, Micro, Hand Held UAV), by Propulsion (Hydrogen, Electric, Solar, Lithium ION), by Payload (NBC Detection, Telemetry Systems, Software Systems, Meteorology), by Application (Civil, Military, Security), by Region & by Country - Global Forecast to 2014-2019, published by MarketsandMarkets, The small UAV market is expected to register growth with CAGR of 21.70%, and reach $582.2 million by the end of 2019.

U.S. Businesses Boost Cyber Security Spending

BAE Systems Applied Intelligence today quantifies the extent of the impact on U.S. businesses of the wave of recent high-profile cyber attacks in December 2013 and January 2014. New research conducted this month reveals that the attacks on international businesses, including banks and retail giants such as Target, led to a significant 60% of U.S. businesses surveyed increasing their cyber security budget.

DARPA Seeks Electronic Component Authentication Tool

The DARPA Supply Chain Hardware Integrity for Electronics Defense (SHIELD) program seeks proposals to develop a small component, or dielet, that authenticates the provenance of electronics components. Proposed dielets should contain a full encryption engine, sensors to detect tampering and would readily affix to today's electronic components such as microchips.

GreenForces Launches Operations

The Michigan-based consortium combines the expertise of a solid base of reliable partners to develop lighter, more durable, advanced material solutions for aerospace and defense customers. In addition to engineering support, GreenForces provides manufacturing capacity in composite materials, investment cast machining, and high-tech rigid circuit boards.

DoD Releases 2015 Budget Proposal of $495.6 Billion

President Barack Obama has sent Congress a proposed defense budget of $495.6 billion in discretionary budget authority to fund base defense programs in fiscal year 2015. The request is $0.4 billion less than the enacted FY 2014 appropriation and is consistent with the current budget caps.

Military Communications Market to Reach $30B by 2022

"Managing bandwidth in increasingly congested spectrum will be a key challenge in meeting future demands for data-centric military communications," observed Asif Anwar, director of the ADS service.

Green Technologies in PCB Fabrication

by Karl Dietz
KARL DIETZ CONSULTING LLC

"Green" and "environmentally friendly" are ill-defined terms. In general, these terms refer to manufacturing that involves the replacement of toxic substances with less toxic materials, the elimination of materials or processing steps, and less consumption of chemicals (i.e., more efficient or higher yield processing, reduction of water use, reduction of energy use, less space requirement, smaller equipment foot print, and recycling and on-site recovery of materials).

Direct Metallization

This family of processes eliminates the electroless copper process. These processes typically have fewer process steps, use less rinse water, have less floor space requirement, and use less toxic chemicals. Direct metallization processes include:

Palladium-based

These processes pretty much follow the classic electroless copper processing step sequence, except the sequence ends with the application of the palladium catalyst, followed by the activation, then skips the electroless bath and proceeds to copper electro-plating.

Carbon or Graphite-based

Using small carbon or graphite particles to render the dielectric hole-wall electro-platable, this process involves very few steps.

Conductive Polymer-based

The process of using a non-conductive monomer to coat the board surface follows an oxidation step that forms a conductive polymer from the non-conductive monomer. The

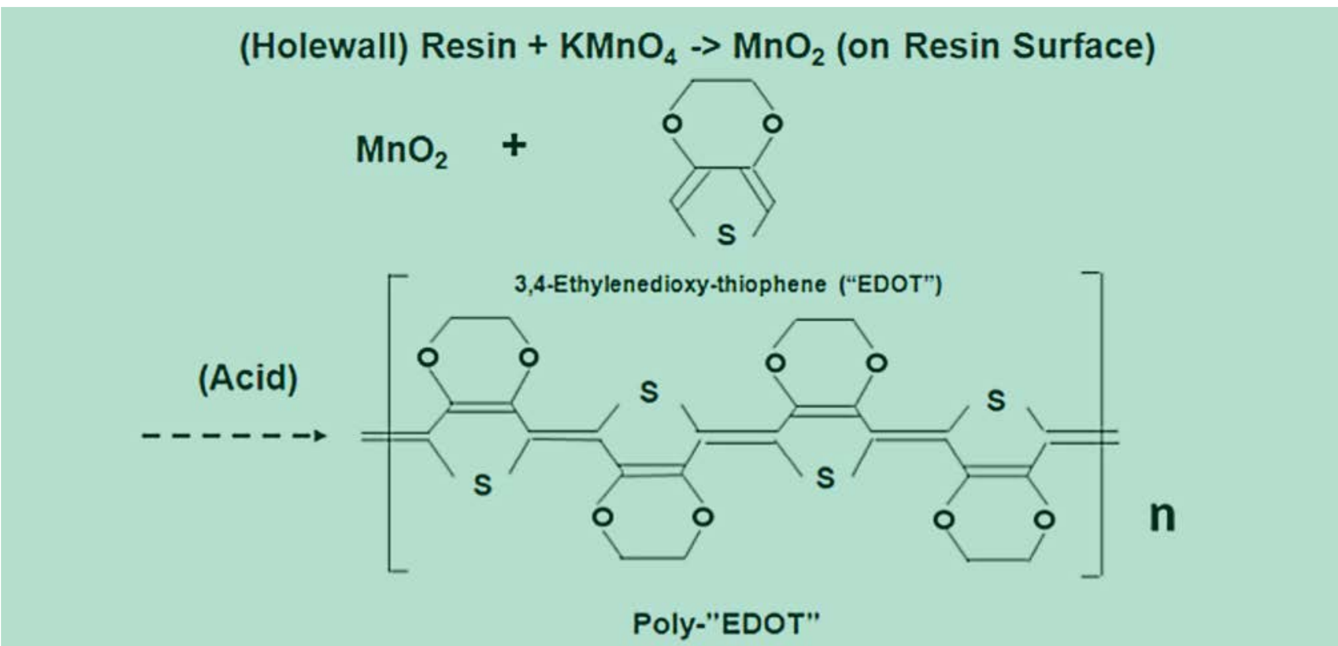

Figure 1: Formation of conductive poly-"EDOT" elimination of chemicals.

polymer then facilitates copper electro-plating on the non-conductive dielectric hole wall. An example of such a conductive polymer formation is the oxidation of pyrrole to poly-pyrrole, using permanganate as the oxidation agent. The permanganate is reduced to manganese dioxide, which is insoluble and needs to be further reduced to the soluble manganese Mn^{2+} ion. Another example is the polymerization of "EDOT" (3,4-ethylenedioxy-thiophene) to poly-EDOT (Figure 1).

The formation of resin coated foil (RCF) typically involves the use of a solvent or solvent mixture to form a resin solution for coating onto a copper foil. Atotech has pioneered an alternative approach that does not require solvent for the formation of RCF. It is a solvent-free powder manufacturing technology called ADEPT (advanced dielectric epoxy powder technology).

On-site Recovery and Recycling

An example of such green processing is Atotech's CupraEtch DE, an iron sulfate-based etchant with minimal undercut for differential etching in the so called semi-additive plating process (SAP). The process runs in parallel with a regeneration unit in which the etched copper is plated out for recovery and the ferric etchant is regenerated.

Elimination of Process Steps

Laser direct imaging (LDI) is a good example for step elimination. The digital CAD data guide a laser directly as it scans the photoresist surface to form a resist pattern. LDI eliminates the need for a phototool and thus eliminates all processing steps and chemicals needed to generate the phototool. In addition, LDI cuts manufacturing lead time and allows scaling of the image, an image compensation to optimize for best fit to registration reference points. It should be mentioned that all digital imaging techniques offer the above mentioned advantages, whether they involve a laser or not.

Substitution of Less Toxic Substances for Toxic Chemicals

Modified Electroless Copper Bath Chemistries

A traditional electroless copper bath uses formaldehyde, a suspect carcinogen, as a reducing agent. Some electroless copper baths have eliminated formaldehyde and have replaced it with hypophosphite, for example. Traditional electroless copper baths have also used stabilizers such as cyanide and EDTA (ethylene diamine tetraacetate). Cyanide is highly toxic and EDTA is a powerful complexing agent that interferes with the precipitation of heavy metals in waste treatment processes. Some electroless processes have eliminated these chemicals and use tartrate instead as stabilizer.

Other examples of substitutions for problematic chemicals include replacing non-biodegradable substances with biodegradable chemcials, (e.g., in cleaners). Gold baths have been modified to eliminate cyanide.

The elimination of lead from solder has been widely discussed, however the actual health and environmental benefits are debatable. Tin/lead solders have been largely replaced by the so-called SAC alloys (tin/silver/copper). Lead-free electroless nickel baths are now also available.

"The elimination of lead from solder has been widely discussed, however the actual health and environmental benefits are debatable. Tin/lead solders have been largely replaced by the so-called SAC alloys (tin/silver/copper). Lead-free electroless nickel baths are now also available."

The push to make base materials halogen-free is gaining momentum. Halogen-free is a bit of a misnomer because it really focuses on the elimination of tetrabromo bisphenol-A as a flame retardant for epoxy resins. While PTFE-based base materials contain the halogen fluorine, nobody is proposing to eliminate these base materials. The alleged problem with tetrabromo bisphenol-A is the potential formation of dioxines during the incineration of base material scrap. Alternative chemistries for tetrabromo bisphenol-A include phosphorus-based compounds, sometimes with added inorganic fillers. However, these phosphorus compounds are not universally accepted. Another approach consists of building inherent flame-retardency into the epoxy resin in the form of aromatic rings.

Alternative Metallization Technologies

There are a number of Z-axis metallization processes that are less wasteful than the traditional plating processes. A traditional through-hole metallization process such as panel plate/tent and etch deposits copper not only in the through-hole but also on the surface where it is not needed, consuming plating chemistry and generating an etching waste stream. Likewise, the pattern plate process requires extra steps for metal etch resist plating and etch resist stripping. In contrast, the ALIVH (any layer interstitial via hole) process uses no plating and etching to metallize the vias but uses a copper paste that is only applied to the via. The B^2it process is another such example: the metallization in the Z-axis to interconnect adjacent metal layers consists of multiple step screen printing of a silver paste by which cone-shaped bumps are formed that poke through the dielectric during multilayer lamination and make contact with the next metal layer. **PCB**

Karl Dietz is president of Karl Dietz Consulting, LLC, offering consulting services and tutorials in the field of circuit board & substrate fabrication technology. To view past columns or to reach Dietz, click here. Dietz may also be reached by phone at (001) 919-870-6230.

VIDEO INTERVIEW

The Impact of Miniaturization on Fab Processes

by Real Time with...IPC APEX EXPO 2014

Editor Andy Shaughnessy caught up with Sanmina's Brian Nelson at IPC APEX EXPO recently and discussed how fabrication processes are affected by advances in miniaturization.

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Customer Feedback: Perception is Reality

by Steve Williams
STEVE WILLIAMS CONSULTING LLC

"Perception is reality."
—Tom Peters, best-selling author

This quote from my favorite business author, Tom Peters, hangs in my office as a constant reminder. The title "world-class" rings hollow if you are the only one saying it about your organization.

Reality

How many times do we see a company promoting themselves as being a world-class manufacturer of PCBs, or as having been voted best-in-class at customer service? Who voted? Again, we are faced with the truth in advertising dilemma. It's a Dilbert cartoon in the making: a group of senior managers get together and declare "you know, we do a pretty respectable job in our business, let's begin calling ourselves world-class."

What does it mean to be world-class? Breaking it down into a single bullet point, it means being on par with the top performers globally in your chosen craft. There are, of course, numerous quantitative metrics used to measure this, such as turnover, quality certifications, productivity, and the requisite financial ratios. But perhaps the most important metric is qualitative: How do your customers think you are doing?

The Facts

You may in fact be a world-class manufacturer, but if your customers don't agree it doesn't really matter. It is surprising to find the high percentage of PCB organizations that have not formally incorporated an annual benchmark survey into their continuous improvement process. True world-class companies are no longer guessing what satisfies their customers; they are actively soliciting feedback and listening to their customers' expectations. A recent poll of over 2100 manufacturing respondents conducted by Industry Week Census supports this fact. It showed that 47% of respondents who say they've achieved a high level of world-class compliance use customer-satisfaction surveys extensively, while the proportion of peers claiming "no progress" in this area show only 6.4% as using them.

KISS

Keep It Simple Steve. There are many tools for soliciting customer feedback such as focus groups, interviews, customer complaints, and face time with the customer, but a well-developed survey can be the easiest way for a company to begin gathering customer perceptions. When designing the survey, making it as easy for your customers to complete is of paramount importance. How many of us have received a survey in the mail with a dollar bill taped to it, kept the dollar and tossed the survey? Why do we do this? Because it is a four-page paper survey with 40 questions that has to be put into an envelope and taken to a mailbox. No one has time for that. With today's technology, an e-mail or Web-based survey can be completed by a customer in three minutes without having to leave their desk. Remember, how you invite them to participate, the way you ask questions and which design template you use will affect participation rates. Surveying all of your customers will not net out the results you are looking for; applying the old reliable 80/20 rule to your revenue stream should result in capturing your top 10–20 customers.

A Web-based methodology is the preferable medium for ease of use, demographic data capturing, and automated scoring/reporting. It can also incorporate automatic email notification to senior management upon receipt of an unacceptable survey rating.

Actionable Strategies

When designing the questions to be used in the survey, take care to ask questions in which the subject meets the following criteria:

- Must be within the organization's control
- Must be one that the organization is committed to take action to improve
- Will provide a competitive advantage

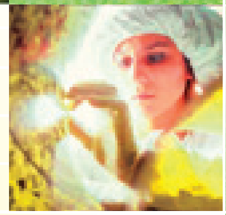
These may sound simple, but many times a company will implement a customer benchmark survey, review the data, and let the process end there. The summary data needs to be presented to a steering committee-level management group, actions assigned, and progress monitored throughout the year, tying out into next year's survey. The intent should be to capture your customer's perceptions of key areas of weaknesses and strengths, and develop an action plan to improve them.

How Not to Use Customer Feedback

Your goal with customer feedback is to gain honest, unbiased input that can be used to improve organizational performance. With that in mind, I would like to share a real life personal experience that exemplifies how not to do this. After having some maintenance done recently on my truck at a former "big-three" dealership, I received a customer satisfaction survey in the mail asking me to rate the quality of customer service during my visit. The same day I also received a personal phone call from the service technician that handled my truck, who wanted to let me know that any rating by me less than "excellent" would result in his getting fired, losing his first-born son, or some other undesirable consequences for him. I returned my survey with my honest critique, noting this conversation and taking exception to the methodology used by the dealership. But how many people would have felt pressured to rate their experience as excellent if it really wasn't? And how valuable is this information to the dealership? From a customer feedback standpoint, it is worthless, and it sure puts all the customer service awards hanging in the showroom in a different light.

No level of performance is sustainable without an occasional adjustment. The appropriate adjustment in strategy can only be developed after measuring your customers' perceptions. As I have said before, you can't improve what you haven't measured, and remember, "Perception is reality." **PCB**

Steve Williams is the president of Steve Williams Consulting LLC (www.stevewilliamsconsulting.com) and the former strategic sourcing manager for Plexus Corp. He is the author of the books, Quality 101 Handbook and Survival Is Not Mandatory: 10 Things Every CEO Should Know About Lean. To read past columns, or to contact Williams, click here.



PCB007 Supplier/New Product News Highlights

Aurora Nets UL Certification for Aismalibar IMS Materials

Chris Kalmus, CEO of Aurora Circuits, says, "We are excited to offer this world-class line of IMS laminates to our customers working on thermal management solutions. Aurora can now offer a high-quality European alternative to the small group of IMS materials currently available in the North American market."

Isola Promotes Gastonguay to President, Americas

Isola Group S.à r.l. has promoted Michael "Mike" Gastonguay to president, Americas. Raymond Sharpe, president and CEO, said, "Throughout his career, Mike has worked closely to help drive customer intimacy by leveraging his knowledge of operations and quality. His skills for collaboratively developing solutions will help Isola to expand in the years to come."

Rogers' Printed Circuit Materials Posts 26.5% Growth

Rogers Corporation (the company) has announced financial results for its fourth quarter of 2013, reporting net sales of $136.2 million and net income from continuing operations of $0.64 per diluted share, which includes a special charge of $0.17 per diluted share associated with an impairment charge related to a year-end accounting revaluation of an investment made in 2009.

LCOA Receives License to Manufacture Zeta Laminates

"LCOA is excited to manufacture the complete line of Zeta® laminates. These amazing HDI dielectrics are changing the way printed circuit boards are made," commented LCOA President Patrick Redfern. "Our mission is to deliver superior products to our customers--products that strengthen their capabilities. "

Orbotech's PCB Equipment Sales Up 11.6% in Q4

Commenting on the results, Asher Levy, CEO, said, "We are pleased to report a strong 2013 in which we posted robust revenues and much improved gross, operating and net margins. These reflected improving business conditions as well as the operational efficiency measures that we adopted at the end of 2012, and we were able to capitalize on opportunities in PCB and electronic components manufacturing.

Isola Expands Production of GETEK Materials

GETEK materials provide the low-dielectric constant and low-dissipation factors demanded by high-speed, low-loss PCB designs and applications, while providing superior thermal performance and high reliability based on the system's 180°C glass transition temperature (T_g).

PCi Installs Burkle Precision Lamination System

The new Burkle Workcell incorporates two, six-opening hot presses with 30" x 30" platens in conjunction with a six opening cold press. The lamination system also includes the addition of a buffer rack, which will give PCi the ability to layup multiple books at once for lamination. Burkle's incorporation of hot oil heaters will provide a more even distribution of heat across all platens and allow the product to be cooled under pressure at a predictable rate.

Fabstream and Electro-Labs.com Form Partnership

Fabstream®, the integrated PCB design and manufacturing service developed by DownStream Technologies, today announced it has formed a new partnership with Elecro-Labs.com. Electro-Labs.com is a free resource for DIY engineers and hobbyists that provides access a variety of original content including articles, blogs, tutorials and design notes to help them learn about electronics, how they work and how to design them.

Gardien Anaheim Expands Services to Include TDR

As the complexity of PCBs has increased in recent years the TDR testing requirements have also increased. To address the market's needs, Gardien has added TDR capability that is able to accommodate single-ended, double-ended, or buried striplines.

COLUMN

PTH Drilling Revisited: Fundamentals, Part 1

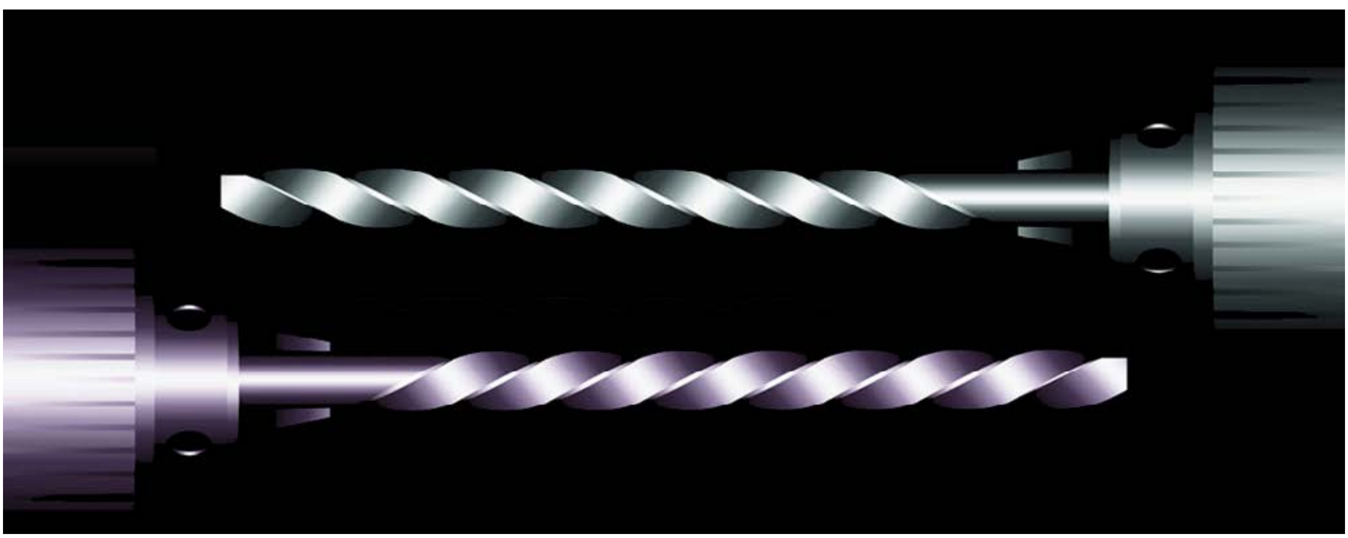
by Michael Carano
OMG ELECTRONIC CHEMICALS LLC

Anyone involved in coaching athletes preaches fundamentals. That means understanding what is at stake and relentlessly executing the basic fundamentals of the craft. Drilling circuit boards is no exception. The basic fundamentals of PTH drilling revolve around several key factors: (1) speeds and feeds—drill in-feed rate and spindle speed of the drill bit; (2) surface feet per minute and (3) the material to be drilled. Understanding and applying these first few critical factors will influence the overall quality of the drilled, plated through-hole, and eliminate issues such as rough hole-walls, excessive nailheading and resin smear. In a future column, additional drill fundamentals will be explored.

Regardless of whether you are playing a football game or manufacturing a printed circuit board, it is all about fundamentals. Understand what needs to be accomplished and how to get there. Success, however it is defined, should not be difficult to achieve. In this edition of *Trouble in Your Tank,* I will present some of what I consider the key fundamental understandings required if one is to drill a quality plated through-hole.

Basic Fundamentals

The goal is quite simple. You want to build as much reliability into the PTH as possible. Of course, there are numerous factors and process steps involved in manufacturing high-quality, highly reliable PCBs. And yes, drilling is just one of those processes. But the old adage applies here: Garbage in, garbage out. A poor quality drilled via will only exacerbate additional problems downstream in the fabrication process. So it is first and foremost about fundamentals. In my travels working with PCB and assembly companies on a global basis, I am often struck by the lack of understanding with respect to the basic fundamentals of drilling a plated through-hole. One would think that common sense would prevail, that does not always happen. Suffice to say that one should always consult the drill supplier with help in setting up the proper parameters. This will depend on hole diameters, board thickness, resin

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materials and drill machine capabilities. But there are basic fundamentals that apply. So let's discuss the basics and illustrate what some of the undesired outcomes are when we do not follow the rules.

Feeds and Speeds

Feed refers to the in-feed rate of the drill bit into the drill stack—essentially this is the Z-axis penetration. The rate in-feed rate is important for several reasons. If the in-feed rate is too great, there is risk to drill bit breakage and at the very least we get a very rough hole wall (Figure 1).

Figure 1: Rough hole wall due to poor drilling practice. Main cause—excessive in-feed rates of the drill tool.

One can easily discern the rough hole wall with gouges in the resin and glass fiber bundles protruding. A hole wall that looks like this makes it very difficult to ensure a plated via that is free of voids and has sufficient electroplated copper thickness to ensure that the deposit will withstand multiple thermal excursions.

Of course, there are additional causes of the protruding glass fibers. In this situation, the cause can also be attributed to a slow drill tool retract rate. The retract rate is the rate at which the drill bit is withdrawn from the via. This is also known as the Z-axis return. Similar to the in-feed rate, the return rate is measured in inches per minute. I prefer a Z-axis return rate at 2x the rate of the in-feed penetration. Again, the reason behind the 2x retract rate is to minimize the amount of time the drill bit remains in the via. The longer the drill bit is in contact with the via, the greater the heat that is generated. This in turn increases the opportunity for drill smear (Figure 2).

Another look at nail-heading in the cross section in Figure 3 brings to light another concern. This concern relates to some direct metallization processes that require a micro-etch prior to the deposition of the conductive coating. If there is excessive nailheading, there is a risk that the thinner portion of the flared copper interconnect will be etched away. This then creates an area of high resistance for subsequent electroplating of copper. Yes the cross-section is

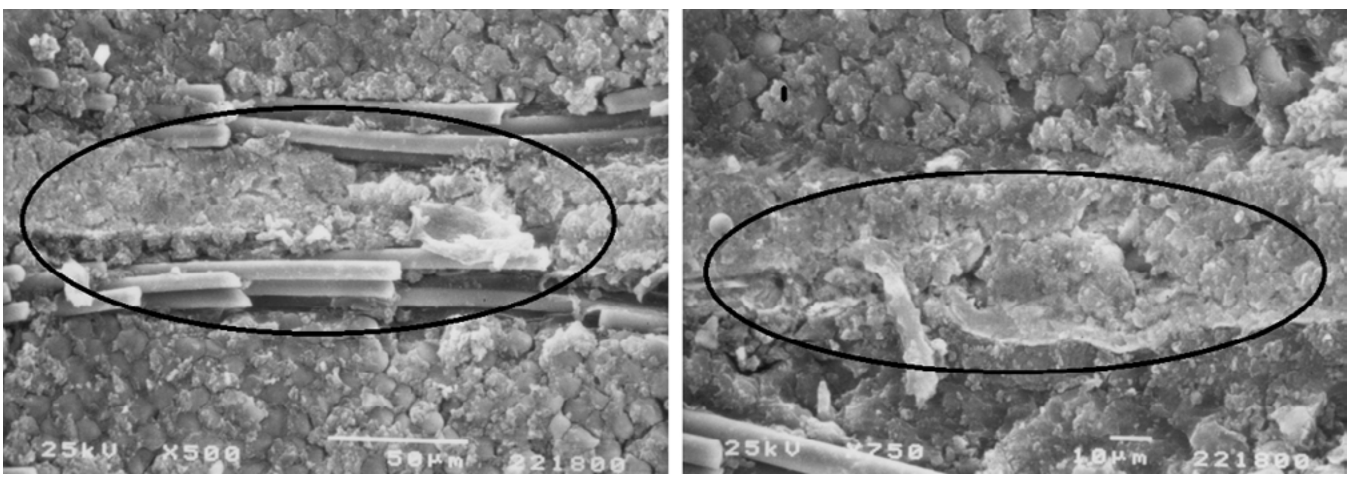

Figure 2: Excessive drill smear and possible deformation of the innerlayer copper foil-nail heading.

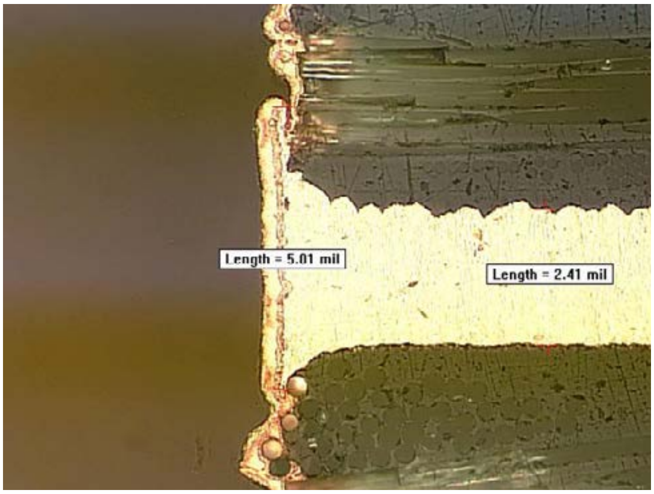

Figure 3: Excessive nailheading (a.k.a., the wall of shame).

aptly dubbed the "wall of shame." But nonetheless, this condition is a possibility.

Spindle Speeds

This parameter refers to the rotational rate of the drill spindle measured in revolutions per minute (RPM). The rotational rate of the drill spindle impacts hole-wall quality in a number of ways. First, excessive speeds will generate more heat, resulting in excessive smear formation. In addition, exceeding the recommended spindle speeds will cause the cutting edge of the drill bit to wear prematurely. Cutting edge wear or rounding as it is often called, results in the drill bit punching its way through the via. Certainly, the punching condition results in rough hole-walls, torn-out glass bundles and broken drill tools.

Surface Feet per Minute, or per Meter

The surface feet per minute, or meter parameter (SFM), is directly related to spindle speeds. Basically, SFM is the distance a point on the drill bit traverses over a period of time. To calculate SFM, use the following equations:

$$\text{Cutting Speed (SFM)} = \text{spindle speed (RPM)} \times \varpi \times \text{diameter (in)}/12.$$

$$\text{Cutting Speed (m/min)} = \text{spindle speed (RPM)} \times \varpi \times \text{diameter (mm)}/1000.$$

What Material are we Drilling Through?

Why is this significant? Well, the longer the drill bit stays in the hole, the greater the opportunity to generate more heat. And with more heat comes resin smear. Obviously, minimizing smear is a top priority. It is also important to realize that one SFM parameter will not apply to all material sets. As an example and from working with numerous PCB fabricators in troubleshooting situations, I have set up a few SFM rules (to serve as a starting point guideline). Again, these are only starting point suggestions and may require adjustments based on layer counts, copper thicknesses, etc. In all cases unless otherwise noted, chip load varies with drill bit diameter.

So as a starting point:

- Standard FR-4 epoxy (135–140 T_g) 470–505 SFM
- Epoxy-higher T_g (170–180 T_g) 460–500 SFM
- Polyimide 390–495 SFM
- Epoxy PPO/IPN 375–400 SFM

Ideally, these are guidelines only, but should serve as a good starting point when optimizing the drilling operation.

Conclusion

Good quality plated through-holes must first start with a high-quality drilled hole. Understanding that drill feeds and speeds, surface feet per minute and the actual material drilled through will influence the overall drilled hole quality. Being able to recognize drill defects early will enable the engineer to properly adjust the key parameters in the operation and ensure a high quality drilled via. **PCB**

Michael Carano is with OMG Electronic Chemicals, a developer and provider of processes and materials for the electronics industry supply chain. To read past columns, or to contact the author, click here.

A Summary of Various Test Requirements

by Todd Kolmodin
GARDIEN SERVICES USA

IPC Class 3

The PCB industry has advanced significantly in the recent millennium. OEM specifications and requirements have also advanced due to the maturing of technologies, which has caused the requirements of electrical test of these higher technology products to advance and increase in intensity. Obviously, the more mature a technology, the finer the lines and spaces must be, the more hole and vias must be present, and the more complex the testing must become. There is just more to test in a smaller amount of space.

Long gone are the "pin-in-hole" technology PCBs, which are now surpassed by the large multilayer, blind/buried and rigid-flex technologies. For the suppliers of electrical test, be it in-house test departments or sub-contracted, the industry specifications can be confusing, and at times incomprehensible.

The OEMs direct the IPC specification (6012, 9252A, AS9100, etc.) for their fabrication to the manufacturer, but in many cases do the OEMs or CMs really know what they are asking for? Do they really understand what they are requiring and how complicated it may be?

There are many variables associated with these specifications and requirements to their designated classes regarding electrical test. OEMs often overlook the electrical properties associated with IPC class performance requirement, and of course, this can be a problem. Manufacturing, plating, etching and all those processes may be within the class requirements.

During the coming months, I will discuss various aspects and intricacies of electrical test. To get started, I will address IPC class 1, 2, and 3.

Class I: General Electronic Products

This class includes consumer products, some computer products and computer peripherals suitable for applications where cosmetic imperfections are not important, and the major requirement is function of the completed board.

Class 2: Dedicated Service Electronic Products

This class includes communications equipment, sophisticated business machines, instruments where high performance and extended life are required and for which uninterrupted service is desired, but not critical. Certain cosmetic imperfections are allowed.

Class 3: High-Reliability Electronic Products

This class includes the equipment and products where continued performance or performance on demand is critical. Equipment downtime cannot be tolerated and must function when required as in life support items or light control systems. Printed circuit boards in this class are suitable for applications where high levels of assurance are required and service is essential.

Requirements for Testing Class 1–3 and 3/A

Minimum electrical test requirements are different between IPC classes. This does not mean that opens or shorts are allowed! However, the electrical thresholds to identify these conditions are different. In the electrical test industry we are not only looking for the extreme cases (infinite open or direct short) we are also looking for indicators of what MAY be a potential problem. This is why the minimum requirements are different between classes. Table 3-1 identifies this.

As seen in Table 1, the resistive continuity and resistive isolation requirements are much different between Class 1 and Class 3. Notice that indirect continuity and isolation testing by signature comparison is allowed in Classes 1 and 2, but AABUS in Class 3. This does not mean that it cannot be used, but it does require authorization from the OEM or customer for that method to be used on Class 3 product.

Class 3/A Exception—Space and Military Avionics IPC-6012, Appendix A

This is an exception beyond the standard Class 3 requirement for electrical test. In this case, parameters are specified when testing product under this class. These requirements need to be on the master drawing and communicated from the OEM to the manufacturer or this type of test may be overlooked. The differences with Class 3/A are shown in Table 2.

Design Concerns vs. Class Requirements

From an OEM or designers perspective one must be aware of constraints built into the board design that may cause some difficulty during electrical test. We find this most prominent with Class 3 product designs. From Table 1 we see that for continuity resistance there must be no circuit in the board whose resistance is greater than 10 ohms. That is the standard. A couple problems come into play here. If you will look back to note 4, below Table 3-1, you will see a statement regarding referee calculations for circuit length. With that said, a board may be out of tolerance to Class 3 with any net

Requirements by Test Level

TEST LEVEL	A	B	C
Performance Class	1	2	3
Source Data	CAM, CAD	CAM, CAD	CAD[1]
TEST METHODS			
Resistive Continuity Testing	≤100Ω	≤50Ω	≤10Ω[4]
Resistive Isolation Testing	≥500kΩ	≥2MΩ	≥10MΩ
Indirect Isolation & Continuity Testing by Signature Comparison	Yes	Yes	AABUS
Adjacency (for Isolation testing)[2,3]	Yes	Yes	AABUS

Note 1. See 5.1.2.
Note 2. Default minimum of 1.27 mm [0.050 in] or AABUS.
Note 3. Includes horizontal and/or line of sight adjacency; vertical adjacency is not required unless specified.
Note 4. For referee purposes, 0.5Ω maximum for each 25.0 mm [0.984 in] of circuit length **shall** apply.

Table 1.

Electrical Continuity and Isolation Resistance	3.8.2	Net List Testing - 250 Vdc - 100 Megohms Min	IPC-9252
Continuity	3.8.2.1	Net List Testing - 250 Vdc - 10 Ohms Max	IPC-9252 & IPC-2221
Isolation Resistance	3.8.2.2	Net List Testing - 250 Vdc - 100 Megohms Min	IPC-9252

Table 2.

having a length exceeding 500 mm (19.68 in.). Compounding this is that some OEMs not only want Class 3, but continuity resistance to not exceed 5 ohms and have net lengths in their board exceeding 750 mm (29.53 in.). This usually leads to delays in final inspection and/or shipping of product until a waiver or master drawing deviation is obtained.

In future months I'll be talking about a number of subjects pertinent to testing including military specifications vis-à-vis electrical test. I will cover the test requirements in specifications 31032, 50884 and 55110.

Meanwhile if you have any questions please don't hesitate to contact me, and as always, I welcome you to put me to the test. **PCB**

Todd Kolmodin is the vice president of quality for Gardien Services USA, and an expert in electrical test and reliability issues. His new column, Testing Todd, now appears monthly in *The PCB Magazine.* To contact Kolmodin, click here.

PCB007 Market News Highlights

U.S. Circuit Board & Component Manufacturing Report

Despite revenue declines in almost every year of the five years leading up to 2014, robust growth in 2010, due to a rebound in demand, led to an expected average annual growth of 1.6%; however, revenue is still expected to decline 2.7% in 2014, hitting $43.9 billion.

February Conference Board Employment Trends Index Up

"February's job report and the ongoing improvement in the Employment Trends Index should provide some relief for those concerned about weakness in the U.S. economy and labor market," said Gad Levanon, director of Macroeconomic Research at The Conference Board. "The majority of the ETI's components have been steadily rising in recent months, suggesting solid job growth will continue in the coming months."

Healthcare Cloud Computing Market: $6.5B by 2018

This report studies the North American healthcare cloud computing market over the forecast period of 2013 to 2018. This market was valued at $1,750.4 million in 2013 and is poised to grow at a CAGR of 29.8% from 2013 to 2018, to reach $6,459.0 million by 2018.

Global 3D Printing Market: CAGR of 16.8% by 2019

According to a new market report published by Transparency Market Research Global 3D printing (Polyjet, FDM, SLS, SLA) Market–Industry Analysis, Size, Share, Growth, Trends, and Forecast, 2013–2019, the global 3D printing market was worth US $2,200 million in 2012 and is expected to reach US $7,240 million in 2019.

Mobile DRAM Revenue Down Slightly in 4Q13

The mobile memory industry's worldwide revenue reached $3.039 billion in the fourth quarter of 2013, bringing the yearly total to $11.826 billion, representing 34.3% of DRAM industry value. Looking ahead to the first quarter of 2014, a 7.4% QoQ decrease in smartphone shipments is forecast, while tablet sales are expected to be weak as well.

3D Printing Market Experiencing Rapid Growth

The 3D printing market has seen rapid growth in recent years due to its increasing applications across different sectors such as consumer products and electronics, automotive, medical, industrial, and aerospace. Decreasing cost of 3D printers and its increasing adoption across the government and education sectors is further expected to spur the demand in the coming years.

IDC: PC Shipments See Continued Decline Through 2018

Worldwide PC shipments fell by -9.8% in 2013, slightly better than a projected decline of -10.1%, but still the most severe contraction on record, according to the International Data Corporation (IDC) Worldwide Quarterly PC Tracker. Fourth quarter results were slightly better than expected, but the outlook for emerging markets has deteriorated as competition from other devices and economic pressures mount.

Wearable Devices Market to Reach $30.2B in 2018

BCC Research reveals in its new report, Wearable Computing: Technologies, Applications, and Global Markets, the global market for wearable computing devices is expected to grow to $30.2 billion by 2018, with a five-year compound annual growth rate (CAGR) of 43.4%.

Growth of 65% for Digital Power Supplies & Power ICs

The global market for digital power is undergoing explosive growth, with revenues for digital power supplies and digital power integrated circuits (ICs) each projected to jump almost 65% in 2014, according to a new report from IHS Technology.

Global Lithium-Ion Battery Market Soars to $24.2B

Lithium-ion battery is used in a variety of markets, such as consumer electronics, automotive, and industrial. The prime drivers of the market are growing demand of electronic products, automotive vehicles, etc. Trends are favorable for growth across the industry; however, significant differences in growth potential among the application markets and regions exist.

ADVANCEMENTS IN THERMAL MANAGEMENT 2014

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PRELIMINARY PROGRAM ANNOUNCED

The Advancements in Thermal Management Conference has announced its preliminary program. These sessions will cover the latest advancements in phase change materials, LED cooling, graphene heat spreaders, compressed air cooling, thermal interface materials, thermal imaging, and much more.

Advancements in Thermal Management 2014 Presentations Include :

- Thermal Conductivity Measurement Methods, Comparison and Innovation for Advancing Graphene-Based Heat Spreaders - Academia Sinica
- Beyond Heat Spreading: Boosting Smartphone Performance through Phase Change Materials - Henkel Electronics Materials
- High Performance Low Pressure Compressed Air Cooling: A New Possibility - Alternative Engineering Solutions
- Advanced Thermal Interface Materials for Z-direction Thermal Dissipation of Extreme Heat Load in Electronic Devices - American Standard Circuits
- Passive Thermal Management of Lithium-ion Batteries using Phase Change Materials - Outlast Technologies
- Thermal Conductive Materials and LED Cooling - Fabrico
- Thermal Imaging Measurements of Low Emissivity Targets: A New and Novel Approach - FLIR
- Thermally Conductive Materials for LED Luminaire Optimization - C-Therm Technologies
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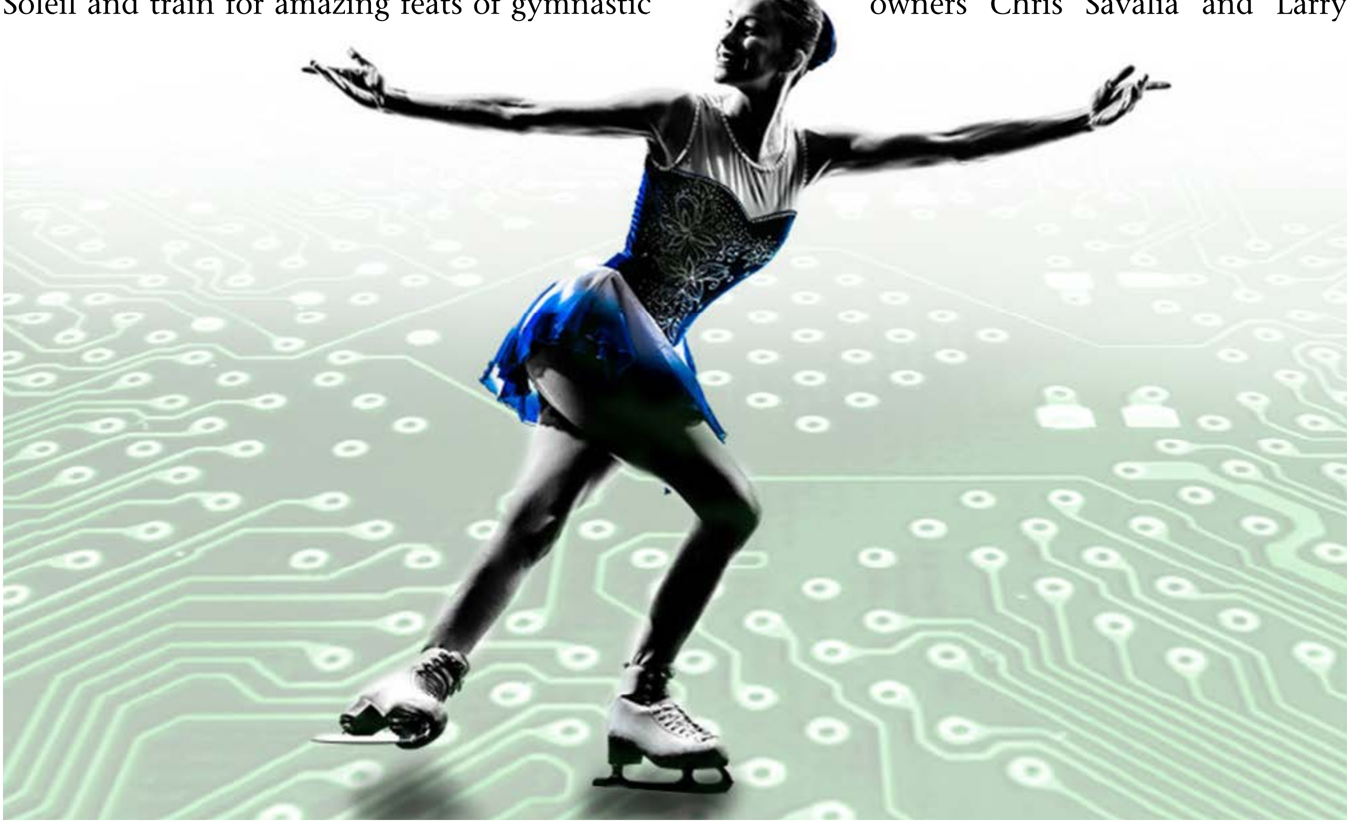
The Conundrum of RF/Microwave and High-Performance PCBs

by Judy Warner
TRANSLINE TECH

I watched the Olympics with my husband and two college-aged daughters, paying particular attention to the women's snowboarding, ice skating and ice dancing competitions. Because our nest will soon be empty, I was feeling nostalgic and thinking about what it was like to be a teen girl watching the Olympics with my parents (good times!). I was amazed how dramatically each sport has progressed since then. Snowboarding didn't even exist,, and I remember holding my breath to see if Olympic ice skaters could actually land a triple Lutz, which many believed impossible. Now, Shaun White is a household name and triple Lutzes are commonplace. Ice dancing used to be very theatrical and a little goofy, at least in my teenage mind. Today, ice dancers work with Cirque du Soleil and train for amazing feats of gymnastic holds, lifts and spins. The human spirit is amazing, breaking limits that were once thought unbreakable.

We in the PCB industry know a lot about this transcendent spirit, don't we? As demand for smaller lines, smaller holes, better tools, equipment and chemistry increases, we always find ways to meet or even exceed demand. I would contend that we have a proud history of breaking barriers! This is certainly true when it comes to RF/microwave and high-performance boards. We have a saying about these types of boards: "They are not always complex, but they are always difficult!" We specialize in these types of boards and have found they require a unique set of skills and expertise to make. In fact, I have fondly nicknamed company owners Chris Savalia and Larry



Padmani the "Cowboys," because they continually head into uncharted technological territory to meet our customer's needs. Despite our pioneering spirits, however, I find myself wondering about where we can go from here to meet ever-increasing speeds and ever-lowering tolerances that can't be held consistently due to the inherent limitations of the PCB manufacturing process. Let's face it, even on a good day, neither plating nor etching is an exact science—which is why there are tolerances in the first place. With increasing frequency I am asked if we can hold line width/spacing to 1 mil tolerance or less. The speed of the chips running on these boards is screaming fast and the laminate, finishes, conductors and connectors are slowing these racehorses down. Engineers are searching everywhere possible to eke out a little more speed or performance. Meanwhile, every point along the supply chain is looking to save a buck. So in short—people want unprecedented precision, consistently and dirt cheap!

"Engineers are searching everywhere possible to eke out a little more speed or performance. Meanwhile, every point along the supply chain is looking to save a buck. So in short—people want unprecedented precision, consistently and dirt cheap!"

After I blogged about this issue recently, a retired engineer said he could achieve those tolerances 30 years ago and wondered why things hadn't progressed. Well, he was referring to a time when he worked for a large R&D company that had an almost limitless budget and a small army of engineers to make that happen. They developed custom tools and equipment.. As we all know, those days are sadly gone and progress is certainly impeded by today's limited budgets.

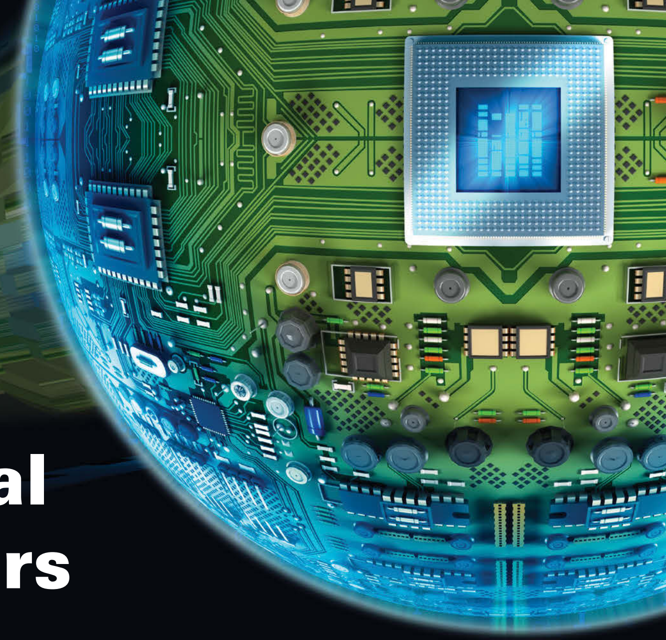
Laminate manufacturers, like Rogers Corp. and Taconic, who make advance circuit materials for high-speed applications, continually advance in producing lower-loss materials, bond ply and adhesives. Progress is also being made on connectors and points of connection to allow signals to flow freely. Currently, it seems like PCB fabricators are the weakest link—constrained by the limits of the manufacturing process itself.

I believe part of the solution may lie in a closer working relationship between designers and their board suppliers. When a designer thoroughly understands the manufacturing process, adjustments can be made during the design phase, which may aid in reliability, consistency and price. Due to economic constraints, many RF engineers are being called upon to lay out their boards without the help of a formally trained PCB designer. Some of these individuals understand the manufacturing process, and some do not. This creates a disconnect between the intent of the design and the realities of board fabrication. Due to the current state of the industry, we are all being called upon to wear more hats—putting a strain on time and available funds. However, the investment in collaborative time is crucial to long term success and cost control.

The demand for RF/microwave and high-performance boards is growing on both the commercial and military front. It seems to me that we are ripe for some breakthroughs that will enable us to produce boards that will aid, rather than hold back, the current generation of high speed chips. Perhaps technologies such as 3D printing will become a viable solution down the road.

Whatever the case may be, I am sure we will one day look back with nostalgia, as I now do the Olympics. Then we will recall these days in which we faced these obstacles, transcended them and then pulled off our own version of a perfect triple Lutz. **PCB**

Judy Warner is the director of sales and marketing for Transline Technology, a PCB manufacturer specializing in RF and microwave applications in Anaheim California. To contact Warner, or to read past columns, click here.



TOP TEN

PCB007 News Highlights This Month

① MFLEX Announces Restructuring Plan

Following a full review of its manufacturing footprint and in an effort to realign its manufacturing capacity and costs with expected revenues, MFLEX is consolidating its production facilities to reduce the total manufacturing floor space by approximately one-third.

② IPC: N.A. PCB B2B Ratio Improves, Sales Lag

"January is typically a slow month in electronics manufacturing, especially compared to December, but this winter the industry may also be feeling the effects of weather-related slowdowns," said Sharon Starr, IPC's director of market research. "The good news is that the book-to-bill ratio continued to climb in January."

③ IPC: Flexible Metal-clad Dielectric Materials Standard

This standard establishes the classification system, the qualification and quality performance requirements for flexible metal-clad dielectric materials to be used for the fabrication of flexible printed circuitry and flexible flat cable.

④ FPCB Market Expected to Reach $12B in 2014

The global flexible printed circuit board (FPCB) market valued US $11.321 billion with a YoY growth rate of 9.4% in 2013, and will be worth US $12.008 billion in 2014 and US $12.686 billion in 2015.

5 Sunstone Circuits Announces On-Time Guarantee

"With this On-Time Guarantee, Sunstone continues to lead the industry by putting the design engineer in control, the way that it should be. Our customers now know that they will have their high quality PCBs in hand on time, or they are 100% free, plain and simple," said CEO Terry Heilman.

6 Newbury Electronics Installs UK's First UV-P300 LDI

The new machine, a UV-P300 LDI, is manufactured by Limata, and uses the latest in laser technology to produce far more technically demanding PCBs than could be achieved using the more traditional photo lithographic techniques. It is the first machine of this type to be installed in the country.

7 Ray Young Appointed GM of Ventec USA's CA Division

Ventec USA is delighted to announce the appointment of Ray Young as general manager of its California operation. He brings with him over 40 years' experience in PCB manufacture at all levels from hands-on processing through plant management and general management to senior operations executive roles in industry-leading companies supplying the high-technology, high-reliability electronics industry.

8 i3 Electronics Achieves Critical Re-certifications

"The company has a strong Quality Management System, and is committed to the delivery of on-time, high-quality products to meet our customer demands. These re-certifications are a reflection of the dedication of all i3 associates to our Quality System. We are incredibly pleased to have received these certifications with no non-conformances," stated Robert Nead, president.

9 Cicor's PCB Division Reports Positive 2013 Results

Cicor which is headquartered in Boudry, Switzerland, looks back upon a successful 2013. The Group increased its order intake in 2013 by 16.5% to CHF 20 1.7 million. Net revenues for 2013 were CHF 190.5 million (2012: CHF 176.0 million), representing an increase of 8.2% over the previous year.

10 WEdirekt Online PCB Shop Achieves Over 40% Growth

With strong revenue growth WEdirekt, the online circuit boards store at Wurth Elektronik has managed an extremely successful year in 2013. Carina Harnisch, the head of WEdirekt, has developed ideas and targets for 2014 to increase this success even further.

CALENDAR

EVENTS

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar of Events, click here.

For a complete listing, check out PCB007's full events calendar.

South East Asia Technical Conference on Electronics Assembly
April 8–10, 2014
Penang, Malaysia

Intermountain (Boise) Expo & TechForum
April 17, 2014
Boise, Idaho

Smart Fabrics & Wearable Technology 2014
April 23–25, 2014
San Francisco, California, USA

NEPCON China 2014
April 23–25, 2014
Shanghai, China

Nordic SI Week 2014
May 5–9, 2014
Stockholm, Sweden

Atlanta 18th Annual Expo
May 7, 2014
Duluth, Georgia, USA

International Conference on Soldering and Reliability
May 13–15, 2014
Toronto, Ontario, Canada

Toronto SMTA Expo & Tech Forum
May 15, 2014
Toronto, Ontario, Canada

12th Annual MEPTEC MEMS Technology Symposium
May 22, 2014
San Jose, California, USA

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