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REWORK, MODIFICATION AND REPAIR

Advanced Rework Technology & Processes for Next-Gen Packages

by Brian Czaplicki—page 16

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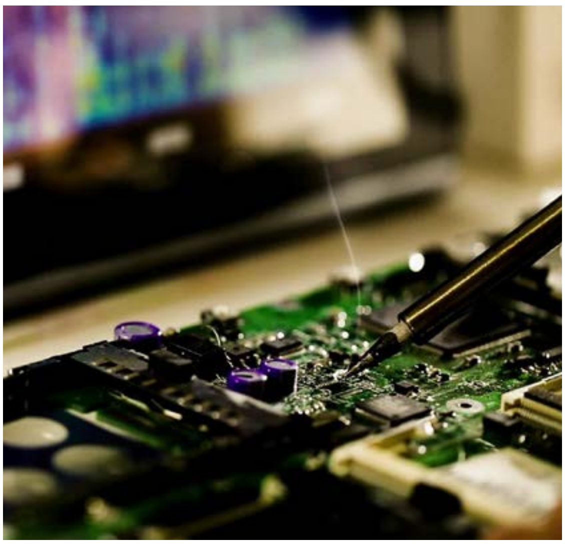
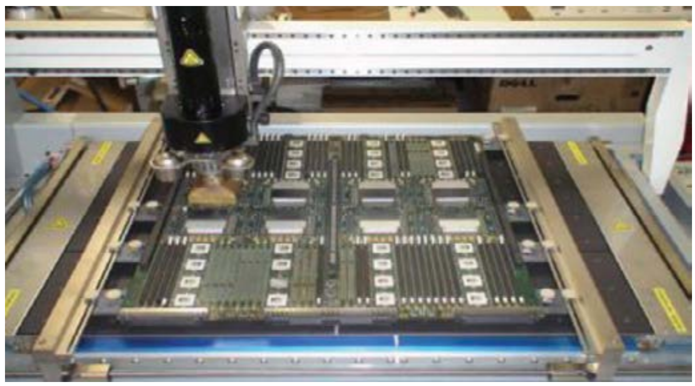
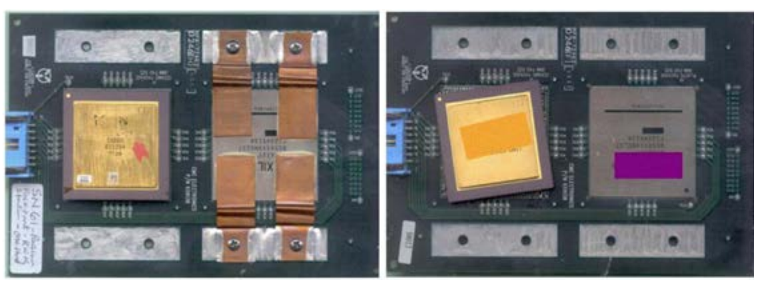
November 2013 Featured Content

REWORK, MODIFICATION & REPAIR

The repair of packages is a necessary evil. And the rework and repair of advanced packages is becoming increasingly complex, not to mention expensive. This month, our veteran contributors explore the ins and outs of repairing packages such as large area arrays and column grid array assemblies.







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THE WAY I SEE IT

The Summit

by Ray Rasmussen
PUBLISHER, I-CONNECT007

What's 20x more conductive than copper, 100–300x stronger than steel (depending on whom you ask) and possibly harder than diamond? What has great thermal conductivity, tremendous surface area and has researchers around the globe working day and night to develop the next generation of products? It's graphene.

Rediscovered in 2004 by physicists at the University of Manchester and the Institute for Microelectronics Technology, Chernogolvoka, Russia, this amazing material has moved from labs around the world into volume production. Still in its infancy, graphene is being used for a whole host of products today and proposed and developed for myriad products of the future.

Did you know that a sheet of graphene as thin as a piece of plastic wrap could support the weight of an elephant? We learned this from a technologist who is working with this wonder material, MIT Professor Tomas Palacios, at IPC's recent TMRC meeting in Chicago. His presentation, along with a few conversations during the meeting, got me thinking about the possibilities.

On the PCB side of things, what's the biggest issue we face? After listening to a ton of presentations over the years, I'd say it revolves around laminates. The drive to thinner, lighter, more functionally capable laminates that won't come apart when wave soldered, is on everyone's list of requirements. How can we make much finer

lines and spaces, get much thinner and still retain the electrical properties we need for today and tomorrow's products?

That's where I am with graphene. I've been reading about it since its discovery and we've published nearly 400 articles related specifically to this material over the years, so I've followed what's been developing.

The Next Generation of PCB Materials

I try to attend as many industry conferences as I can. I've noticed that everyone's making incremental changes to their materials or processes to improve the PCBs or assemblies we produce. No one's really seeking out that game-changing technology (save Joe Fjelstad's Occam Process) which would move the industry to another plateau. Not being a scientist or an engineer, I can only react to what I read from some really smart people. Maybe that's my advantage, or maybe I'm a bit naive. I don't know why it can't be done, so I only think of the possibilities.

> *I don't have all the answers, but that shouldn't hold us back. This material has way too many phenomenal characteristics, which address many of the pain points our customers have. I think it makes sense to take a look, think about and discuss the possibilities.*

As mentioned, graphene is highly electrically conductive, a great heat conductor (5000 W/MK), very strong and just one atom thick. Now, add in four-atom-thick nano-insulating materials that Palacios discussed in his presentation, along with carbon nanotube solder (SAC 305 paste is already being made with carbon nanotubes) and we may have a platform for next-generation electronics.

I don't know a lot about these new materials but I believe the following represents a few more of the characteristics.

- Fireproof (no need for flame retardants)
- Little or no moisture absorption
- CAF problem solved
- Resistance—smaller lines not a problem
- Giant heat sink
- Heat tolerant (won't delaminate)
- Nano insulating materials available
- Great surface area (good adhesion)
- Potential to be extremely thin
- Stretchable/bendable
- Lightweight
- Almost no CTE issues
- Highly durable solder joints that won't crack

Now, I'm sure there are some drawbacks. How will we make the circuits or vias on this new material? It's at least as hard as diamond and a lot stronger than steel. How will we solder to it (already being done in the lab)? I don't have all the answers, but that shouldn't hold us back. This material has way too many phenomenal characteristics, which address many of the pain points our customers have. I think it makes sense to take a look, think about and discuss the possibilities.

In order to not look too foolish before publishing this piece, I consulted a few industry experts to see if what I am suggesting makes sense. I queried my friend, Joe Fjelstad, who then suggested I get some feedback from Dr. Alan Rae. Here's what they both had to say.

Rae: There are definitely real opportunities for graphene in circuit board manufacture—in fact I had a conversation very recently with a board materials manufacturer. There is lots of work to do to get it to work. Graphene can be printed or chemical vapor deposition (CVD) on epoxy or other substrates, but will not etch easily. It will need an additive process. Good thermal and electrical conductivity in plane, and out of plane connections could be made with silver inks, for example (iimak is already making silver-graphene inks). So I can actually envision a system—even roll to roll—that might work well, but the board contacts and component attach details need a lot of thought even before we start thinking about reliability.

Fjelstad: Thanks to you both for sharing your thoughts. This is the way we progress. Personally I am still 'on the dock' on this subject. Every sailboat needs a sail, a tiller, an anchor and a skilled sailor who (hopefully) knows the waters. Moreover, every journey of interest requires us to leave the safety of the harbor.

Academics often tend to be highly exuberant about their research. Which, extended to the metaphor, means they are often excellent sails but unfortunately they also often lack sailing skills and knowledge of the waters (experience on the manufacturing floor).

The result has often taken us off course (though, clearly we have visited places of future interest as a result). Presently, processing of graphene appears to be still a largely "uncharted sea." It will be interesting to see what happens. One can only hope they don't start selling a lot of tickets before they prove the journey is safely navigable.

The Graphene Summit

So, what do we do about this? We can watch the world race forward to develop new capabilities for industries around the globe and do nothing or we can grab hold of the opportunity this material offers and change our world. I do know that most of us prefer to let things evolve at their natural pace. If graphene has a place in the industry, it will come, someday. To borrow a term I love from Dr. Nakahara (Naka), I say, "bullshit nonsense." There's too much at stake to allow others to drive the future of our industry.

Please don't take this the wrong way. I do believe that materials companies are working very hard, making tweaks to improve their products, producing laminates that are a bit thinner, a bit better heat conductors, a better conductor of electricity, etc. It's an ongoing, never-ending introduction of material sets designed to offer solutions, but they never quite get to where they need to be. They make things better, but they don't necessarily solve the problem since OEMs continue to push technologies to the limit to build the products of tomorrow. With graphene, we might very well be able jump ahead of the curve and give them something they don't expect: a new way to build their products entirely based on graphene PCB technology. Wouldn't that be cool? We can give them the PCBs of tomorrow, today (or, as soon as we can develop the materials and processes needed).

Here's what I propose: a summit in the form of a conference open to all. I hope it could be an IPC or iNEMi gig, but if not, I'd be willing to host it.

At the conference, we can at least talk about the possibilities of using this amazing material to provide the interconnection technology of the future. I know most suppliers are looking at and playing around with graphene in their labs, but we need a game-changing material which will give our customers, the OEMs, the solutions they're looking for. After we meet, if it still makes sense to move forward, some task groups can be formed to explore the possibilities.

What I would hope to come away with after we've heard from the experts (research scientists, supplier CTOs, etc.) is whether graphene can truly be a game-changer for our industry. If it can, then we need to grab and run with it.

Speaking of conferences, I'll be at Graphene Live, Printed Electronics USA later this month in Santa Clara. Drop me a note if you'd like to meet. **SMT**

Some additional reading on the topic:

- Understanding Interface Properties of Graphene Paves Way for New Applications
- Researchers find chemical process for creating holes in graphene oxide
- Graphene Overview—Wikipedia
- "White graphene" halts rust in high temperatures

Ray Rasmussen is the publisher and chief editor for I-Connect007 Publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine.* To read past columns, or to contact Rasmussen, click here.

SMT PERSPECTIVES & PROSPECTS

Tin Whiskers: Concerns and Potential Impact

by Dr. Jennie S. Hwang
CEO, H-TECHNOLOGIES GROUP

To view other articles in this multi-part series on tin whiskers, click here.

What is the biggest concern about the growth of tin whiskers? A simple answer is the "uncertainty."

Electronic system failures attributing to or related to whiskers have been reported in the past before the electronics industry was converted to lead-free. With the elimination of the use of lead (Pb) in electronics in compliance with worldwide RoHS regulations, Pb-free materials including pure tin (Sn) have been used as surface coating for component leads and metal terminals, and as solder materials in making solder joints.

Pure tin makes a practical replacement to Sn-Pb as a choice of surface coating because of its economics, availability and performance in manufacturability, compatibility and solderability. Today, most component manufacturers offer pure tin-coated components.

On electronic system failure, as an illustration, one of the well-studied and highly publicized incidents was the TOYOTA Camry 2003 model investigation. The unintended acceleration of the vehicle speed control was reported in 2009. National Highway Traffic Safety Administration (NHTSA) initiated an investigation with the technical support of NASA Engineering and Safety Center. Destructive physical analysis of a failed accelerator pedal position sensor assembly from a consumer vehicle that was identified with a diagnostic trouble code found the presence of tin whiskers. A tin whisker had formed a 248 Ω resistive short between two terminals of the accelerator pedal position sensor of its potentiometer accelerator pedal assembly. A second tin whisker of similar length grew from a 5-volt source terminal adjacent to a pedal signal output terminal, but this whisker did not make contact with any other terminals at the time of the analysis.

In this potentiometer accelerator pedal assembly, the terminal leads were made of a copper alloy coated with 2 µm of pure tin. The separation between adjacent terminals was in the range of 1000–1500 µm.

Electrical tests of the failed unit confirmed intermittent resistance behavior—from the initial 3.5 MΩ, dropping to 5 kΩ, and then remaining between 238 Ω–250 Ω, until the pedal assembly was mechanically shocked. Mechanical shock to the pedal assembly returned the resistance to 3.5 MΩ and further pedal actuations dropped the resistance again to 5 kΩ and finally to the range between 238 Ω and 250 Ω. These symptoms were attributed to the presence of tin whiskers.

This shorting resistance remained unchanged throughout the entire range of the travel of the pedal, except when mechanical shocks were delivered. Inspection of the as-identified "non-failed" potentiometer pedals revealed tin whiskers present in similar locations as the failed pedal. The thickness of the bridging whisker is calculated to be approximately 1.7 µm, based on its length (1.9 mm), electrical resistance (240 Ω), and the electrical properties of tin. The electrical current needed to melt a whisker of this length and thickness in air was reported to be approximately 5 mA.

This study indicated that tin whiskers did grow from the tin-coated copper-alloy terminal leads and the whiskers did result in intermittent resistive short in the accelerator pedal position sensor of a 2003 Toyota Camry.

With the above illustration, if/when tin whisker occurs, what are likely sources of uncertainty or potential adverse impact? Concerns and impact primarily fall in the following four categories:

1. Short circuits

When a whisker grows to a length that bridges the adjacent lead or terminal, this conductive whisker causes an electrical short. However, if a whisker is formed but does not bridge its neighbor, there will not be an electrical short. To complicate the phenomena, there are occasions where whiskers may not cause failure or a failure may not be detected even when the whisker physically touches the adjacent lead due to lack of electrical current flow. This could occur when an insulating surface film is formed on whiskers as the result of oxidation or the formation of other insulating compounds on the whisker surface. The relative magnitude of the applied voltage of the detecting ohm-meter and the dielectric breakdown strength of the insulating film determines the detectability of failure. Additionally, although the whisker may grow with time, it may also diminish when/if the electric current can fuse (melt) it. In this case, tin whiskers may not create a "permanent" short, but rather a transient malfunction. This self-annihilating ability further contributes to the elusive behavior of tin whisker.

"When a whisker grows to a length that bridges the adjacent lead or terminal, this conductive whisker causes an electrical short. However, if a whisker is formed but does not bridge its neighbor, there will not be an electrical short. To complicate the phenomena, there are occasions where whiskers may not cause failure or a failure may not be detected even when the whisker physically touches the adjacent lead due to lack of electrical current flow."

2. Tin metal arcing

Under high level of current and voltage that is able to vaporize the whisker and ionize the metal gas, metal arc can occur. Reportedly, tin whisker arc was demonstrated at supply voltage of 13 volts and supply current at 15 amps at atmospheric pressures of about 150 torr. The level of driving forces required to drive the arc decreases with the reduced pressure. A NASA report attributed a satellite failure to tin metal vapor arc as the suspected root cause. It is expected that tin arc is more likely under reduced atmospheric pressures or vacuum environments.

3. Break-off debris

The whiskers, being brittle and conductive in nature, can break off from its base of coating surface, which may create functional issues. This is particularly a concern for sensitive electronic devices, such as optical and computer disk driver applications. The break-off behavior varies with the service conditions and the characteristics of the whisker.

4. Unwanted antenna

Tin whiskers can act like miniature antennas, which affect the circuit impedance and cause reflections.

In this case, the most affected areas are in high-frequency applications (higher than 6 GHz) or in fast digital circuits.

Overall, long, brittle and needle-shaped whiskers are potentially more harmful than those in mould and nodule shapes.

The above potential impact of tin whiskers is "known knowns." Nonetheless, the "known unknowns," such as specific external conditions, application environment either during service or during testing, and the uncertainty of tin whiskers remains to be inevitable.

Stock markets do not like uncertainty, nor do electronics. Our effort is to minimize uncertainty, which will be discussed in the upcoming columns of this series on tin whiskers. **SMT**

Dr. Hwang, a pioneer and long-standing contributor to SMT manufacturing since its inception, as well as to the lead-free development and implementation, has helped improve production yield and solved challenging reliability issues. Among her many awards and honors, she is inducted to the WIT International Hall of Fame, elected to the National Academy of Engineering, and named an R&D-Stars-to-Watch. Having held senior executive positions with Lockheed Martin Corp., Sherwin Williams Co., SCM Corp, IEM Corp., she is currently CEO of H-Technologies Group providing business, technology and manufacturing solutions. She has served on U.S. Commerce Department's Export Council, various national panels/committees, the board of Fortune 500 NYSE companies, and various civic and university boards. She is the author of 350+ publications and several textbooks, and an international speaker and author on trade, business, education, and social issues. Her formal education includes four academic degrees as well as Harvard Business School Executive Program and Columbia University Corporate Governance Program. For further info, visit www.JennieHwang.com. To read past columns, click here.

Video Interview

Medical RoHS Exemption Ends in 2014

by Real Time with... SMTAI

The EU's medical exemption for RoHS ends in July 2014. But Dr. Ron Lasky of Indium has a recommendation for a high-rel lead-free solder: SACM, which includes manganese.

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Advanced Rework Technology and Processes for Next-Gen Packages

by Brian Czaplicki
AIR VAC ENGINEERING CO.

SUMMARY: What are the next set of challenges that will need to be addressed regarding area array and SMT rework? This article discusses the five rework gaps identified by iNEMI, and the associated technical and process challenges.

Abstract

BGA rework is now largely mature, although new supplemental processes that provide improved process control such as solder paste dipping and non-contact site cleaning can now be integrated into existing processes if the rework technology that is used allows.

So, what is the next set of challenges that will need to be addressed in regard to area array and SMT rework? The International Electronics Manufacturing Initiative (iNEMI) has recently published its 2013 Technology Roadmap for the global electronics industry which includes a section dedicated specifically to rework and repair. Of particular interest and importance is iNEMI's gap analysis which identifies future specific gaps and challenges that will result from such factors as government regulations, disruptive technologies and new product requirements.

This article will review five of the key rework gaps and challenges identified by iNEMI including:

1) Reworking very large, next-generation area arrays on large high-thermal-mass assemblies

2) Development of hand-soldering processes for reworking 01005 components

3) Development of industry-standardized processes for reworking package-on-package (PoP) devices

4) Development of industry-standardized processes for reworking quad flat, no lead (QFN) devices

5) Development of site redressing processes that prevent lifted pads, soldermask damage and copper dissolution[1]

This article will discuss the five iNEMI rework gaps and challenges including identification of the key technical/process challenges, outlining in detail the efforts-to-date aimed at addressing these new challenges as well as the next steps required for complete resolution of these challenges.

Introduction

The five major rework gaps and challenges identified in the rework and repair section of the 2013 iNEMI Technology Roadmap requires a combination of new thinking, new and innovative technology and a lot of good old fashioned hard work.

BGA rework systems, which have successfully handled the requirement to rework lead-free BGAs for 10-plus years will now be required to handle a number of new technical challenges including the ability to align next-generation extra-large (70–100 mm), high I/O (>1000) components as well as having the thermal capacity to reflow these large components while meeting the current stringent standards for both maximum package temperature and the maximum joint temperature Delta which are based on much smaller, current generation components. Other machine/process challenges related to next-generation large devices will include such "simple" things as vacuum-holding capability as well as more complicated issues such as component warpage and site preparation. In addition, these XXL components will most often be found on very large, high-thermal-mass assemblies for server, telecommunications and networking applications which means that the BGA rework system must also have the capability to hold and preheat these very large, high-thermal-mass assemblies.

BGA rework systems will also be required to handle new challenges associated with PoP rework including controlled solder paste/flux dipping, the accuracy to place 0.3–0.4 mm pitch devices and the force control necessary to place a dipped top device on an unreflowed bottom device so both packages can be reflowed together. QFN rework requires the integration of pasted or pre-pasted and reflowed devices as well as the process know-how to control voiding in the center ground pad area.

The rework industry's reluctance to replace wick-based site redressing with non-contact methods is beginning to change. The industry's view of solder wick as a fast and easy solution for preparing a site must be tempered by the fact that wick-based cleaning lacks process control, thereby subjecting the PCB to a higher potential incidence of pad or soldermask damage.

The pros and cons of various flux/paste application methods including dipping, paste-on-device, paste-on-board, stay-in-place stencils and multi-up stencils are reviewed and summarized.

Finally, the topic of 01005 rework is analyzed in detail including the potential use of hand tools, BGA rework systems and combined (man/machine) technology systems.

Next-Generation Large Area Array Rework

Some of the largest area arrays in use today include CCGAs, as well as BGA sockets and connectors with lead patterns approaching 50 mm. iNEMI forecasts component sizes of 60–75 mm; however, future rework requirements for 80–90 mm components have already begun to surface.

These next-generation large area arrays may have high-thermal-mass issues such as metal BGA sockets. Further complicating this issue is the fact that these large, thermally challenging devices will typically be found on large, high-thermal-mass PCBs.

Soldering Process	Parameter	Units	2011	2013	2015	2017	2023
Pb-free	Maximum package sizes	mm	50	50	55	60	75
	Maximum package temperature (dependent on component body size)	°C	245-260	245-260	245-260	245-260	245-260
	Target solder joint temperature	°C	235	235	235	235	235
	Target delta T across solder joints	°C	<10	<10	<10	<10	<10
	Time Above Liquidus (TAL)	Sec	60-90	60-90	60-90	60-90	60-90

Table 1: Large area array rework[2].

		Max Temp (°)		Delta T (°)		TAL (sec)	
TC #	Location	Actual	Spec	Actual	Spec	Actual	Spec
1	Top of Package	260	260		-	-	-
2	Joint (corner)	235	235	6	< 10	52	60-90
3	Joint (corner)	235				55	
4	Joint (corner)	239				72	
5	Joint (corner)	238				68	
6	Joint (corner)	237				69	
7	Joint (corner)	241				75	

Table 2: 114 mm BGA (Ph 150°C, 495C @ 2.5 scfm, 150 sec).

iNEMI's major concern is the ability to reflow these next-generation large devices on large, high-thermal-mass PCBs based on the current stringent specifications as shown in Table 1.

The challenge is that next-generation area arrays will increase in size by 50–100% and will typically be found on large, high-thermal mass PCBs. But, the reflow specifications are the same as for today's standard BGAs.

Large Area Array Thermal Profiling

A 114 mm (4.5") square BGA with 10,000 I/O was thermally profiled. Seven thermocouples (TCs) were used to instrument the test vehicle. Six TCs measured joint temperature and one measured package temperature. The PCB was the same size as the device, so preheating the joints to 150°C represented the board preheat stage.

Significant development effort was done in regard to optimizing the thermal distribution of the nozzle required for this very large device. The nozzle design is proprietary at the time of this writing and therefore cannot be photographed or illustrated in detail.

This extremely large device required significant thermal energy and time to reflow it. The PCB was preheated to 150°C with a high-power, indirect IR bottom heater. The top heater setting after preheat was 495°C at 2.5 scfm flow for 150 seconds. The top heater setting of 495° is very high compared to the 300–325°C setting typically used for BGAs. But the large size of the component and the nozzle required significantly more thermal energy. A board cooling system was used to cool the part down after reflow which is critical to achieving targeted time above liquidus (TAL). The results are shown in Table 2.

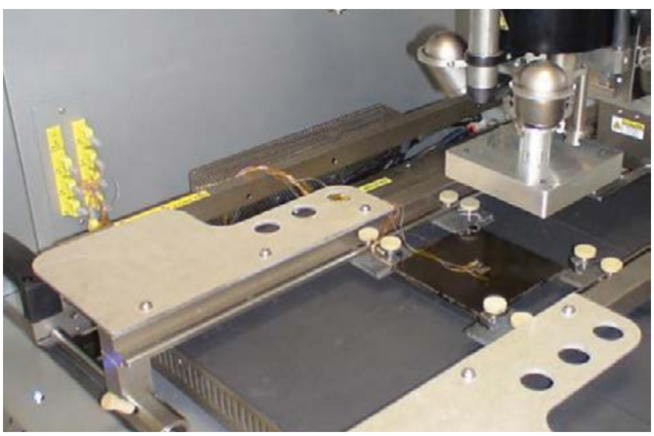

Figure 1: Instrumented 114 mm BGA on BGA rework system.

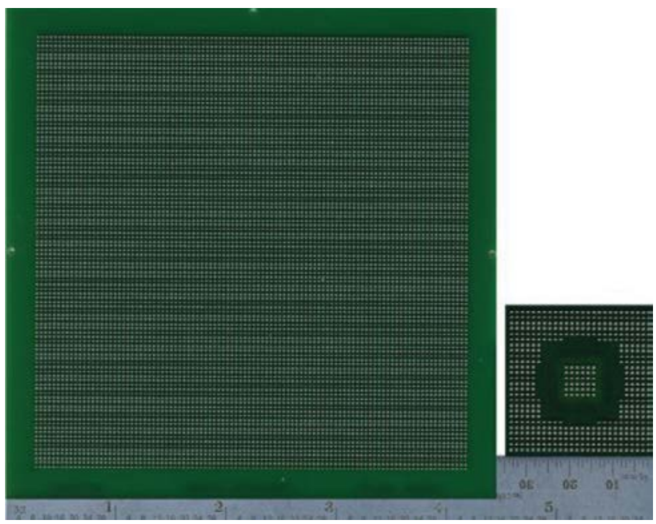

Figure 2: 114 mm BGA (10,000 I/O), with 35 mm BGA shown for scale.

		Max Temp (°)		Delta T (°)		TAL (sec)	
TC #	Location	Actual	Spec	Actual	Spec	Actual	Spec
1	Top of Package	250	260		-	-	-
2	Joint (corner)	240	235	6	< 10	75	60-90
3	Joint (corner)	240				78	
4	Joint (corner)	241				92	
5	Joint (corner)	241				88	
6	Joint (corner)	235				76	
7	Joint (corner)	239				86	

Table 3: 114 mm BGA (Ph 150°C, 350C @ 3.0 scfm, 167 sec).

All specifications were met except the TAL for two joints fell short of the target. The volume of air used to cool down the component can be easily reduced to correct this. The bigger issue, though, is that the maximum package temperature was 260°C, which leaves no margin for error.

A modification was made to the rework system that allowed significantly higher flow rates to be used. The thermal energy transferred to the component is a combination of temperature and flow so the higher the flow rate, the lower the temperature required. A low temperature/high flow approach typically reduces package temperature, but it can negatively impact the Delta T of the joints if the flow is too high, so the optimum balance of temperature and flow must be found for each application.

Increasing the gas flow from 2.5 scfm (current maximum) to 3.0 scfm (25% increase) allowed the nozzle heater temperature to be reduced from 495°C to 350°C (30% reduction). The results of the temperature and flow modification are shown in Table 3.

The lower temperature/higher flow approach reduced the maximum package temperature from 260°C to 250°C, well below the current guidelines with no negative impact on the delta T of the joints. All joints except one met the TAL target of 60–90 seconds using this approach.

It is important to note that the 114 mm BGA is attached to a 114 mm test board with no layers. The thermal settings required to reflow a device of this size on a large, high-thermal-mass assembly will be significantly higher. It will be critical for the BGA rework system to have the nozzle temperature/flow and board heating/cooling/handling capability required to rework these next-generation large devices on high-thermal-mass assemblies (Figure 3).

Next-generation large component technology will also provide additional challenges not cited by iNEMI including alignment capability, warpage issues, component/site preparation, large board handling capability and nozzle vacuum requirements. It is anticipated that the vision system on rework machines of the future must be able to align components at least up to 75 mm and perhaps as large as 100 mm or more (Figure 4). Warpage/coplanarity issues will be a major issue for next-generation large devices, especially as the pitch decreases over time. Non-contact site cleaning technology must include large size nozzles that provide safe, effective and fast cleaning of the residual site solder. Finally, the vacuum capability of the nozzle must be sufficient not only to hold large devices in place, but also to lift and remove them out of reflowed solder.

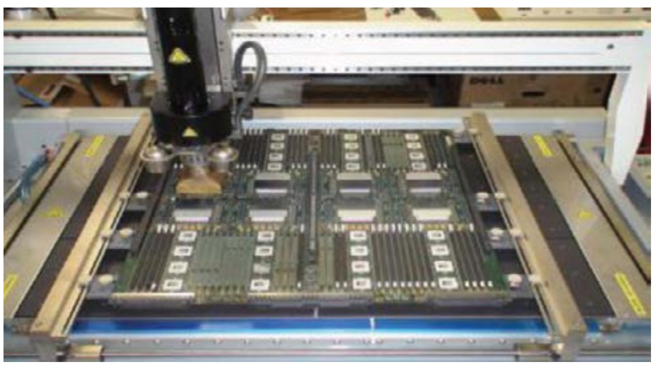

Figure 3: 22 x 24 high-thermal-mass PCB on large board rework system (board courtesy of IBM).

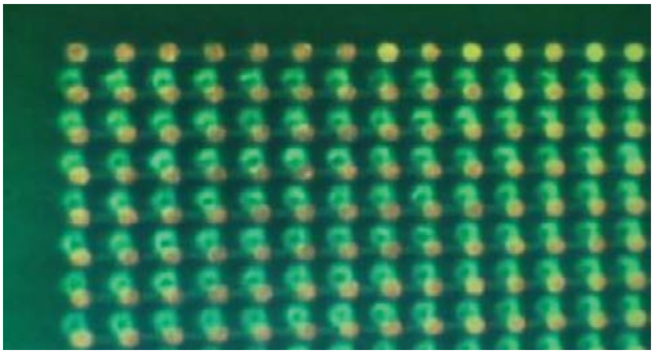

Figure 4: 114 mm BGA corner viewing in vision.

One major roadblock to the development of effective rework technology and processes for next-generation large devices on thermally challenging assemblies is access to and the cost of these devices and assemblies. Cooperative effort is needed between OEMs/CMs and rework equipment suppliers in this area to address the critical issues outlined above.

01005 Rework

Small enough to pass through the eye of a needle and multiple times smaller than a pepper flake, 01005s are nearly invisible to the human eye. These microscopic devices pose significant rework challenges including component handling, site preparation and reflow.

01005s are not yet used in widespread high volume production, but it is believed that current users are performing hand-soldering rework when required. iNEMI's view is that hand-soldering rework of 01005s is difficult but possible for a skilled operator.

These are conflicting industry views regarding 01005 rework with the majority of views indicating that 01005s cannot be reworked. On the other hand, manufacturers of both hand tools and BGA rework equipment indicate that they have equipment capable of reworking 01005s. Web-based research found several hand tools said to be capable of 01005 rework; no hand-tool-based video of 01005 rework was found. On the other hand, several 01005 rework videos were found using BGA rework machines, but many have limitations or issues including high capital cost, low throughput, lacking ease of use, and the ability to rework 01005s with adjacent spacing of 0.2 mm or less.

Figure 5: 01005 in eye of needle and next to pepper flakes.

Another issue is the inability of most machine-based systems to handle almost half of the cases where the residual site solder cannot be reused due to paste printing defects such as insufficient solder (Figure 6). Some rework machines do provide a paste dispensing capability, but the complexity and efficiency of dispensing microscopic dots in a repeatable fashion in a hot rework environment is a major concern.

One other alternative for 01005 rework is to combine the best features of hand-soldering and BGA-type machine rework into a man/machine rework interface (MMRI). In this approach, the operator has manual control of all processes, which are done directly at board level without using slower, more expensive and often complicated beamsplitter-based systems. The board level rework approach also eliminates Z-axis accuracy issues that exist with most beamsplitter-based systems. If the beamsplitter is not

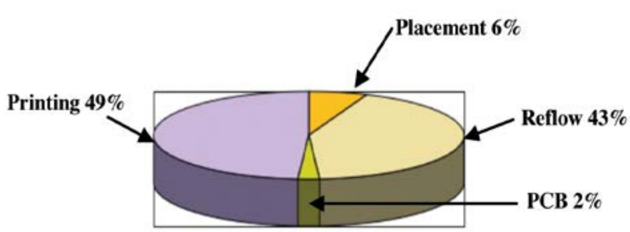

Figure 6: Root cause of defect.

calibrated accurately and often, the nozzle will not properly contact the 01005 during removal, and the positioning will be off during placement. In addition, some BGA rework systems do not have the accuracy necessary for placing micro-discretes regardless of how often the vision system is calibrated. Remember that we are talking about microscopic devices, so minor placement errors which had no impact in the past on BGA rework, now become significant.

In addition to manual control, the MMRI approach also provides the operator with numerous machine-related advantages, including inspection quality microscope- based optics, integrated top and bottom heating technology and perhaps most importantly, elimination of the precise manual dexterity required for hand-soldering rework. The 01005 removal throughput with the MMRI approach is multiple times faster than beamsplitter-based systems, and as fast as hand tools.

The 01005 replacement process is greatly simplified when the residual solder on the pads can be reused. A stereo microscope with high magnification zoom lens assists the operator in picking the replacement device from the tape holder, eliminating any manual handling of the part. The site is fluxed with a micro syringe to minimize over application of flux which is a key iNEMI concern. Indium 30B halide-free flux is used as it does not contribute any ionic species which can create a conductive pathway for dendritic growth that can cause electrical failure if not properly heat activated. Unlike hand-soldering, the MMRI process includes full board preheat, which should eliminate any flux non-activation concerns, though halogen-free flux is recommended as an additional safeguard.

Alignment is done easily and quickly at board level using the inspection-quality stereo microscope with high magnification zoom lens, fine adjust X/Y table and theta rotational adjustment. Another advantage of the MMRI process is that a misaligned 01005 can be removed, aligned and replaced in a single step.

The 01005 replacement process becomes far more complicated when the residual solder cannot be used. First, any solder remaining on the pads must be removed with a micro-site cleaning nozzle, which provides both heat and vacuum. The board cooling system and the nozzle cool air bypass are activated and continue until the board temperature drops to 70°C. The board cooling system is powerful and the PCBs that 01005s will be used on will have low thermal mass so the cooldown will occur quickly. A proprietary micro-dipping tool is used in conjunction with a precision depth dip tray to transfer solder paste to the pads. The stereo microscope with zoom lens allows the operator to view the paste application process and to inspect the paste prior to proceeding. 01005 rework throughput can be increased by using a batch approach where all 01005 defects are removed and site cleaned and then all sites are pasted and replaced separately.

The nozzle is heated at low temperature and the replacement component is picked from the tape pocket. Static electricity and paper dust are two tape-related concerns. The replacement device is aligned with the pasted pads, placed and reflowed. Force feedback is provided to the operator during manual placement, which is important as assembly-based placement testing indicates that placement force in excess of 2 newtons (200 grams) can cause component cracking. Another significant advantage of the MMRI system compared to both hand-soldering and BGA rework systems is that after the replacement component is placed on the pasted pads,

Figure 7: Man/machine 01005 rework interface (MMRI).

the operator can retract the nozzle slightly and reflow the device with convective heating. This allows the 01005 to self-center which is not possible when the device is held in place with a conductive heating tip. Using the IR bottom heater in conjunction with the convective heating nozzle provides the gradual ramp-up desired for replacing ceramic capacitors which cannot be accomplished with conductive heating tips. Nitrogen is recommended for the convective reflow process to improve wetting and reduce oxidation of the fine grain solder particles.

The cleanliness of the micro-tip is critical to insure consistent vacuum removal of these microscopic devices on an ongoing basis. The operator periodically uses an ultra-fine gauge cleaning tool to keep the micro-vacuum tip clean.

PoP Rework

A PoP is two or more fine pitch components stacked on top of one another in an effort to save board space. The bottom package is typically a high-performance logic device and the top package is typically a high capacity memory device. Warpage of the bottom package caused by the CTE mismatch between the die, molding compound and substrate is by far the most common PoP issue. Warpage is a key issue for PoP due to the fact that the packages are extremely thin and typically fine pitch. PoP warpage typically manifests itself as a head-in-pillow (HiP) defect, which is defined as the incomplete coalescence of the solder joint between the PoP sphere and the printed solder paste. Other contributors to HiP defects include flux exhaustion, poor wetting and incorrect solder paste chemistry.

PoP Rework mimics standard BGA rework with a few modifications. PoP devices can either be removed separately with a standard nozzle that requires zero clearance (Figure 12) or together with a vacuum-activated tweezer nozzle, which requires some adjacent clearance (Figure 13). Some companies glue the two packages with adhesive so they can be removed together with a standard nozzle. PoP removal should not include any downward nozzle pressure during the removal process as this can result in solder ball migration to adjacent components. Vacuum-based component removal using a vacuum sensor accomplishes this task.

- Tip Contact Time : 7 seconds
- Heating Slope : 13° / second
- Max 01005 Temp : 242°C
- Heating Cycle : 7 seconds

01005 Removal
(Combined Conductive / Convective Heating)

- Tip Contact Time : 0 seconds
- Heating Slope : 2° / second
- Cooling Slope : -5° / seconds
- Max 01005 Temp : 242°C
- Heating/Cooling Cycle : 60 seconds

01005 Replacement
(Convective-only Heating)

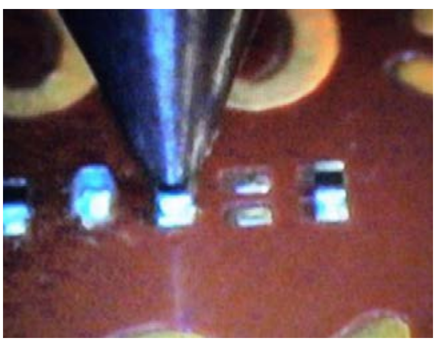

Figure 8: 01005 Micro-tip nozzle.

Figure 9: Paste transfer onto 01005 pads.

Figure 10: 01005 Replacement (left) site cleaned pads (right).

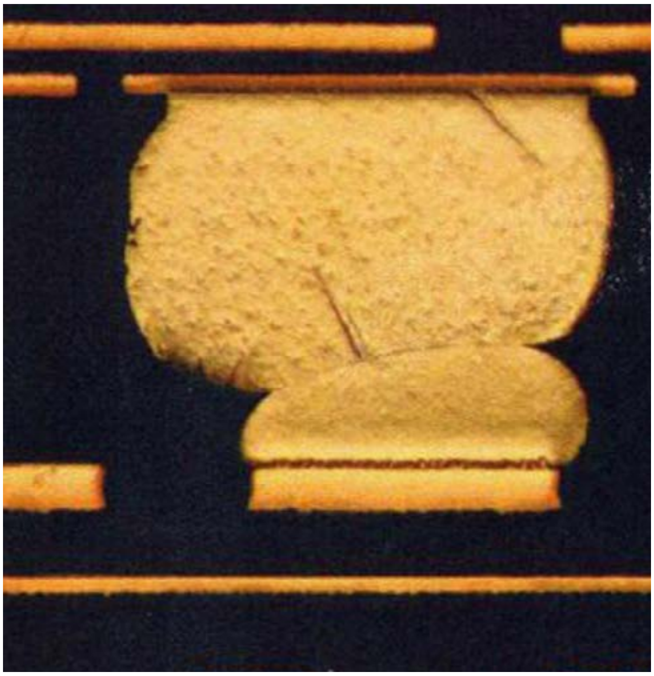

Figure 11: HiP defect[4].

After the components are removed, the residual site solder must be removed. The "stone age" practice of removing the residual solder with a soldering iron and wick should be replaced by non-contact solder removal to eliminate the potential for lifted pads and soldermask damage. The cautionary verbiage associated with using solder wick (i.e., manual site dressing is very dependent on operator skill, damage often occurs when operators do not tin the bit, do not apply pressure to the pads, the speed of the wicking process is critical, etc.) should serve as a wake-up call to companies who continue to allow wick-based site cleaning to be used because their operators prefer it or because it is fast. Higher lead-free reflow temperature and the continued drive toward finer pitch devices should signal the end of wick-based cleaning, however iNEMI estimates that wick is still currently used 80% of the time for site preparation. Every operator can detect a damaged pad and knows how to fix it, but determining if the soldermask has been damaged by the solder wicking process is far more difficult.

Some BGA rework equipment manufacturers' claim to have a non-contact site cleaning system, but they really have a heated nozzle with a metal vacuum tip that is moved across the site with manual "x," "y," and "z" controls. A true non-contact site cleaning tool incorporates a vacuum sensor that automatically and continuously adjusts the vacuum tip height.

The most advanced systems go one step further by using a high-temperature composite vacuum tip rather than a metal tip to completely eliminate the possibility of a heated metal tip contacting the board or the pads (Figure 14).

Users are demanding faster non-contact site cleaning solutions in order to switch from solder wick. Some BGA rework manufacturers have already developed larger, site-specific cleaning tools designed to clean the site in a single pass (Figure 15).

PoP replacement is more complicated than replacing a BGA. First, the bottom package is

Figure 12: Standard nozzle removes one package at a time.

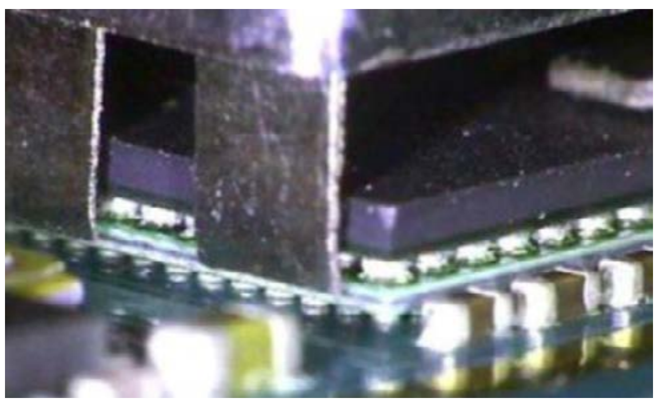

Figure 13: Tweezer nozzle (Finetech) removes both packages together.

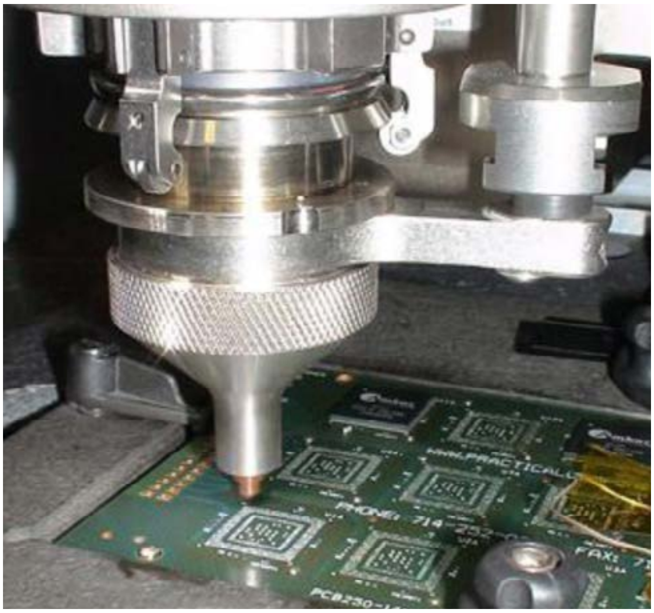

Figure 14: Non-contact site cleaning system.

Figure 15: Large site cleaning nozzle (Zevac AG).

picked and is typically dipped in a controlled volume of flux or dippable solder paste, using force control to insure repeatability. Ideally, the dipping process can have multiple programmable dip locations so that the dip tray does not have to be re-prepared after each process (Figure 17). Dipping the bottom package in solder paste helps to address the warpage/HiP issue discussed earlier. Using a dippable solder paste chemistry with a higher temperature activation will help reduce flux exhaustion and improve wetting. If the beamsplitter has independent top and bottom lighting, camera zoom and the ability to move to all areas of the component, the solder paste on the spheres can be inspected during alignment in vision (Figure 18). This allows the operator to terminate the process if the paste has bridged or is missing from any spheres.

The top package can be dipped in either solder paste or tacky flux as the top package will have a lower CTE mismatch and therefore less warpage. If the top package is dipped in solder paste, it can be inspected in vision. If the package is dipped in tacky flux, inspection in vision will not be possible; however, the imprint of the spheres into the flux tray can be inspected to ensure that all spheres have flux on them. Some flux manufacturers are now adding a color dye to the tacky flux so inspection is possible.

The top package is aligned with the top side of the bottom package and placed onto the bottom package. Force control (1–2 newtons) is

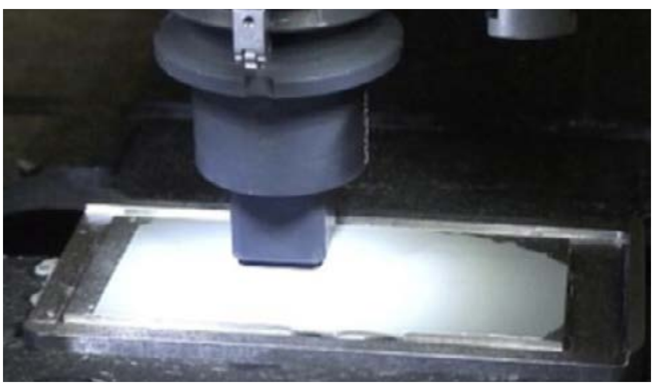

Figure 16: Force-controlled solder paste dipping.

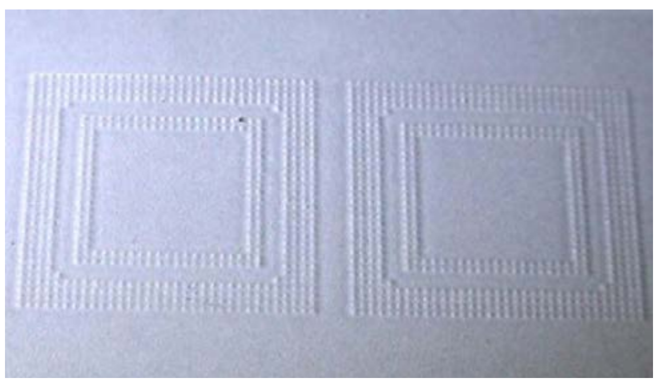

Figure 17: Multiple imprints in solder paste.

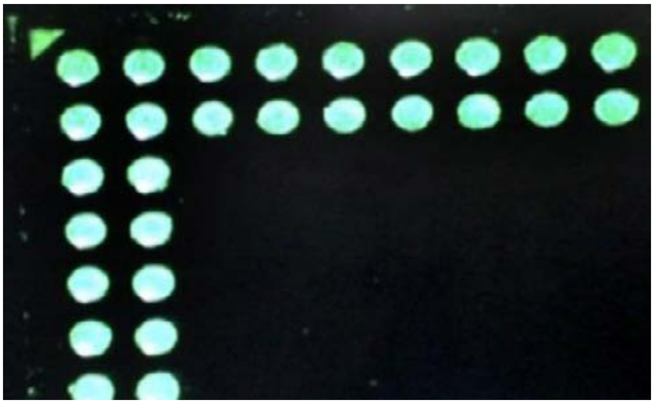

Figure 18: Inspecting paste on spheres in vision.

recommended. Both packages are then reflowed together. Some BGA rework manufacturers recommend reflowing the packages separately. It is not clear why this approach is recommended as it results in an additional complete reflow cycle for the bottom package and the PCB. Nitrogen is recommended for the reflow process to improve wetting and reduce oxidation of the fine grain solder particles.

Through-mold via (TMV) PoP (Figure 19) is Amkor's next-generation 3D packaging solution which uses a laser ablation process to create recesses within the dielectric material as opposed to current photolithographic techniques where the signals are formed on the surface of the dielectric[5]. TMV PoP utilizes a balanced, fully molded structure which improves warpage control and allows bottom package thickness reductions. Thermal shadow moiré testing demonstrates that the TMV PoP exhibited a dramatic improvement in warpage compared to the conventional PoP package as shown in Table 4.

TMV PoP Solderability Testing

A 77 x 132 mm test board (eight layers, 1.0 mm thick) and 14 mm TMV PoP devices were used for solderability testing (Figure 20). The

Figure 19: Amkor TMV PoP.

bottom package is 0.65 mm pitch with 620 I/O while the top package is 0.5 mm pitch with 200 I/O. A typical preheat/soak/ramp/reflow/cool soldering profile was developed on a BGA rework system by instrumenting one TMV PoP.

No thermal changes were made to the reflow process throughout the study. The only thing that was changed was the component/site preparation method and material as summarized in Table 5.

The objective of the study was to see if the component/site preparation method/material had any significant impact on the TMV PoP in regard to warpage, HiP or any other defects.

PoP Solderability Testing Results

Cross-sectioning results of the PoP solderability testing indicates that the biggest factor influencing good joint formation is the liberal use of flux. Best results for both top and bottom joints resulted when flux was brushed on both the site and top side pad surface on the bottom PoP. Flux dipping produced reasonable results, but joints were not always as well

Package/Substrate	TMV/0.30	FC PoP/0.30
Max Warpage (μM)	-51.8	-136.8

Table 4: Thermal shadow moiré results[6].


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AND SUPPLY CHAIN
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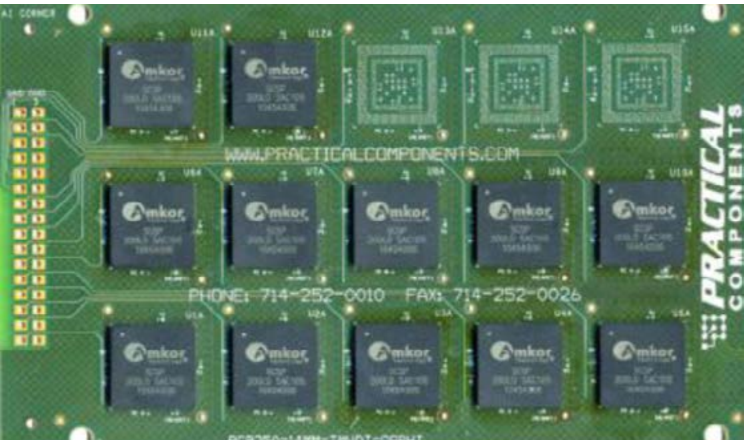

Figure 20: TMV PoP test vehicle.

formed as when flux was brushed on the pads. Solder paste dipping showed the poorest results with some cases of complete opens and at best only partial wetting of solder sphere to pad. Nitrogen also appears to produce better overall results than air and appears to help in marginal soldering situations.

One thought is that the small size of the PoP solder spheres limits the volume of flux or solder paste that can be applied during the dipping process to levels that are not sufficient to produce good solderability results. But the sample size in the study was relatively small and should be verified by follow-up testing using a larger sample size.

QFN/MLF Rework

Amkor refers to theses as MLFs (micro leadframe) while many others refer to these components as QFNs (quad flat, no leads). IPC calls these devices BTCs (bottom terminated components).

The MLF is a plastic encapsulated package with a copper lead frame substrate. The package uses perimeter lands on the bottom of the package to provide electrical contact to the PCB. The package also has a large center pad on the bottom of the package to provide an efficient heat path to the PCB.

The two major issues associated with QFN technology are excessive voiding in the thermal pad area and outgassing which may cause solder balling and/or splatter. Both issues are caused by flux entrapment due to the low component standoff height. IPC-A-610 allows voiding levels of up to 25%.

The QFN/MLF rework process mimics the PoP process explained earlier except that solder paste dipping is not possible with QFNs due to package flatness. Solder paste must be applied to either the component or the pads prior to replacement. There are a number of processes for applying solder paste, including solder preforms, polyimide or metal site stencils, polyimide or metal component stencils, stay-in-place stencils or multi-up stencils.

The stay-in-place stencil approach applies a tacky polyimide stencil to the device (Figure 25a). Paste is applied and the excess removed with a doctor blade. The device is then reflowed and the stencil is removed leaving a bumped device (Figure 25b). A second stencil is applied to the pads and paste or flux is applied (Figure 25c). The bumped

	Bottom Package				Top Package		
Placement #	Paste Dip	Flux Dip	Flux Site	Flux Top of Pkg	Paste Dip	Flux Dip	Nitrogen
1-2		✓				✓	
3-4			✓	✓			
5-6			✓			✓	
7-8	✓				✓		
9-10	✓		✓	✓	✓		
11-12			✓		✓		
13-14		✓				✓	✓
15-16	✓				✓		✓
17-18			✓	✓			✓

Table 5: TMV PoP solderability testing.

Figure 21: Cross-section showing poor results (solder paste dipping).

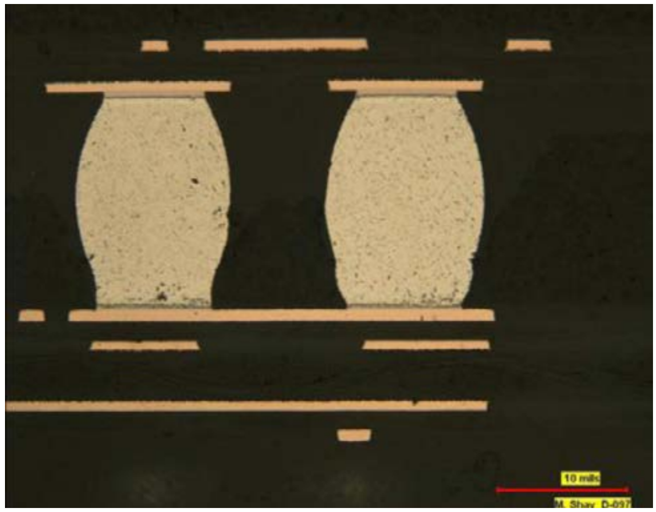

Figure 22: Cross-section showing good results (flux brushed on).

QFN/MLF is placed in the site stencil and reflowed. The site stencil remains on the board permanently. Reliability testing by NASA/DOD indicates that the stay-in-place stencil performed at the same level as traditional board paste printing.

Another pasting methodology is the multi-up method where a multi-up stretched metal stencil is used instead of a single component stencil (Figure 26). Typically 20 devices can be stenciled together depending on size. After the components are stenciled, a vacuum table is activated to hold the components in place as the stencil is lifted. The pasted components are reflowed and stored as bumped components for later use. Tacky flux is applied to the site prior to placement.

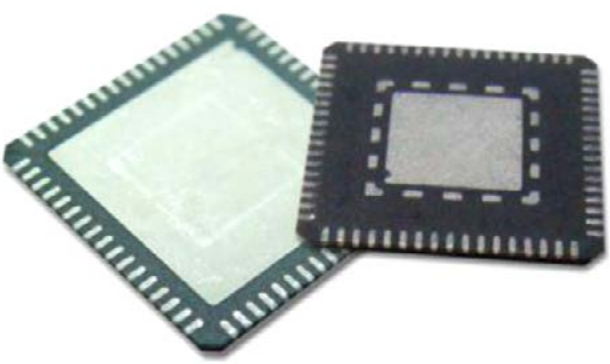

Figure 23: QFN/MLF devices.

The design of the solder paste stencil for the thermal pad on a QFN is critical to help minimize voiding and outgassing. Amkor recommends that the stencil have multiple smaller openings instead of one large opening which will typically result in 50–80% solder paste coverage. Amkor also recommends a stencil thickness of 0.125 mm for 0.4 and 0.5 mm pitch parts and 0.15–0.2 mm thickness for coarser pitch parts[9].

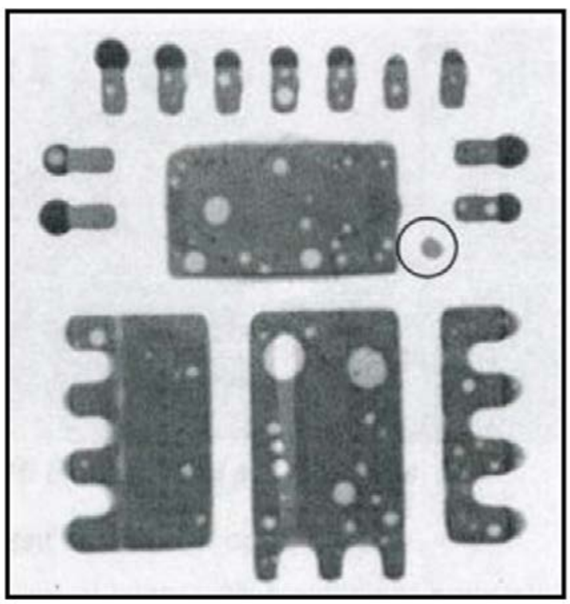

Figure 24: Example of voiding and solder balling under a power QFN[7].

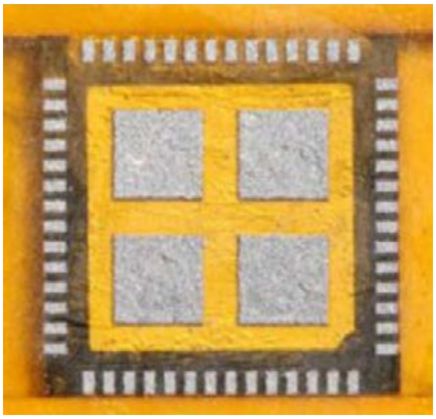

Figure 25a: QFN with stencil and solder paste[8].

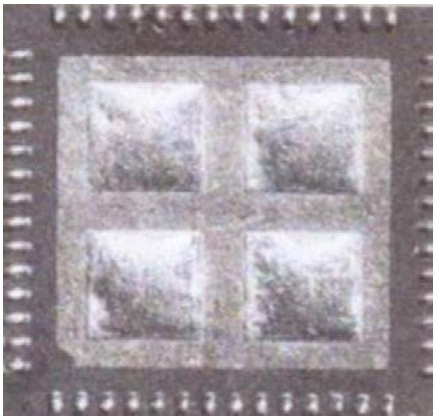

Figure 25b: Bumped QFN after reflow and removal of stencil[8].

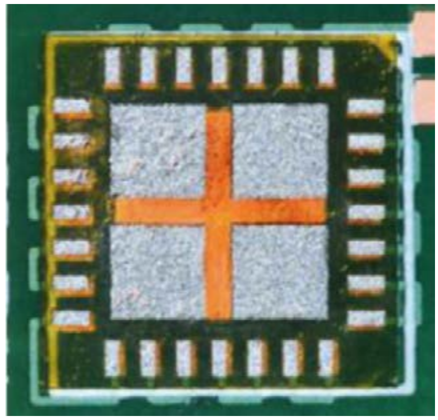

Figure 25c: Stay-in-place site stencil[8].

QFN Solderability Testing

A 203 x 140 mm (8" x 5.5") 0.062" thick test vehicle along with 10 mm square MLF components with 0.5 mm pitch were used for solderability testing. Two thermal profiles were developed; a short soak/ramp profile and a longer soak/ramp profile.

Three paste-on-device metal stencils with different center pad designs and paste coverage were used as shown below. All stencils used were 0.125 mm (.005") thick.

In addition, the multi-up stencil system described previously was used in conjunction with the center pad #2 stencil design. The MLF devices were stenciled and reflowed prior to use in the test. Indium 9.0A no-clean solder paste (type 4 mesh) was used with all stencils.

The objective of the solderability study was to determine which stencil design provided the best results in regard to minimum voiding in the center pad region. A second objective was to determine if the pre-reflowed QFNs from the multi-up stencil performed as well as pasted QFNs with the same stencil design.

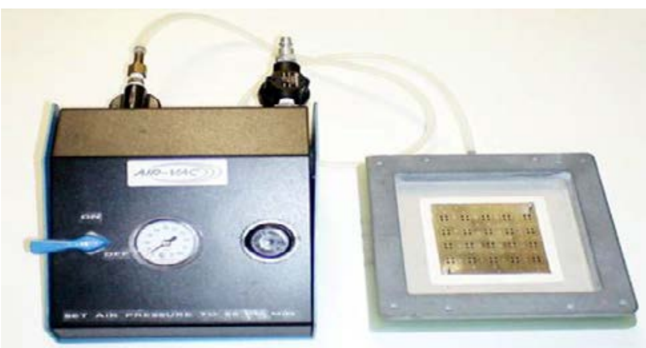

Figure 26: Multi-up stenciling system.

Results

Voiding results using the various center pad stencil designs and short versus long soak/ramp cycles are summarized in Table 6.

All of the QFNs had total percent voiding well below the IPC specification of 25%. The long soak stage provided less voiding than the short soak stage with all three stencils. The long soak stage with the lowest percent solder paste coverage yielded the best results. Finally, the QFNs that were pre-bumped with the multi-up stencil approach yielded similar results to the standard pasting approach.

Conclusion

Large area arrays (>50 mm) on large, high-thermal mass PCBs will create rework challenges including meeting the current strict reflow and package temperature guidelines that were established for much smaller BGAs. Other challenges that will need to be addressed include alignment capability, warpage, large board handling and safe/fast/effective site cleaning. Access to next-generation large area arrays on high-thermal-mass PCBs is required to develop effective rework solutions.

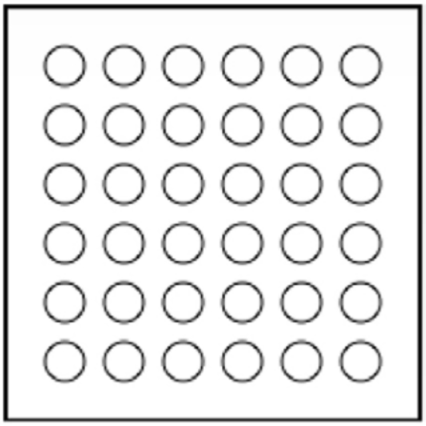

Figure 27a: 1.00 mm diameter circles @ 1.2 mm pitch—50% coverage[10].

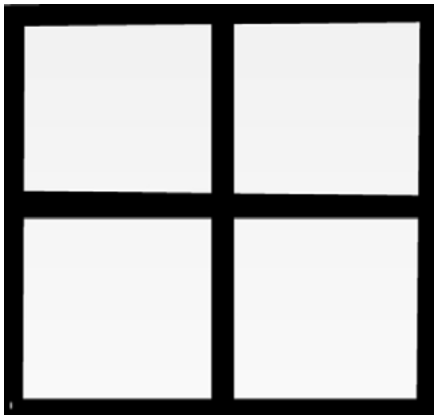

Figure 27b: 3.10 mm squares (10) @ 3.95 mm pitch—60% coverage[10].

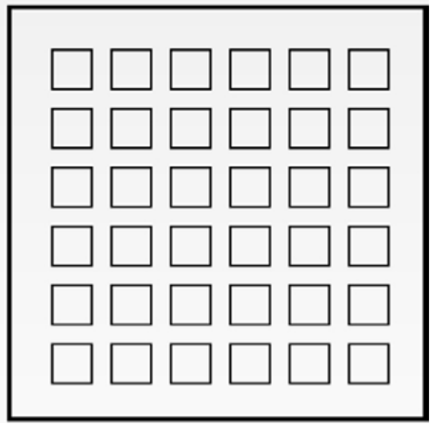

Figure 27c: 1.35 x 1.35 mm squares (10) @ 1.5 mm pitch—81% coverage[10].

Methodologies must be developed for reworking microscopic 01005s in a cost-effective, practical manner that provides high throughput capability. The ability to clean the site and prepare it with solder paste will be important as 50% of 01005 defects are created by the paste printing process. A man/machine rework interface (MMRI) approach was proposed as a possible solution.

Packaging innovations such as Amkor's TMV PoP will help resolve HiP issues that are found frequently with current PoP packaging technology. A PoP solderability study showed that manual flux application and the use of nitrogen yielded the best results.

Several MLF/QFN solder paste application methods were discussed including two new and innovative methods: stay-in-place stencils and the multi-up stencil. The design of the stencil for the center pad area is critical to minimize voiding caused by flux entrapment from the low package stand-off height.

Modifications to existing BGA rework equipment as well as new equipment and processes will be required to meet the challenges associated with reworking next-generation SMT applications.

Acknowledgements

I would like to acknowledge Mario Scalzo, senior technical support engineer at Indium, for providing all of the solder pastes and fluxes used in this paper as well as for the insight he provided regarding the various solder alloys and flux chemistries.

I would also like to thank Chuck Richardson at iNEMI for allowing me to utilize information from the Rework and Repair section of the 2013

				Voiding (Center Pad)	
Stencil	**Location**	**% Coverage**	**Profile**	**Total**	**Largest Single**
36 Circles	1A	50%	Short Soak/Ramp	11.5%	1.6%
36 Circles	1B	50%	Long Soak/Ramp	6.5%	0.6%
4 Windows	2A	60%	Short Soak/Ramp	17.9%	2.0%
4 Windows	2B	60%	Long Soak/Ramp	10.5%	1.9%
25 Windows	3A	81%	Short Soak/Ramp	13.4%	2.4%
25 Windows	3B	81%	Long Soak/Ramp	11.3%	1.8%
4 Windows (1)	4A	60%	Short Soak/Ramp	13.3%	1.1%
4 Windows (1)	4B	60%	Long Soak/Ramp	16.1%	1.4%

(1) Using Multi-Up Stencil, Reflowed in Advance of Use, Flux Added to Site

Table 6: QFN voiding summary.

iNEMI Technology Roadmap in this presentation.

Thanks also to Don Morgenstern and Ron Wachter at Air-Vac for performing all of the PoP and MLF solderability testing. I would also like to thank all of my other co-workers at Air-Vac who helped on this project.

Finally, I wish to thank MPI for providing X-Ray analysis for the PoP and QFN/MLF solderability tests as well as 01005 production assemblies, and Endicott Interconnect Technologies for performing the PoP cross-sectioning. **SMT**

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Rework and Reliability of High I/O CGA Assemblies

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This article was initially presented at the 2013 IPC APEX EXPO Technical Conference.

SUMMARY: Commercial-off-the-shelf column grid array packaging technologies in high-reliability versions are now being considered for use in a number of NASA electronic systems. Understanding the process and quality assurance indicators for reliability are important for low-risk insertion of these advanced electronic packages.

Abstract

This article presents rework and re-column attachment of two high-input/output (I/O) CCGA (CGA) packages (560 and 1144 I/Os). Subsequent to re-column attachment and isothermal aging, the integrity of tin-lead solder-column attachment was determined and presented. In addition, the process-control parameters for assembly of re-columned CGA packages using either vapor-phase or rework stations were established for both package types/sizes. Details of these process control parameters solder paste-print uniformity as well as quality assurance indicators based on visual inspection before and during thermal cycling tests are presented. Qualification guidelines generated based on these and additional optical photomicrographs, X-rays, SEMs, and destructive cross-sectioning of thermally cycled, reworked, re-columned, and re-assembled test vehicles of these CGAs are presented in detail.

Introduction

The author has addressed assembly reliability behavior of numerous ceramic column grid array (CCGA or CGA) types in previous investigations[1, 2, 3]. In addition, package suppliers also provided some board level reliability data for their specific packages[4, 5, 6, 7]. For high-reliability applications, CGAs with a 1.27 mm pitch (dis-

tance between adjacent ball centers) or lower are now replacing surface mount leaded packages, such as ceramic quad flat packs (CQFPs). In addition to size reduction, CGAs also provide improved electrical and thermal performance; however, their solder columns are prone to damage, and it is almost impossible to rework defective solder joints. Rework, re-column, and re-assembly may be required to address solder defects due to processing or column damage prior to assembly due to shipping and mishandling. This article presents test results for column attachment process and integrity as well as assembly reliability for two different CGA package sizes/styles/I/Os, one with 560 and the other one with 1144 I/Os. Re-columned packages were assembled on PCBs using tin-lead solder paste that were reflowed either by vapor-phase machine or rework station. Optical microscopy and scanning electron microscopy (SEM) was used to capture damage progress of column and solder interconnection due to thermal cycling at intervals. Results performed und different thermal cycling ranges along with optical photomicrographs, X-ray, SEM, and X-sections are also presented.

Assembly, Rework, and Re-assembly of CGA560

A CGA package with 560 columns was selected for assembly and subsequent rework, re-column, and re-assembly, and reliability evaluation. Figure 1 depicts a photomicrograph of the CGA560 package with interposer attached and its interposer layer alone on top of package. The CGA560 package had a few key characteristics that are considered to be ideal for the rework process optimization. These special features included:

• Package availability: Individual virgin packages as well as test vehicles (TVs) with package assemblies were available, and the effect of additional rework on thermal cycle behavior after re-columning and re-assembling could be compared.

• Large ceramic package: The package is relatively large since it was designed to simulate its plastic counterpart version with the identical configuration, I/O counts, and 1.27 mm pitch.

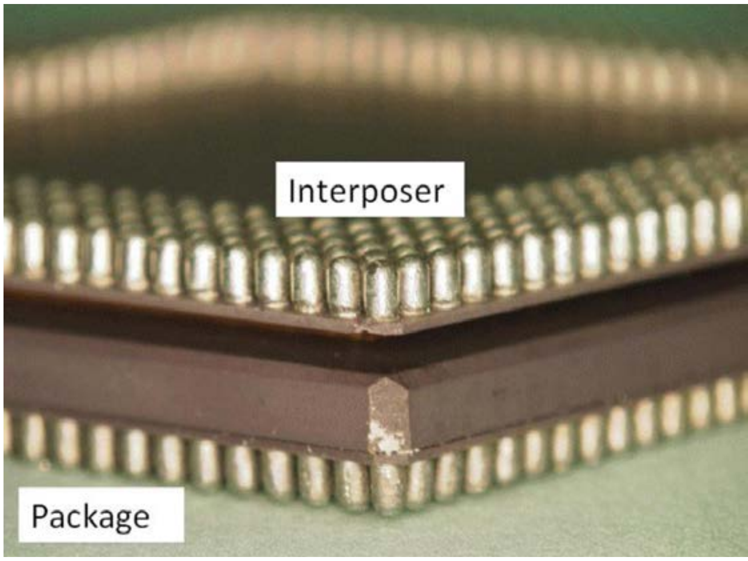


Figure 1: Optical photomicrograph of a virgin CGA 560 I/O package before re-columning with interposer (bottom) and an interposer layer alone on the top.

It is a peripheral array rather than a full array which is a common configuration for CGAs.

• Large CTE mismatch: The package had an added ceramic interposer for absorbing CTE mismatch to improve assembly solder joint reliability. This thin ceramic interposer was removed prior to re-columning in order to introduce maximum stresses due to CTE mismatches during thermal cycling exposures.

• Large columns: Possibly because of the package size and interposer, solder column diameter is unusually larger than standard diameter; therefore, the re-columned version had lower diameter requiring smaller PCB pad sizes for assembly.

• Assembly rework: Assembled packages were removed by rework station. Also utilized two pad designs using the initial TVs, one for CGA and the other for PBGA.

Key Rework Parameters

A design of experiment (DOE) technique was utilized to cover many aspects of re-columning and re-assembling that are considered unique for this package configuration. The following parameters were part of the DOE matrix even though, in some cases, because of re-assembly processing issues, they could not be evaluated for subsequent thermal cycling behavior characterization as it was planned originally.

• CGA packages with and without corner staking were successfully removed from assembled TVs. In the first attempt, corner stakes induced minor damage to the board at corners away from the pads since the direction for removal was not clearly given to operator. Damage to board was minimized through providing a more detail procedure for reworking. Figure 2 depicts photomicrographs of packages after removal showing remains of columns on the interposer and daisy chain pattern for the exposed package pads.

• Ceramic interposer layers were removed both for virgin and reworked packages prior to re-column attachment on the new package with the land grid array pattern.

• These daisy chain packages had traces between many pads to accommodate full daisy chain resistance monitoring when assembled onto a board. Masking of these traces was considered before column attachment; however, the vendor was able to perform column attachment successfully with no evidence of shorts without masking the daisy chain traces. Tin-lead solder paste was used for column attachment.

• One re-columned virgin package was subjected to pull testing to assure quality of column solder joint attachments prior to committing to re-columning of other parts.

• Two additional re-columned virgin packages were subjected to isothermal aging and pull testing to determine quality of bond interfaces after aging exposures. One package had an additional simulated re-columning reflow to represent rework.

• Two mini-stencils were used for the two pad sizes: one designed for CGA pads, and the other designed for smaller pads for PBGA attachment. Mostly the CGA pad design was used.

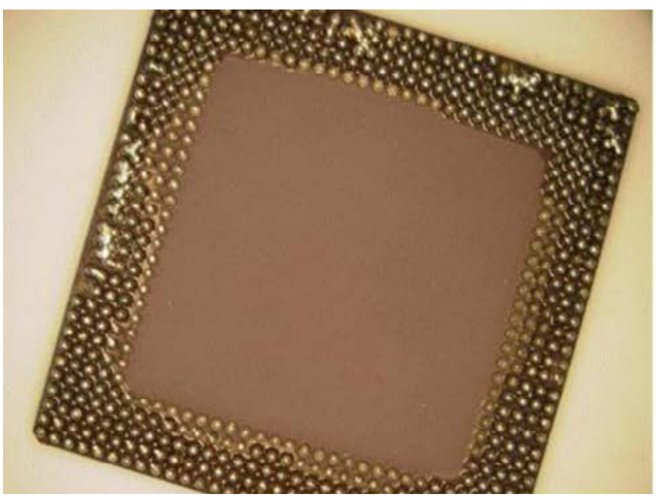
• All packages were placed onto PCBs using a rework station. Both the rework station and the vapor phase reflow machine were used for reflowing solder pastes. The TVs with PBGA assemblies were also reflowed in place one more time during reflow of re-columned packages.

• A vapor-phase reflow profile for tin-lead solder with constant reflow temperature at 217°C for duration of 60 seconds was used.

• Acceptable reassembled TVs as well as those with known manufacturing defects were subjected to thermal cycling to detect early failures due to workmanship and damage progress with cycling for CGAs with acceptable quality.

• Optical photomicrographs, X-ray, and cross-sectioning were documented.

Reworked Package



Package Base

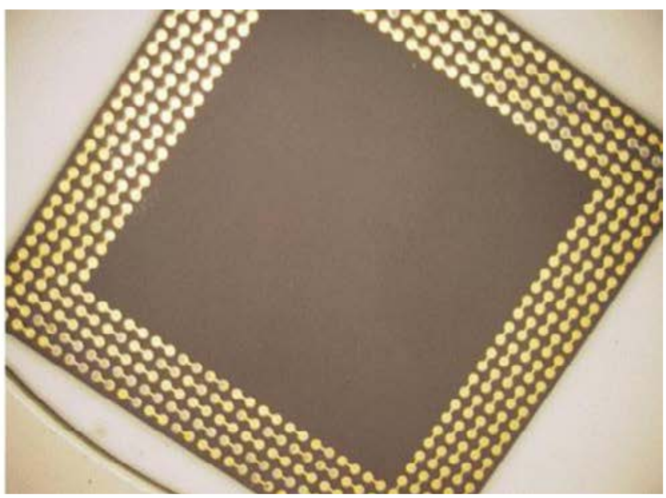


Figure 2: Optical photomicrographs of a removed CGA560 package after rework showing removed/shorted columns (left) and package daisy chain pattern without interposer (right).

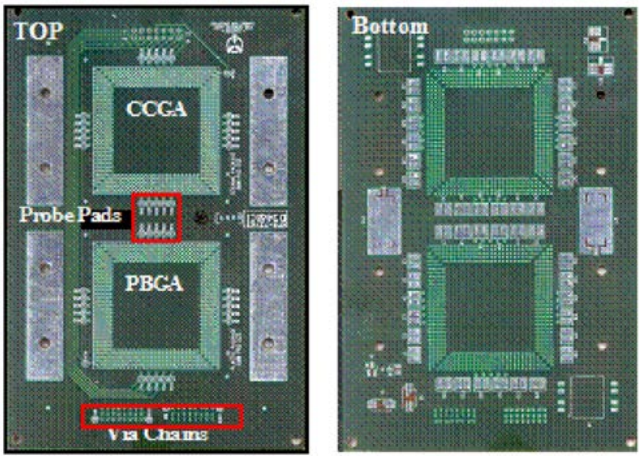


Figure 3: PCB design showing package daisy chain, probing pads, and via daisy chains.

PCB/TV/Package CGA 560 I/Os

Figure 3 depicts the top and bottom of the board design for the CGA560 package assembly showing the daisy chain configurations, including PBGA560 probing pads. The PCB's pads had hot air solder level (HASL) tin-lead surface finish as specified in IPC[8] for tin-lead solder assembly.

Re-assembly of CGA560 Results

A detailed test matrix for rework, re-column, and re-assembly of TVs was outlined at the start of the build. However, during subsequent re-assembly, it was recognized that on-the-spot modifications are required to achieve acceptable assemblies based on visual inspection of outer-row solder columns due to numerous assembly challenges. For example, Figure 4 includes two representative TVs after re-assembly of re-columned CGA560 packages. One has acceptable quality, but the other was rejected because of gross package twisting possibly occurred due to uneven nuzzle heat flow. As stated, a rework station was used for both placement and reflow since it represents a more realistic condition.

Inspection after Re-assembly of CGA560

Photomicrographs were taken after all test vehicles were reassembled to document quality of solder joints, including those with various workmanship defects. Figures 5 shows optical photomicrographs for re-columned CGA560 packages assembled under various conditions. Several processing defects are noticeable from these photos, including the following:

- Photomicrographs comparing quality of solder joints reflowed by vapor-phase machine or rework station. In a case where solder paste was not reflowed by rework, station was reflowed using reflow machine.
- Significant column shift when the package is assembled on relatively smaller pads designed for its PBGA package assembly.

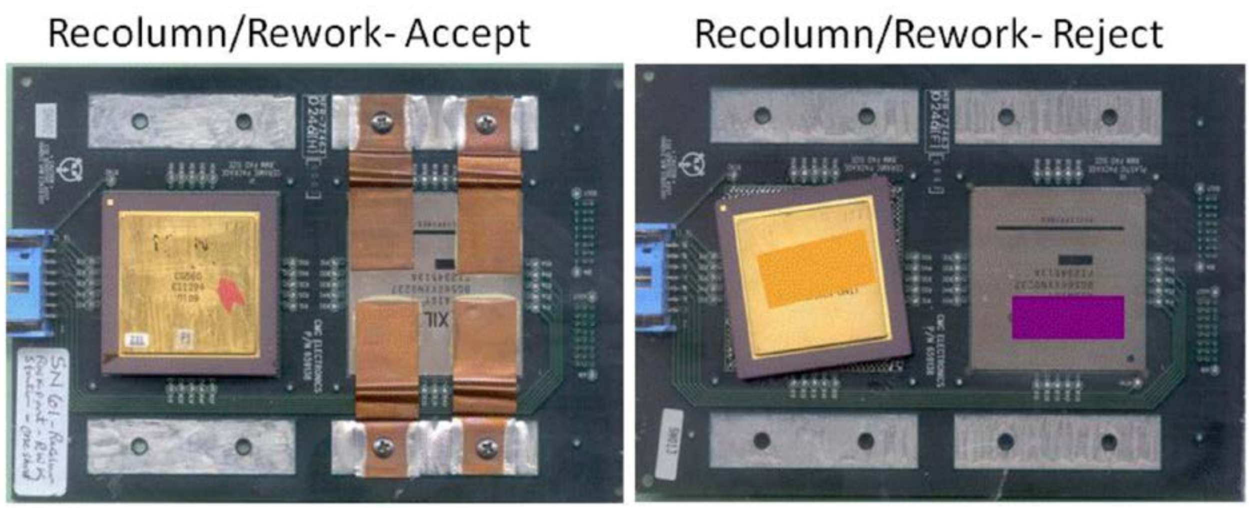


Figure 4: Representative TVs after re-assembly of re-columned CGA560 packages: one with acceptable quality and the other rejected with gross package twisting occurred during solder reflow by a rework station.

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• Solder short between the two columns in the middle of package outer row.

• Corner column shift and also the appearance of solder column separation at the package side (not shown at high magnification).

• Solder balls on the package in addition to the board side (photomicrographs not shown here); their source was not identified.

The soldered column separation from the package side is a significant failure and is unusual. This might be due to the weakness in re-column attachment, which might have been exacerbated by another reflow during re-assembly causing solder separation at the pads. Note; however, that the new columns have much smaller diameter that are placed on relatively larger package pads allowing more movement of columns during reflow. Follow-on test results for strength reduction on re-columned packages with and without additional reflow and subsequent aging at 125°C all indicated lack of significant interfacial degradation. Consequently, the tensile test results reject the possibility of failure due to weakness of solder joints at interfaces. Another possibility is that the smaller re-column size relative to the large package size and weight causes elimination of self-alignment, which is a key advantage of the area array package. Daisy chain connections between the pads at the package side also are not representative of a working part and may contribute to such interfacial failure. Solder on daisy chain traces can possibly further facilitate column shifting to the neighboring pads during solder reflow.

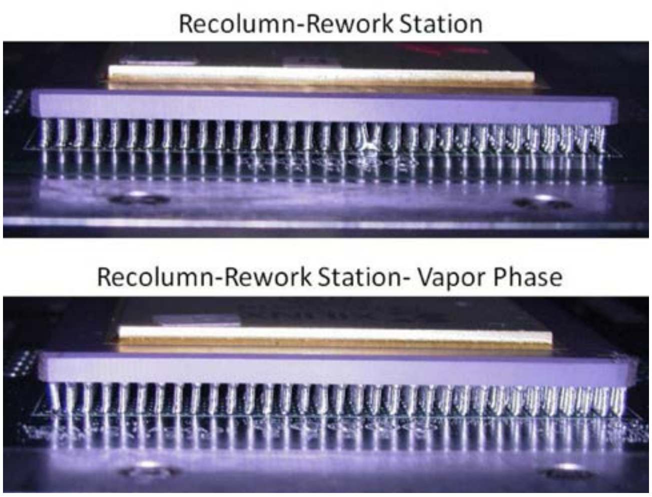

Figure 5: Representative of optical photomicrographs for re-columned 560 I/O package assemblies.

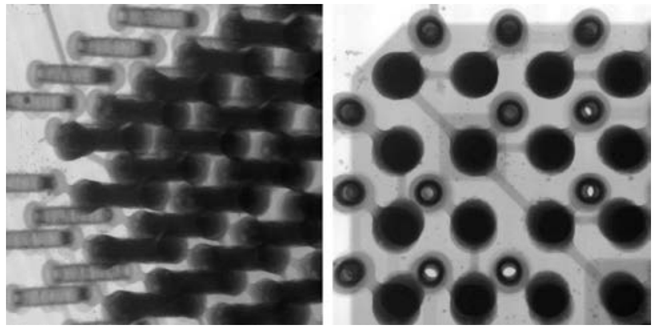

Figure 6: X-ray photomicrographs for re-columned and re-assembled CGA560 after thermal cycle exposure showing solder balls, but no separation at package pads detected visually.

Results for CGA560

Thermal Cycle Conditions

Only a few assemblies had acceptable quality because of manufacturing challenges. Four assemblies considered to be acceptable were subjected to a cycle condition ranged from -55° to 100°C with a 2–5°C/min heating/cooling rate. Dwells at extreme temperatures were 15 minutes.

X-ray Characterization

A real time, 2-D X-ray system with a stationary microfocus source intensity and off-axis rotational capability was used to determine the damage states of re-columned CGA560 assemblies. Figure 6 shows an X-ray photomicrograph for an assembled CGA560 after thermal cycle exposure. The X-ray technique clearly detects abundance of solder balls but no indication of other defects; neither solder damage nor solder separation at pads due to thermal cycling.

Damage Progress with Thermal Cycles

Damage progress with thermal cycling was established using optical microscope. Figure

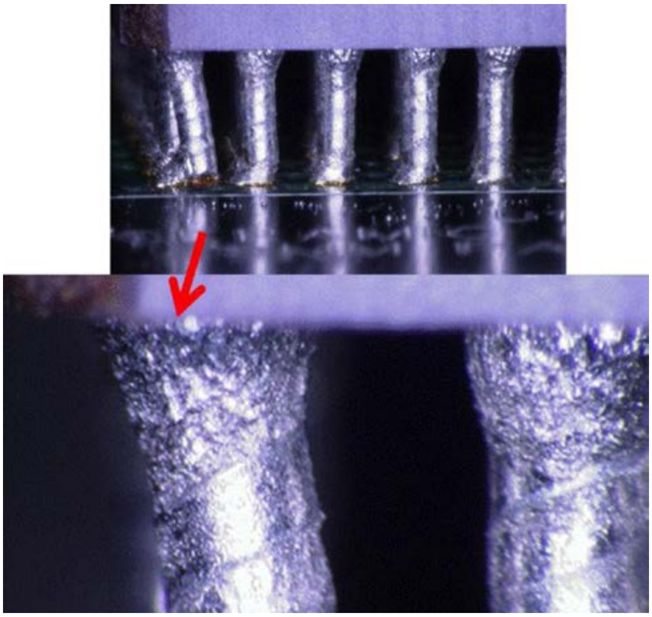

Figure 7: Optical photomicrograph re-columned and reassembled CGA 560 I/Os after thermal cycles showing microcracks in solder at the package side.

7 presents a representative photomicrograph showing workmanship defects due to manufacturing as well as damage due to thermal cycling. Based on all inspected solder joints, there were various defects due to re-assembly that are categorized as follows:

• Solder balls at the package and board sides are apparent from low and high magnifications of re-column attachments. Coalescence of a large number of solder balls was observed at the package side at higher magnification. The sources of these solder balls are not clear, but they could be the result of solder splash from paste during solder reflow.

• Several displaced columns showing a larger corner column shift are apparent. Magnified photomicrographs clearly show signs of damage and microcracking due to thermal cycling at the package side.

• Several columns were shifted after thermal cycling. Photomicrographs of these at higher magnification clearly show pad separation from the package. This failure is unusual since microcracking generally occurs in the solder, as shown in the previous figure.

As discussed, soldered column separation from package side is considered an unusual and significant failure. Tensile test results exhibited no such failure mechanisms and no indication of interfacial weakness. Possible reasons for such a failure mechanism may be an unusual package size/weight and use of a smaller-column diameter.

SEM Photomicrographs and X-section

After thermal cycle completion, one sample was cut at its periphery in preparation for additional optical, SEM, and cross-sectioning. Figure 8 depicts representative optical photomicrographs of the assembly prior to cross-sectioning. Damage and microcracks exhibit better resolution since optical lenses now can get close to the package with no interference from the board. Figure 9 depicts representative SEM backscatter photomicrographs of column attachments at various magnifications up to 1,000 times. Cracks at the package side in solder interfaces are clearly apparent. Figure 10 depicts a photomicrograph at much higher magnification showing at least three types of microcracks. Potential mechanisms include: a) the large microcracks at the package interface surrounding the pad interface are due to the weak re-column attachment; b) the microcracks close to Cu spiral are due to weak Cu/solder interface and local CTE mismatch; and c) the microcracks parallel to interface between solder and column are due to the overall package/board CTE mismatch.

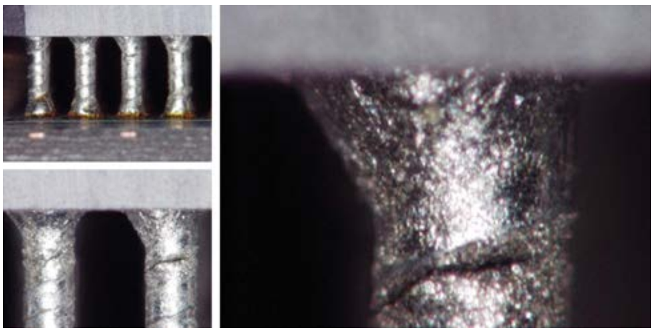

Figure 8: Optical photomicrographs of re-columned and reassembled CGA 560 I/Os after thermal cycles and prior to X-sectioning showing microcracks in columns and solders at the package side.

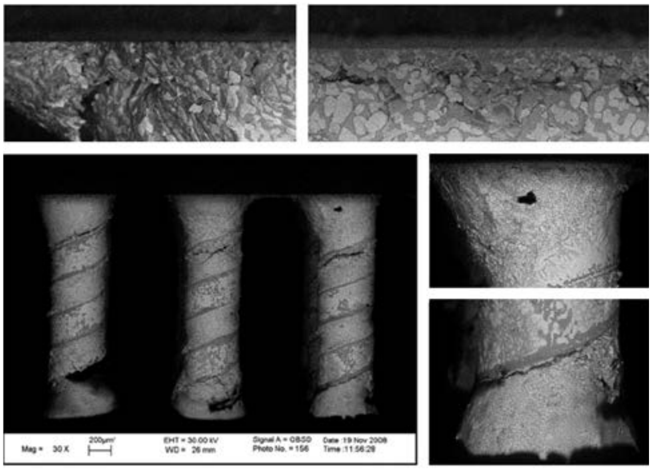

Figure 9: SEM photomicrographs of re-columned and reassembled CGA560 after thermal cycles and prior to X-sectioning showing microcracks in columns and solders at the package side.

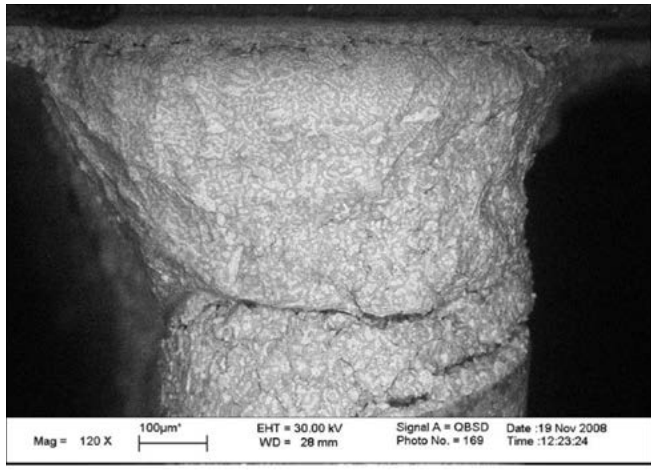

Figure 10: SEM photomicrograph of re-columned and reassembled CGA560 after thermal cycles and prior to X-sectioning showing different types of microcracks in column and solder at the package side.

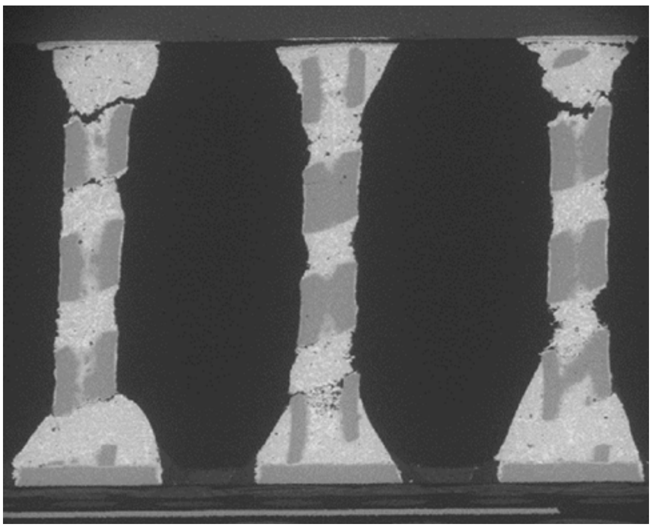

Figure 11: X-section photomicrographs of re-columned and reassembled CGA560 after thermal cycling showing microcracks and separation mostly at the package side (top).

X-section photomicrographs for the three corner columns are shown in Figure 11. It clearly shows significant damage and minor-to-full cracking, more often at the package sides.

Figure 12 depicts SEM photomicrographs at higher magnifications, showing interfacial damage conditions both at the package and at the PCB sides. Separation at the package pad interface with minimum solder remnant at the pad is possibly an indication of weaker metallurgical bond due to re-columning and second reflow due re-work/re-assembly. More damage and cracking at the package side may also be due to a larger local CTE mismatch between the ceramic and solder at the package side in comparison to polymeric PCB and solder at the board level.

Evaluation of CGA 1144 I/Os

The purpose of this aspect of the investigation was to characterize assembly reliability of CGA1144. Eutectic tin-lead solder alloy was used for assembly. In contrast to the CGA560, this package had different pad configuration and column type. Differences include:

- Fully populated area array package rather than peripheral array
- Internal flip-chip die rather than wire bond
- 1 mm pitch rather than 1.27 mm
- 35 mm package body rather than 42.5 mm

Similar to other CGA packages, three columns from each corner were missing; they were intentionally removed by the package supplier in order to improve solder joint reliability. Corner solder columns usually fail first in thermal cycling because they have the longest distances to neutral point (package center).

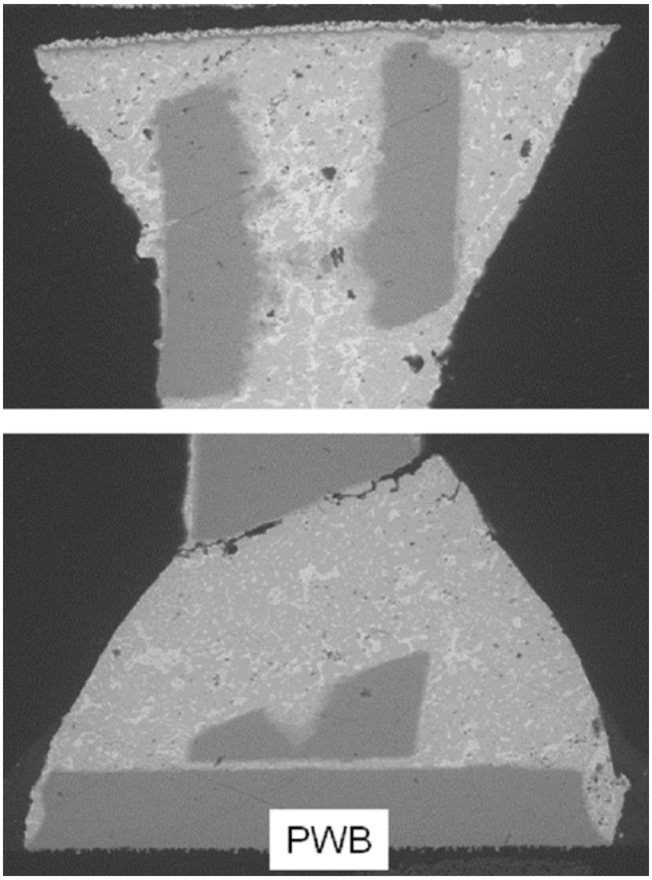

Figure 12: X-section photomicrograph of re-columned and reassembled CGA560 after thermal cycling showing interfacial condition at package and PCB sides. Full cracking at the package side is apparent.

The original column type in this package is also different from the CGA560; it uses Pb90/Sn10 solder columns with no Cu wrap. Similar to re-columned CGA560, the Cu wrap columns replaced the virgin columns of high-lead composition. Both a typical and a smaller-diameter column were included for evaluation. Smaller-size columns can be used for the high I/O CGA since the package is smaller and lighter, reducing potential of column breakage due to overloading condition. Because of these significant changes, assembly processing parameters were different from the CGA560 packages; therefore, they required being tailored again for reflow optimization.

Tailoring was performed based on previous experiences for similar packages. Additionally, the process was modified on the spot if required, this being possible because only twelve packages were assembled. Ease and consistency in paste deposition, condition of fillet formation after reflow, and solder joint visual appearance were a few important parameters used for tailoring process.

Key re-column and re-assembly parameters for processing and evaluation are as follows:

- Successfully re-columned eight CGA1144 packages with 20-mil column diameter. No fallout due to re-columning processes.
- Successfully re-columned four CGA packages with 15-mil column diameter; all solder joint column attachments exhibited acceptable visual quality.
- Prepared two boards for assembly, each having four and two packages with 20- and 15-mil re-column diameters, respectively.
- Utilized two mini-stencils for solder paste printing, one with 7/23 (thickness/aperture opening) and the other with 8/26 configuration.
- Individually placed each package onto the board using a rework station with optical inspection capability for accurate placement of CGA package onto board pattern with paste deposition.
- Assembled 10 re-columned, high I/O CGA packages using a vapor-phase reflow machine.
- Individually assembled two re-columned, high I/O CGA packages using a rework station to establish process steps for assembly and to determine if there are differences between the two techniques in terms of reliability and failures. A rework station is an option for assembly in a low volume manufacturing environment when generally only one or a few CGA parts are assembled onto board. Obviously, it is not an option for high volume manufacturing, but rework station still is used for rework of defected assemblies.

A fully populated board had 6 re-columned CGA1144 packages. All assemblies exhibited acceptable—although, in many cases, not ideal—solder joints at the board side, indicated by visual inspection and verified by daisy chain resistance measurement. Inspection of solder joints at the package side is more difficult to

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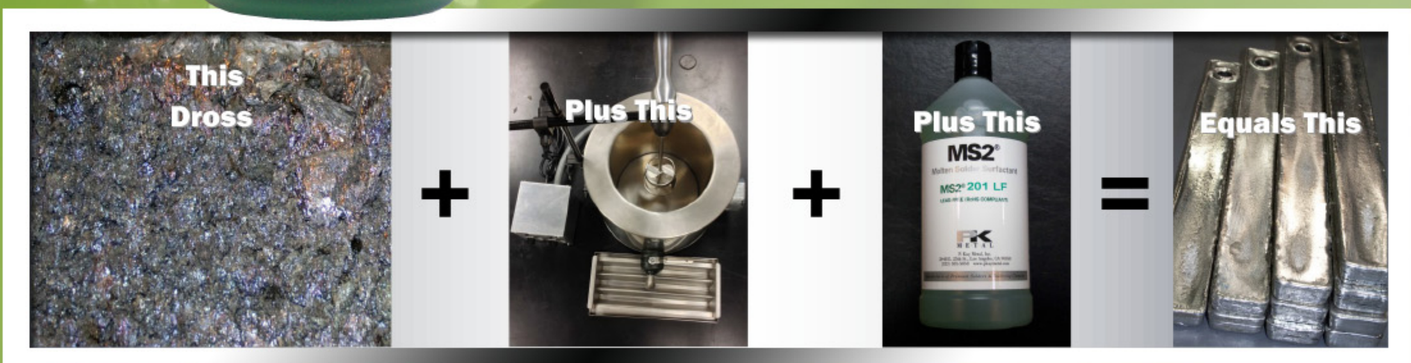

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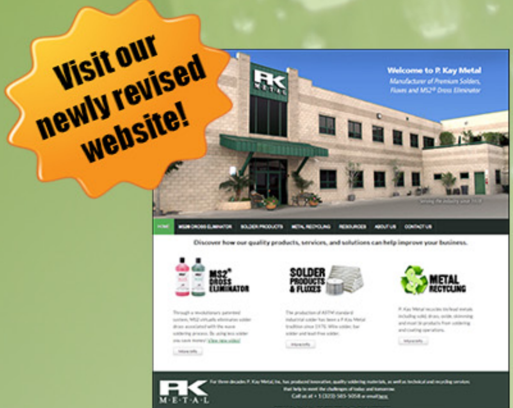

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perform, but from what was observed, they also appeared to be acceptable. The two test vehicles built under various manufacturing processing conditions were subjected to thermal cycling. Only a representative test result is discussed below.

CGA1144 Package Re-column

Re-columning was performed using Cu-spiral columns at the same facility that CGA560 packages were re-columned. Two re-column sizes were used, one with 20- and the other with 15-mil diameter. Photomicrographs of the two re-columns at a low and a high magnification are compared in Figure 13; the right side shows the 20-mil diameter columns. Except for the column size differences, solder joints for both conditions have visually acceptable quality with shiny appearance and good fillets. No pull testing was performed; therefore, the tensile strength differences between the two column sizes are unknown.

Stencil Design, Paste Deposition, and Volume Measurement

The stencil thicknesses were 7 and 8 mils, and the two aperture openings were 23 and 26 mils for low and standard volume conditions, respectively. An RMA tin-lead paste was used for paste printing using automatic manufacturing parameters. Figure 14 depicts a photo of a board in which all six CCGA patterns were individually paste printed using a mini-stencil. After printing, each paste print on the PWB was visually inspected for gross defects such as bridging or insufficient paste. On rare occasion, quality of paste deposition was improved by adding a small amount of paste when insufficient paste was detected. When bridging was discovered, solder paste was removed to open the bridge. In some cases, when the prints had offsets larger than acceptable levels, they were cleaned and reprinted for the second time. Figure 15 depicts optical photomicrographs showing acceptable paste deposition quality (left) and reject quality (right).

Solder paste volumes for selected pads were estimated using a laser profilometer with 3-D dimensional measurement capability. Solder

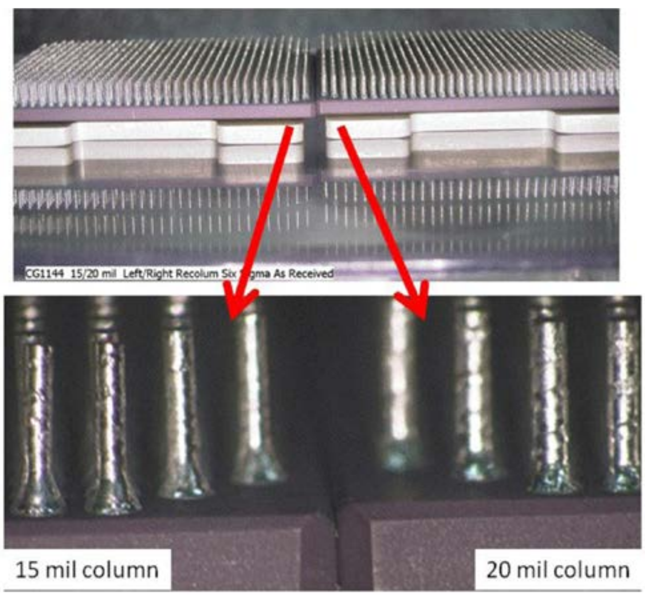

Figure 13: Photomicrographs of the two sizes of re-columned packages (20- and 15-mil columns) at low and high magnifications.

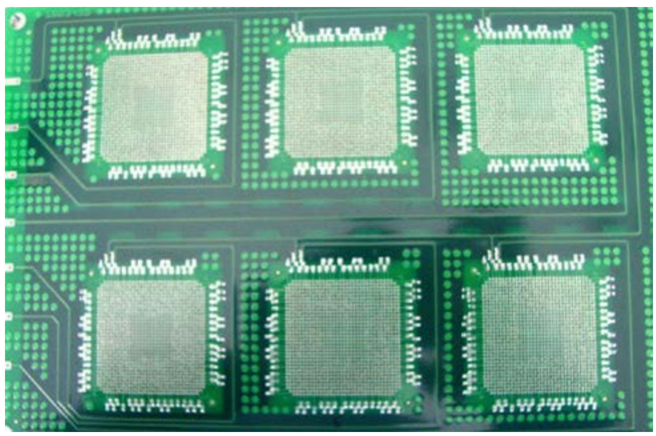

Figure 14: Optical photo of a high I/O CCGA board after paste printing with a ministencil.

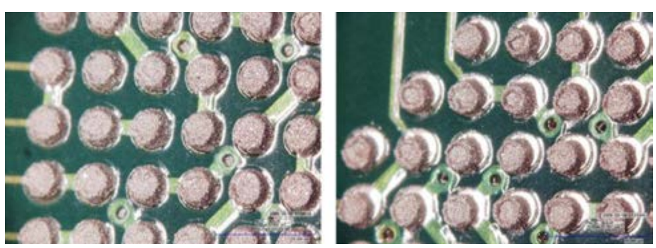

Figure 15: Optical photomicrograph of paste deposition with mini-stencil with acceptable solder paste quality (left) and reject (right).

paste areas and heights were measured for solder volume documentation. Measurements were made at numerous locations—including corner and center pads—to gather solder volume data and their corresponding distributions. An example of photomicrographs of paste deposition with 7/23 mini-stencil (thickness/opening) after paste printing, estimated/calculated solder paste volumes on each pad, and color-coded paste height distribution measurements are shown in Figure 16. Similar information for the 8/26 mini-stencil (thickness/opening) is shown in Figure 17.

Figure 18 depicts an assembled test vehicle with six high I/O packages. Note the input and output traces extending to the board edge and also the probing pads at the package peripheral for manually detecting failures.

Inspection before Environmental Tests

Visual inspection using an optical microscope was used during assembly to optimize processes based on the visible outer-row column solder conditions. Visual inspection was also performed prior to and during thermal cycling to determine quality of solder joints both at the package and at the board sides. The degree of damage progress in columns and solder joints with cycling was also monitored. Even though only peripheral column interconnections can be inspected, such inspection provides valuable information for CCGA assembly quality and reliability. It provides not only information on solder joint quality, but also on solder damage progress and failure mechanisms since generally CTE mismatch failures first occur in the corner and outer-row columns.

However, for re-columned CCGAs, it was soon recognized that interface close to the package pad are more critical than solder joint quality at the board side. It is more difficult to inspect and document solder joint quality and interface integrity at the package side because the large board area in package vicinity interferes with optical lenses. For this reason, after cycling, boards were cut close to the package body and visually inspected for better identification of damage and cracking even though it is realized that this was not a representative of inspection for hardware. Optical and SEM photomicrographs were taken before X-sectioning.

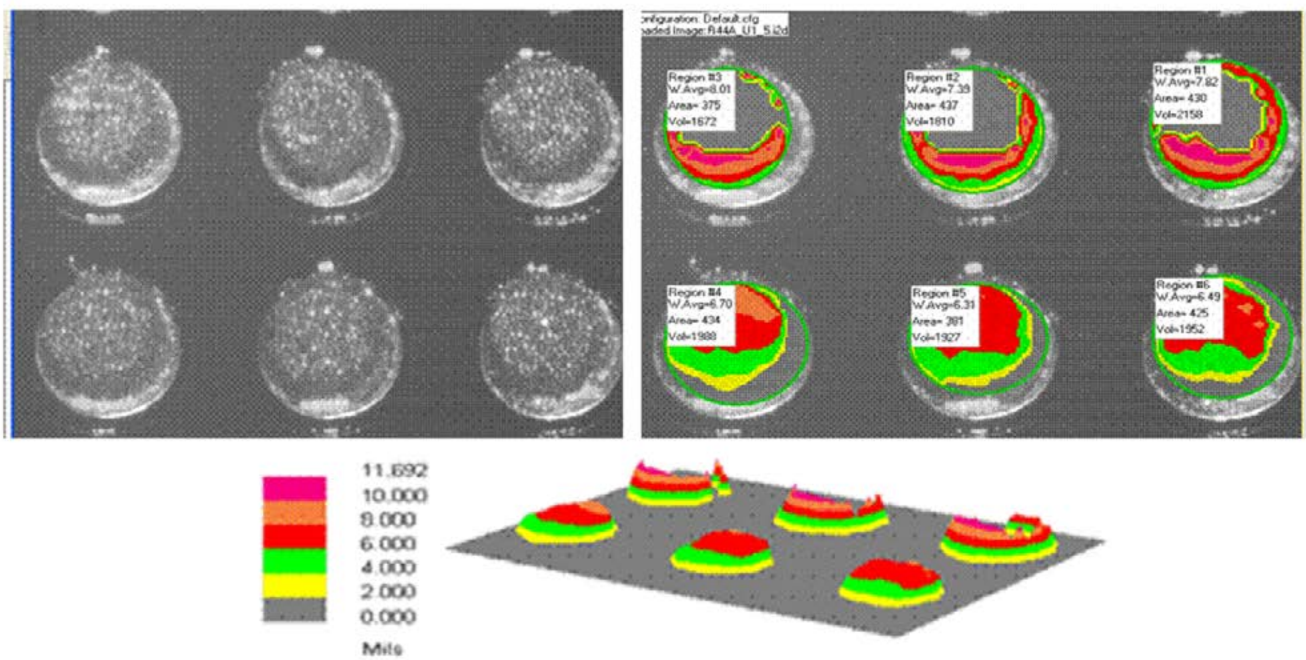

Figure 16: Optical photomicrograph and measured/calculated solder paste information for paste print with ministencil with 7-mil thickness and 23-mil aperture opening diameter.

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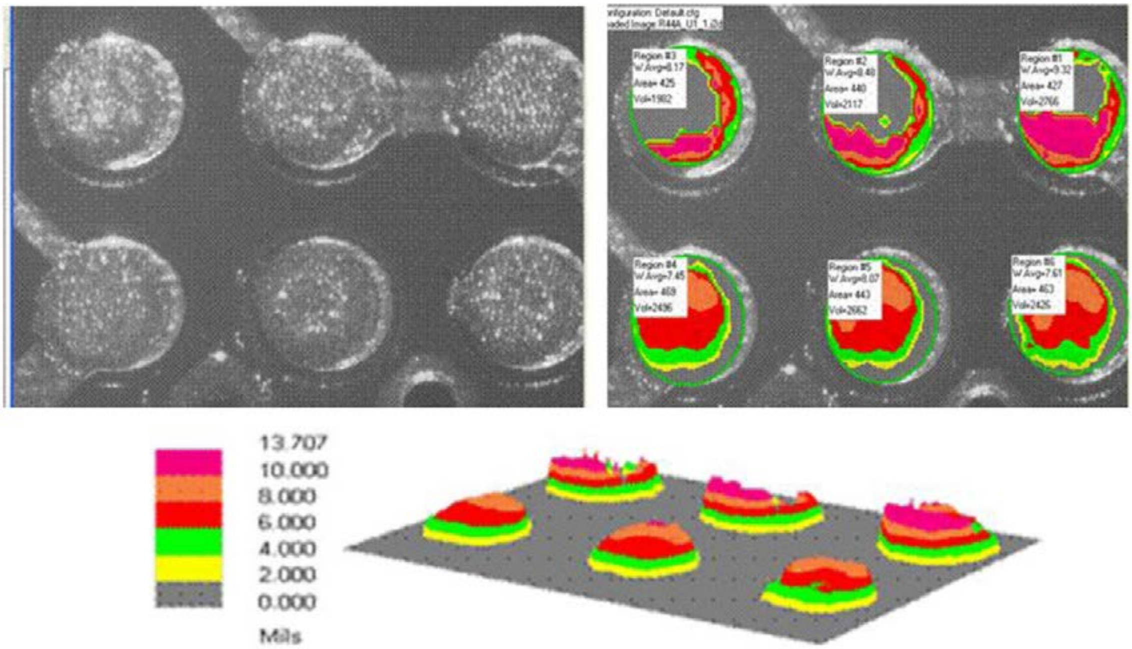

Figure 17: Optical photomicrograph and measured/calculate paste information for paste print with ministencil with 8-mil thickness and 28-mil aperture opening diameter.

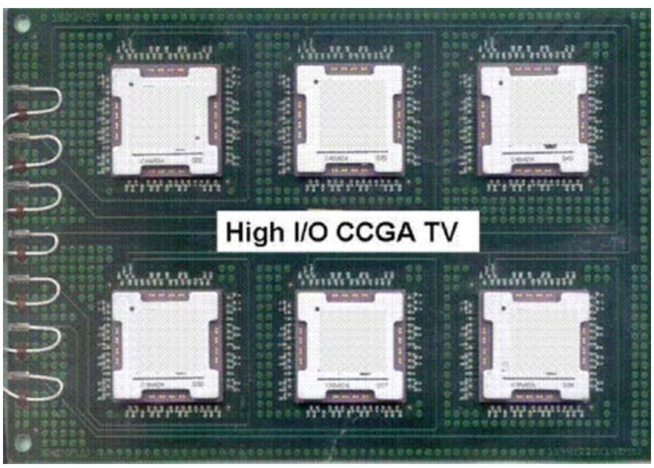

Figure 18: Photograph of an assembled test vehicle having six re-columned, high I/O CGA packages.

Test Results after Thermal Cycling for CGA1144 Assemblies

Thermal Cycle Condition

Only the Cycle C condition, ranged from -120° to 85°C with about 5°C/min heating/cooling rate and 10-minute dwells, was selected to characterize thermal cycle behavior of the two test vehicles, each having six high I/O CCGA package assemblies.

To better characterize microcrack formation of re-columned package assemblies, two packages were cut close to the package body for optical, SEM, and cross-sectioning. Because of potential failure of re-columns at the package side, it is critical to be able to inspect them; however, it is generally difficult to inspect assemblies at the package side because of board obstruction. Inspection of solder joints at the board side is easier since solder joints are blocked only by package periphery. For this reason, a thorough optical inspection was performed for two package assemblies after cycling and cutting for X-sectioning. Representative optical photomicrographs of the solder joints at the package side from the cut sample are shown in Figure 19. This figure also includes the pseudo 3-D optical photomicrograph, which is a compilation of images from different optical focus layers. If the optical lenses are aligned correctly with solder joints at the package interface, it is possible to reveal finer microcracks that are generally difficult to detect for a non-cut package assembly.

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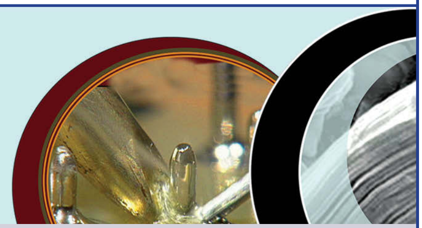

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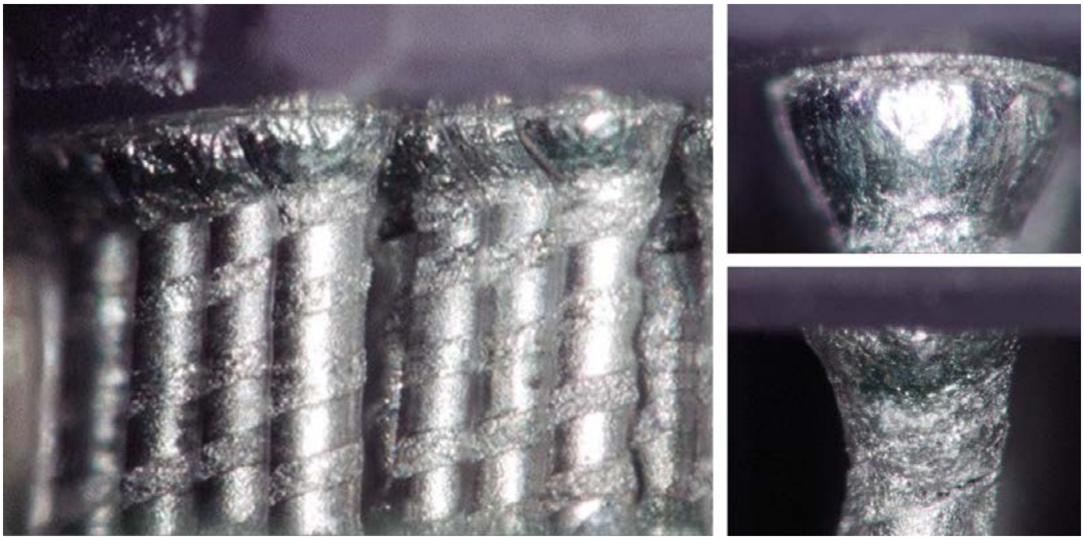

Figure 19: Representative optical photomicrographs, including those with pseudo 3-D optical photomicrograph, showing damage and microcracks at the package side.

Photomicrographs clearly depict damage at the package side and even microcracks near the pad interface taken at much higher magnifications. Note that these microcracks could not have been detected during routine optical microscopy evaluation since they are fine and also close to the package interface, making it difficult to detect, as mentioned earlier. Note that these microcracks were first revealed during SEM evaluation at much higher magnifications, and then searched for during an optical inspection.

Conclusions

Key findings based on column attachment and re-assembly of CGA packages onto PCBs which were subjected to a number of thermal cycles are as follows:

• The Cu-spiral re-column version of the CGA560 package without its original ceramic interposer layer exhibited good attachment interconnection strength as re-columned and after exposure to isothermal aging at 125°C up to 500 hours.

• Based on only a few test samples subjected to thermal cycling and visual inspection, it appears that re-columned CGA60 package with no interposer is a viable rework solution from an assembly perspective only. Further work is required to substantiate these test results for an active-die version.

• All CGA1144 assemblies with re-columned packages passed 200 severe thermal cycles (–120°/85°C) with no apparent visual damage or daisy chain failures.

• Based on limited thermal cycle test results and visual inspection during thermal cycling, it appears that re-columning of CGA1144 is a viable option from a solder attachment perspective only.

Acknowledgments

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The author would like to acknowledge A. Mehta, N. Neverida, and R. Ruiz at JPL for their support in test vehicle assembly, thermal cycling, and failure analysis. Thanks also to column attachment manufacture's personnel for providing service and support. The author extends his appreciation to program managers of the NASA Electronics Parts and Packaging (NEPP) Program, including Michael Sampson, Ken LaBel, and Dr. Charles Barnes and Douglas

Sheldon for their continuous support and encouragement. **SMT**

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Dr. Reza Ghaffarian has more than 30 years of industrial and academic experience. For the last 19 years at NASA's JPL, he has led R&D activities on reliability and quality assurance in advanced electronics packaging and has been a consultant resource for most JPL spaceflight projects including Mars Curiosity Rover.

Mil/Aero007 News Highlights

Saline Lectronics Achieves Distinction with AS9100C Audit

The company has completed its AS9100 Certification for the fifth year in a row, and this year received a "Best-In-Class" distinction. Saline Lectronics is now certified to AS9100 Revision C, the fourth and latest release of the AS9100 standard, which takes in the revised requirements of ISO 9001:2008 and nearly 100 additional criteria specific to the aerospace industry.

SMTA Finalizes Counterfeit Electronic Parts West Program

SMTA and CALCE are pleased to announce that the program for the Counterfeit Electronic Parts and Electronic Supply Chain Symposium West is finalized and registration is open. This symposium will provide a forum to cover all aspects of changes in the electronic parts supply chain on how an organization performs part selection and management through the entire life cycle.

Conflict Minerals Issues Reach Far into Europe

Under pressure by U.S. laws, human rights campaigns, and guidance from the Organisation for Economic Co-operation and Development, European companies are already being asked by their customers to declare the use of conflict minerals.

U.S. DLA Program Mitigates Risks of Counterfeit Electronics

A little over a year ago, an initiative by the U.S. Defense Logistics Agency launched, aiming to sharply mitigate the risks of counterfeit electronic parts entering the military supply system. The effort featured SigNature DNA, an advanced anti-counterfeit technology platform. The initiative has already begun to pay off.

Cirtronics Achieves AS9100 RevC Certification

Cirtronics Corporation, a New England-based EMS provider, is proud to announce it has achieved quality certification to AS9100 RevC. AS9100C certification is an internationally recognized quality management standard for the aviation, space, and defense industry.

Sanmina's Mexico Plants Earn Diebold Awards

Sanmina Corporation, a leading integrated manufacturing solutions company making some of the world's most complex and innovative optical, electronic, and mechanical products, has announced that its Guadalajara, Mexico operations are the recipient of Diebold, Incorporated's 2012 Gold and Silver awards for quality and performance.

Blackfox Debuts IPC Course Focused on Space Assemblies

Blackfox announces the latest addition to their IPC industry-developed and approved program curriculum, IPC/WHMA-A-620 Space Hardware Addendum. As a follow up to the IPC/WHMA-A-620B course, the space addendum provides additional requirements to ensure the performance of cable and wire harness assemblies that must survive in space.

Axis Electronics Hosts SC21 Best Practice Supplier Event

The event focused on the successful implementation of SC21 tools within Axis Electronics to drive business and service excellence, helping Axis customers deliver excellence to end customers.

Tin Whiskers Symposium Presented by IPC, CALCE

"IPC and CALCE share a common goal of helping to educate the industry on the latest information about tin whiskers theory and practice," says Sanjay Huprikar, IPC VP of member success. "This partnership has expanded the reach of both organizations, allowing us to develop a strong agenda with presenters who have deep knowledge of the complex technical challenges related to tin whiskers."

EVOLUTIONARY SOLUTIONS

Power of the People

by Karla Osorno
EE TECHNOLOGIES

State of the art is defined as the highest level of development of a device, technique, or scientific field, achieved at a particular time. So it makes sense that one important criterion for OEMs would be an EMS who has state-of-the-art facilities in which to build state-of-the-art products.

Five key areas of development make all the difference when it comes to achieving state-of-the-art status: people, equipment, building, culture, and systems. All are important. However, these are not enough to manufacture state-of-the-art products. The power lies in the people.

Secret Sauce

People are the secret sauce. And when the secret sauce is missing, success is not possible. Significant pain and failures result even when all areas except the people are state-of-the-art.

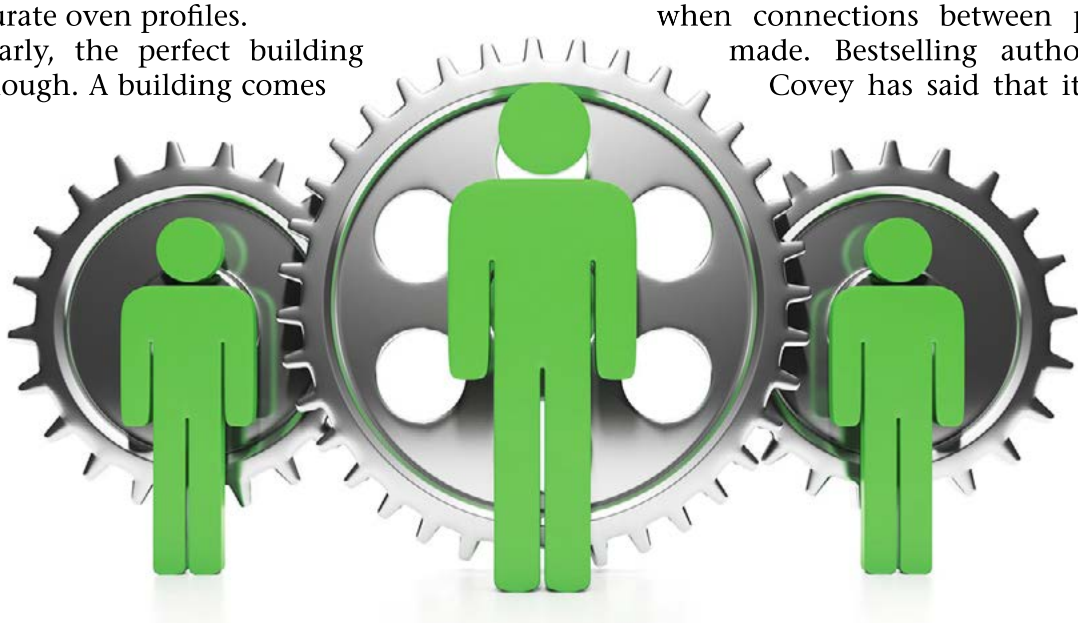
Imagine having state-of-the-art equipment and not having the right people to run it. On a surface mount line, the equipment is important to consistency and efficient throughput, and pain points develop when an operator makes repeated mistakes that result in misprints, assembly of wrong components or poor soldering due to inaccurate oven profiles.

Similarly, the perfect building is not enough. A building comes alive only when the right people are inside, in the right positions, getting results.

Culture refers to the cumulative deposit of knowledge, experience, beliefs, values, and attitudes by a group of people. A manufacturing plant with a dynamic, positive, problem-solving culture and the wrong people is a plant that is not going to thrive. Employees who approach the day with an attitude of independence and a lack of teamwork negatively affect the number and quality of units shipped that day.

Logical and effective systems in a plant impact costs and service and enhance long-term relationships. People are what bind these systems together. Ineffective people who ignore processes, systems and procedures compromise quality, resulting in rework carts everywhere.

We can all think of an example in the service realm of companies who have created the perfect environment with regard to equipment, buildings, culture and systems, but the wrong customer service experience. When a greeting, conversation, or interaction with an employee is negative, or even neutral, the degree of cleanliness of the floor or the efficiency of the cash register does not matter. Impressions are made when connections between people are made. Bestselling author Stephen Covey has said that it takes five




Why did you choose THAT fabricator?

deposits into an emotional or relationship bank account to offset one withdrawal.

In the product manufacturing world this looks different and yet the principle is the same. Success, for an EMS company, begins and ends with people—its team of employees. Interactions with customers matter and exemplify Covey's theory about relationship bank accounts.

The Power of 5:1

Delivering good news to customers on a regular basis will be critical to maintaining a strong relationship bank account. It may be tempting to communicate only when there is a problem, but this can be dangerous because the withdrawals will outweigh the deposits. When people have an attitude that no news is good news, the relationship will suffer long term. Simply delivering quality product on time is not enough. Effective people are those who understand the significance of daily decisions on company results.

Communication and relationships between employees matter to an even greater degree. The complexity and sheer volume of transactions and decisions made in a typical day of manufacturing necessitate people communicating effectively. People are critical to properly optimizing all of the other areas required for state-of-the-art status, which is why it all begins with hiring practices.

Hiring

When hiring, an EMS company should look for the right person who can handle the defined job responsibilities and be a good fit with the rest of the team, with the same core values as corporate. A few general requirements make a person qualified to work in any industry: honesty, strong work ethic, and desire to contribute. For our industry in particular, a job description should identify key education and skills that are required for success. Education may vary, however, candidates who demonstrate initiative, persistence, and commitment in their educational pursuits are more likely to fit into our industry's continually changing environment. Skills may range from general technical or mechanical skills to more highly skilled operators and engineers. For the basic skills, demonstration comes with work experience, schooling, or even skills used in hobbies. For the more highly skilled positions, demonstrated work experience and education must be required.

A hiring team may want to look for more soft skills such as talent and attitude rather than skills and knowledge (TASK). Talent and attitude cannot be taught. Skills and knowledge applicable to the company and specific industry can be taught via formal and informal training.

"All new employee training should begin with an orientation in which the company history, vision, mission, values, safety and general procedures are described."

Training

When hiring is done right, most people come to any new position with the required skills and abilities. However, company-specific processes and systems must often be learned. Therefore, training on company procedures, processes and systems should be covered in the first 90 to 180 days.

All new employee training should begin with an orientation in which the company history, vision, mission, values, safety and general procedures are described. This will acquaint new hires with their role in furthering the company's success and familiarize them with the overall processes and systems of the organization.

For production employees in a manufacturing plant, a specific production orientation is effective and may take the shape of a weeklong program in which employees will be taught the basics about working on the production floor. Procedures and activities such as scanning time to jobs, electrostatic discharge controls, component handling, and importance of process controls, quality and equipment maintenance are among the various topics that are important to cover.

A great way to ensure that skills training requirements are communicated, scheduled, executed and evaluated is to have a training policy and plan. Software programs can help you to manage these details and provide reporting, or a company can manage this by simply using a spreadsheet tool like Excel.

The best processes use software to manage the training program so there are no tracking or training gaps. Requirements should be entered by job title initially to provide consistency across the company and match job description requirements. Requirements may also be added based on individual or departmental needs or in response to quality issues identified where training could improve the situation in the future.

New employees should be given a training plan that outlines expectations and provides a map of what courses are required, including a deadline for completion.

Recordkeeping of completed and outstanding training may be used by supervisors to assess skill sets of the individual and the department. Supervisors appreciate recordkeeping and reporting because they can see exactly what is needed and who is qualified to complete an activity. For example, if a supervisor needs a solderer, he can review the training records and choose a solderer from all employees even if that person's primary job responsibilities are in another area. They can also build strength in an area by using the reporting to create cross-training plans. This leads the supervisor to seek opportunities for the employee to grow.

Growing

Attending training is not enough. Employees must grow in their knowledge and skills for the training to be effective. To ensure success, classes must be consistent between departments, provide a variety of assessments and include an instructor review at the end.

On-the-job performance assessment is the next step. For example, an employee taking a project management course should be asked to lead a project and then assessed. Results of the assessment should be acted on so that the employee grows.

Leading

Strong trainers and supervisors should lead their teams to achieve their individual goals and objectives. In a comprehensive training program, some general areas of classes to consider are leadership, technical skills, employee development, technology instruction, and certifications.

Some suggested classes to offer include:

- Leadership Toolbox
- Company Values in Action
- Lean Manufacturing
- Drawing Reading
- Internal Audits
- Management Action Programs
- AOI Operator Training
- Aegis Operation
- Certified Test Operator
- Certified SMT Operator Training

Some leadership will come via informal methods. Problem-solving conversations and character development conversations provide leadership opportunities for supervisors. Communication and relationship development within departments and across departments should also be established through meetings or shadowing.

Employees should be encouraged to shadow other departments, especially the department in the process flow directly before them and directly after them. Understanding the source of inputs to their operations and the impact of their outputs on the next operation is helpful for the employee to make more relationship deposits than withdrawals.

The hiring, training, growing, and leading of employees is required for achieving state-of-the art people—a requirement for achieving strategic objectives. The power of people to achieve state-of-the-art status cannot be understated, and yet it is only one area for an EMS to consider. Stay tuned for more on creating a state-of-the art manufacturing organization. **SMT**

Karla Osorno is business development officer for EE Technologies, Inc., an EMS provider delivering complete engineering and manufacturing services with locations in Nevada and Mexico. To read past columns or to contact Osorno, click here.

SMTonline Supplier/New Product News Highlights

GE Acquires Imbera Electronics

GE Healthcare Finland Oy, in partnership with GE Idea Works, announced today that it has completed the acquisition of Imbera Electronics Oy, a pioneering Finnish company that has spent over 10 years developing advanced embedded electronics packaging technology and manufacturing solutions.

Absolute EMS Adds CyberOptics SPI & AOI Systems

CyberOptics Corporation a world leader in AOI and SPI inspection solutions for the global electronics assembly and semiconductor capital equipment markets announces that Absolute EMS has purchased both its SPI and AOI inspection systems as part of its recent expansion.

Ellsworth Expands with Henkel Loctite Multicore HF 212

Ellsworth Adhesives adds new Henkel Loctite Multicore HF 212 to its ever-expanding range of products. The Electronics Group of Henkel has just launched Loctite Multicore HF 212, a halogen-free solder paste ideal for high value PCB assemblies, and, starting today, you can purchase this new product from Ellsworth Adhesives Europe.

Pulse Integrates SMT Components on LDS Antennas

Pulse Electronics Corporation, a leading provider of electronic components, now announces in-house capability to integrate passive surface mount technology components on 3D laser direct structuring antennas.

Viscom Introduces New Inspection System

The new Viscom S3088 Conformal Coating Inspection system inspects coatings quickly and reliably for typical defects such as cracks, bad spots, layers that are too thin or too thick, smearing, impurities, or splashes. Transparent protective coatings contain UV fluorescent indicators that emit visible light, allowing automatic optical inspection.

Agilent Debuts Fully-automated Inline ICT Solution

Agilent Technologies Inc. has introduced the fully-automated Medalist i3070 Series 5i Inline In-Circuit Test System. With a compact chassis, the system uses 33% less floor space than conventional 3070 systems.

Fujipoly Introduces New Sarcon Interface Material

Fujipoly's new Sarcon GR25A-0H2-30GY is a 0.3 mm thick, low thermal resistance interface material with a low-tac surface on both sides. This special treatment dramatically reduces material tearing and damage during assembly and rework operations.

Koh Young America Expands; Moves to Larger Facility

Koh Young Technology, a global leader in 3D measurement technology for electronics assembly, announces the relocation of Koh Young America's offices, process development lab, and showroom to a larger facility nearby.

P. Kay Metal's MS2 Receives Patent Allowance in Korea

Dan Feinberg, vice president for the MS2 group, noted, "The combination of additional patents allowed for MS2, as well as the new offline method of use in conjunction with the new DOFFS offline equipment, is greatly adding to the global acceptance of this process and recognition of the very significant cost saving realized by our global customers."

Balver Zinn to Sub-license Nihon Superior's SN100C Patent

Balver Zinn has been granted the right to sub-license the SN100C® patent by Nihon Superior Co. Ltd. Tetsuro Nishimura, president of Nihon Superior Co. Ltd., and Josef Jost, president of Balver Zinn, recently met and finalized the details of the agreement under which Balver Zinn now has rights to sub-license its patent for the SN100C alloy globally, with the exception of the United Kingdom and Ireland.

SMT TRENDS & TECHNOLOGIES

Pick and Paste

by Eric Klaver
ASSEMBLÉON

What defines a good electronic product coming from a production line? All process variables need to be 100% without any influence from outside, which means all machines producing in exactly the same way, in exactly the same environment. In the printer, for example, the paste must be evenly distributed at exactly the right locations and in exact amounts. The pick-and-place equipment must place components precisely, with the right force at the right board coordinates—and all perfectly cured in the oven.

The reality is normally quite different, which explains the need for inspection units in the line to verify various steps in the production line. One of these units is the solder paste inspection (SPI) system. Offsets can be determined by solder paste inspection and results fed back to the printer (paste volume data) or downstream equipment (paste offset data).

Solder Print Offsets

At the pick-and-place equipment, the actual mount data (coordinates plus correction) is based on a calculation based on reading fiducial marks. The result is a placement according to CAD data. However, even if all seems to be correct, the board yield will not be undesirable if all process variables are not what they are supposed to be. Solder print offsets, for example, will eventually lead to board errors (Figure 1). This is most problematic for components requiring highly accurate placement, or very small components like 08004, 01005, 0201 and Rnets.

A number of factors can cause the offset. The quality or accuracy of the stencil or the PCB itself is important, for example. Temperature changes (which can differ for each system in a production line!) can cause boards or stencils to shrink or stretch. And with board stretch that may differ per system in the flow line, how accurate and transferable is the SPI information when the boards can differ within every machine?

Correcting Process Variables at the Pick-and-Place Equipment

For best possible board quality, some of the functions of the SPI are therefore being taken over by the pick-and-place equipment itself. If

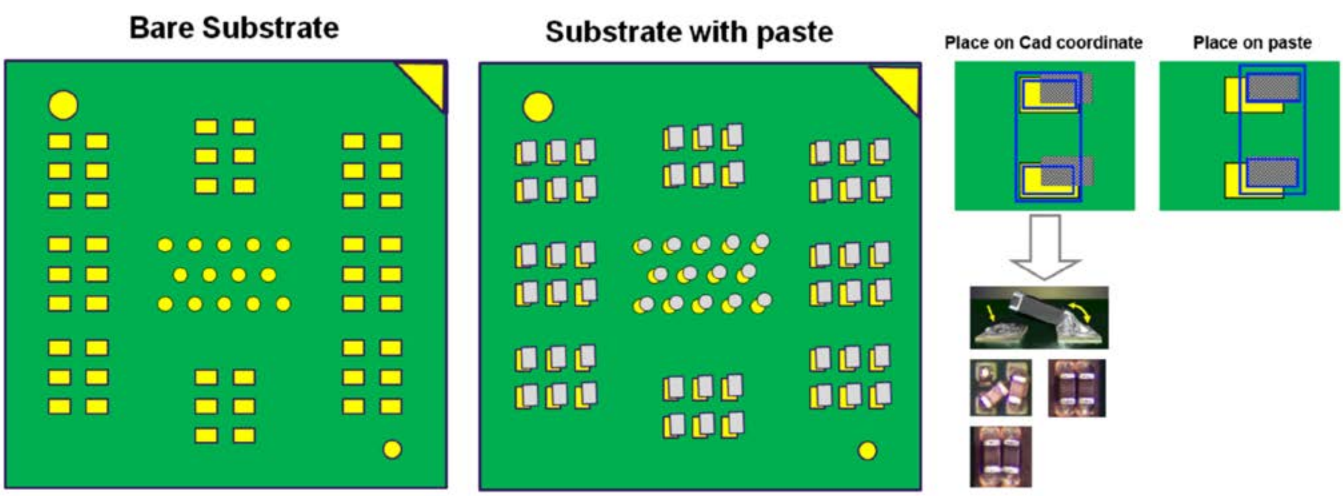


Figure 1: When placing on CAD coordinates, paste offset may lead to defects.

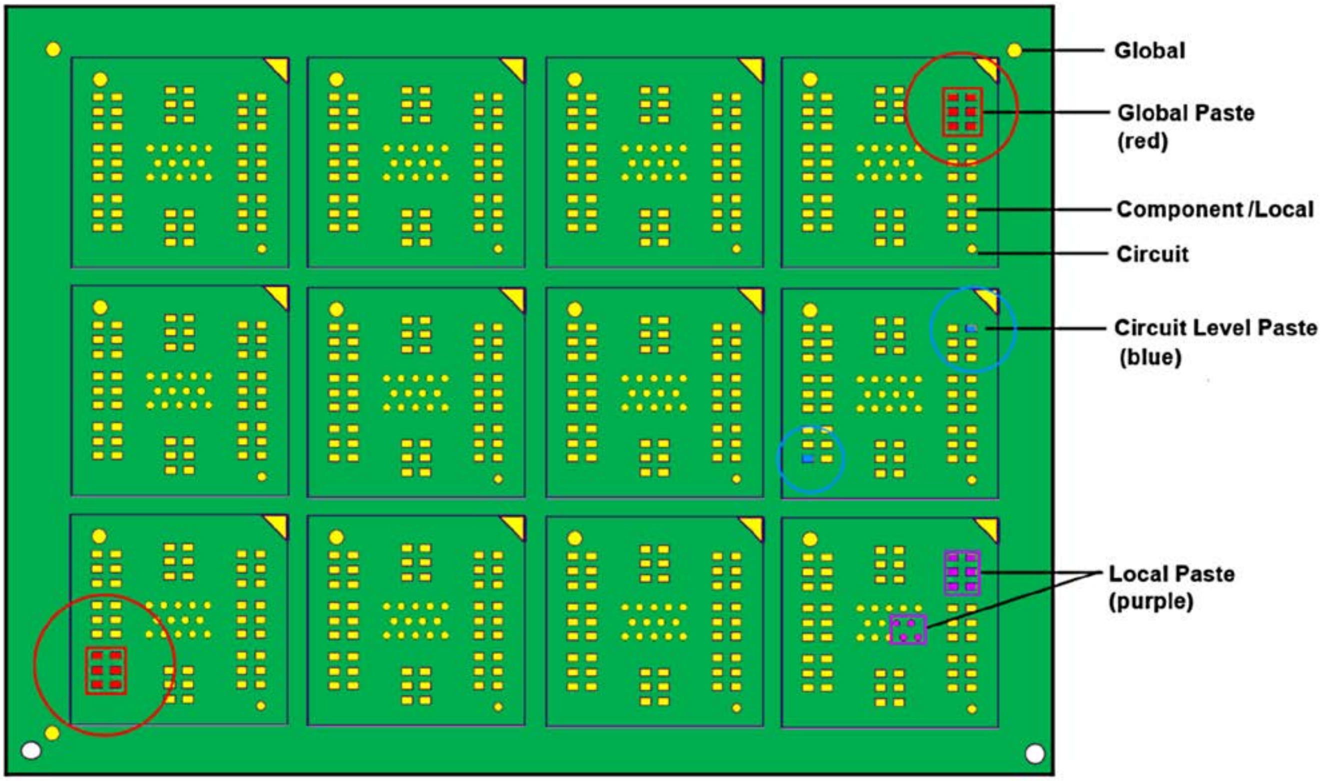


Figure 2: Fiducial locations.

the solder amount is generally sufficient and paste offsets are causing most of the issues, then the pick-and-place equipment can perform offset inspections and there is no need for additional equipment. Instead of the standard fiducial alignments (Cu fiducials), the placement coordinates are then based on paste fiducial alignment. The algorithms for recognizing paste fiducials are rapidly improving to raise overall board quality.

Depending on the components and required output—and just as with standard fiducials—global paste fiducials, circuit paste fiducials or even component paste fiducials can be used (Figure 2). Using global fiducials will keep the recognition time short, and the offset correction is applied to all subsequent placements for the highest outputs.

For critical components, or where the accuracy of a specific component is crucial, then the recognition of paste offset can be performed locally, too. Increasing the number of recognition steps in the process may reduce the output, but will significantly improve the overall board quality.

A number of items need to be taken into account when recognizing and applying corrections based on paste fiducials. As can be seen in Figure 3, there are a number of contrast specific items that will determine correct recognition: the flux, solder mask, shadow, CU pad and the PCB material itself. The reliability of the data is determined by the recognition algorithms that can also interpret variations (irregularities) in paste shape or take multiple paste locations to maximize precision.

Additionally, algorithms must check on whether a measured paste offset is still within placement process limits (Figure 4). Too much offset may lead to poor soldering, tombstoning, bridging or shorts (especially when the interspacing decreases). Enhanced paste fiducial recognition algorithms must therefore also calculate the distance of the solder paste from the CU pad.

Three levels of fiducial recognition

To enhance the accuracy of alignment there are three levels of (paste) fiducial recognition

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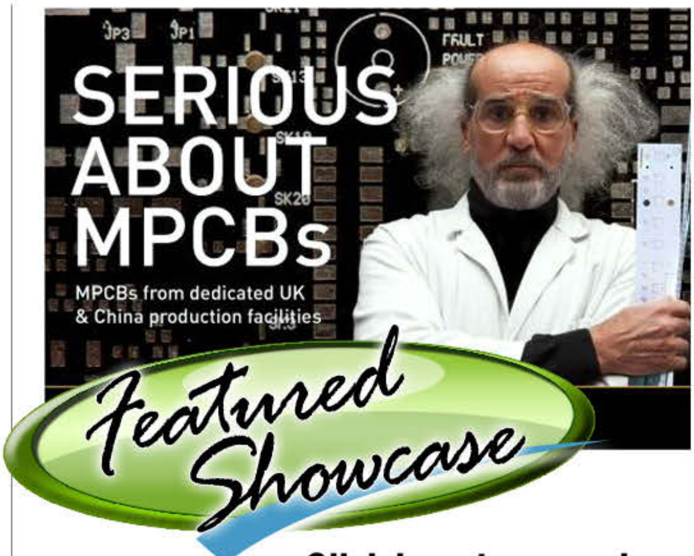

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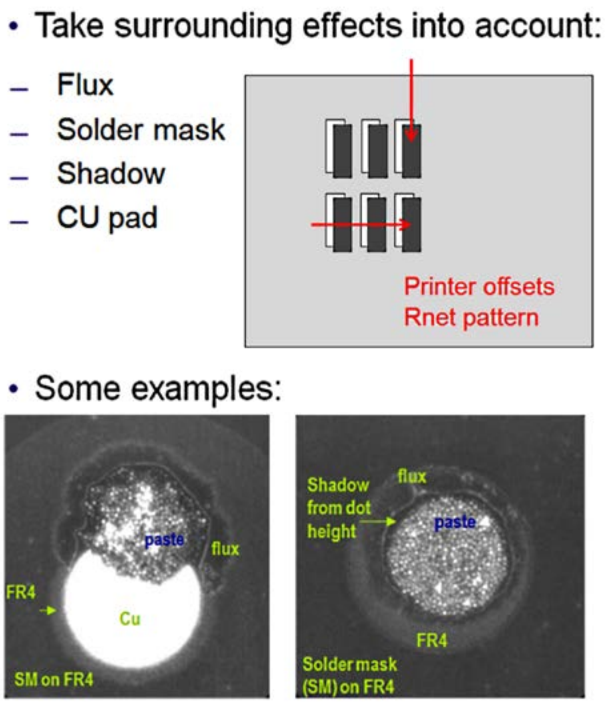

Figure 3: Factors to take into account for correct recognition.

types, basically also in order of eventual placement accuracy.

a) Single paste fiducial
b) Multiple fiducial
c) Pattern fiducial

Recognizing a single paste fiducial (Figure 5) is fast, but irregularities in the shape may still cause a slight offset. Recognizing multiple fiducials will average out all possible shape irregularities and

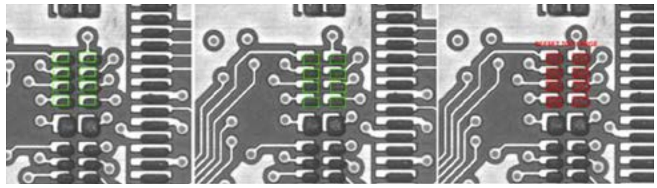

Figure 4: Paste offset—place on CAD coordinates, paste location or disallow.

so lead to better placement. Multiple fiducial recognition is done in one go and is therefore just as fast as recognizing a single paste fiducial.

Last is pattern fiducial recognition. This is a local alignment feature, which basically uses the landing pads of a component itself—and more local than this you cannot get. This feature is most useful if a particular component (flip chip, micro BGA) requires absolute placement accuracy.

Pick-and-place is a process, and as many process variables as possible need to be filtered for best possible product quality. Dealing with variable paste offsets is one process variable that can be successfully solved at pick-and-place level. **SMT**

Eric Klaver has been with Assembléon since 1998. Klaver specializes in vision technology and feeding and is currently the chairman of IEC work group TC40WG36, which specializes in component packaging. To read past columns, or to contact Klaver, click here.

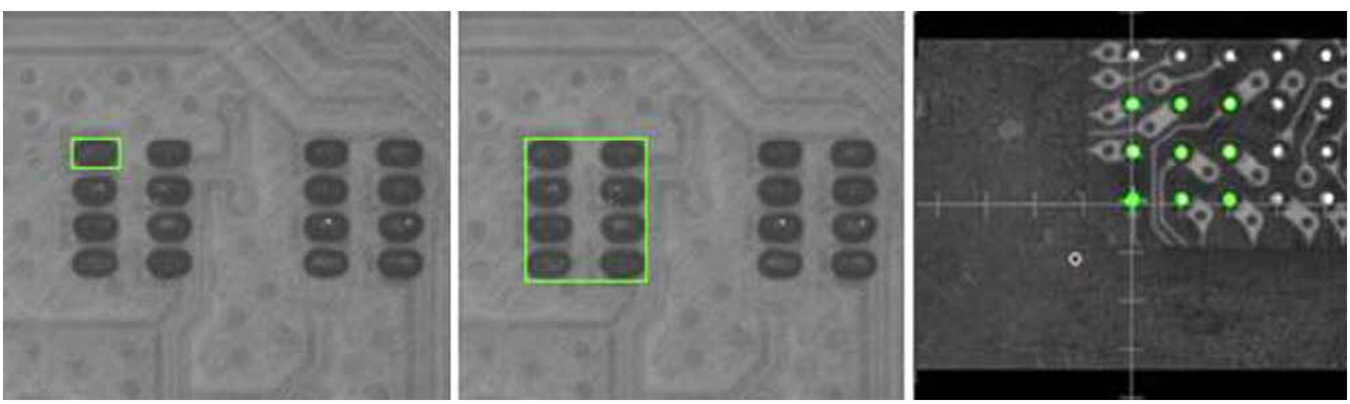

Figure 5: Single and pattern fiducial recognition.

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NOVEMBER RELIABILITY EVENTS

November 12–14, 2013 • Hilton Orange County • Costa Mesa, California

Sponsored by Lockheed Martin, the Tin Whiskers Symposium and Conference on Solder & Reliability provide comprehensive perspectives on lead-free reliability, from theory to practice. Subject-matter experts from academia and industry will provide insight for the challenges found in every market sector, including: military/aerospace, aviation, medical, automotive, telecom and consumer electronics.

IPC calce

7th International Symposium on Tin Whiskers

Tuesday, November 12, 8:00 am–5:00 pm
Networking Reception 5:00 pm–6:30 pm

Wednesday, November 13, 8:00 am–12:00 pm

Learn from:

- CALCE–University of Maryland
- Lockheed Martin
- Rockwell Collins
- Purdue University
- Raytheon
- Auburn University
- Celestica
- Brown University
- BAE
- Loughborough University
- Bosch
- And more ...

Explore the full range of tin whiskers challenges:

- Causes of growth
- Risk mitigation
- Materials perspective
- Methods for detection
- Failure analysis

View Agenda

IPC

IPC Conference on Solder & Reliability

Wednesday, November 13, 1:00 pm–5:00 pm
Thursday, November 14, 8:00 am–5:00 pm

Learn from:

- Indium
- MacDermid
- Sandia National Laboratories
- AIM
- CalTech Jet Propulsion Laboratory
- GE Oil & Gas
- Trace Labs
- MicroSemi
- Integral Technologies
- Celestica
- DfR Solutions
- And more ...

Focus on practical methodologies that can be deployed today:

- Strategic reliability considerations
- Solder alloys, low-temperature and laser soldering
- Pad crater risk assessment — and a “drop-in” solution
- Cleaning, contamination and corrosion
- Computational modeling and data interpretation

View Agenda

Sponsored by: LOCKHEED MARTIN

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TOP TEN

News Highlights from SMTonline this Month

① Electronics Industry to See Better 2013 and Early 2014

Business managers must constantly adjust their strategies by adapting to what's happened and what's likely to happen. World economies remain difficult to gauge as governments look at changing interest rates and many other factors cloud the outlook.

② Dr. Peter Diamandis to Keynote IPC APEX EXPO 2014

Peter Diamandis, M.D., has been selected through a vote of electronics industry professionals to present the opening keynote at IPC APEX EXPO 2014, in Las Vegas, Nevada. Diamandis is chairman and CEO of the X Prize Foundation, which designs and launches large incentive prizes to drive radical breakthroughs for the benefit of humanity.

③ Dr. Thomas Dekorsy Named GM of ESCATEC Switzerland

ESCATEC announces the appointment of Dr. Thomas Dekorsy as general manager of ESCATEC Switzerland, effective October 1, 2013. He replaces Gerhard Klauser, who will move to a new role heading up special projects.

④ eXception EMS Reaping Rewards of Globalization

eXception EMS, a leading UK-based EMS provider, has seen an increase of nearly 25% growth in sales over a two year period, and an order book increase of 35% since 2012. It now has more than 60 active customers across a variety of industry sectors including aerospace, energy, defence, semiconductor, and oil and gas.

5 Alchemy in the Electronics Era

The adage that the only constant is change always holds true in electronics. In some areas, like wire bonding inside chip packages, change doesn't occur too quickly. Many chipmakers and packaging companies have used gold wire bonds for decades, but some are moving away from the precious metal.

6 Sypris Strengthens Research Capability with Purdue

The newly-expanded research center will continue to focus on advancements in cyber security, as well as on network and critical infrastructure protection for government and commercial entities through Sypris' partnership with Purdue University's Center for Education and Research in Information Assurance and Security.

7 Flextronics Expands Energy Portfolio to Aid OEMs

Flextronics has announced an expansion of its portfolio of energy infrastructure solutions and services that will help original equipment manufacturers (OEMs) address regional shifts in the energy market by developing and delivering products to market faster, enhancing their regional market reach, and freeing up cash flow by leveraging Flextronics' global capabilities.

8 Huntsman Opens New Technology Center in Shanghai

The new $40 million facility forms an integrated technology and innovation campus together with the existing technology center opened in September 2008. The facility includes machine halls, laboratories, and offices and complement existing technology centers in The Woodlands, USA and Brussels, Belgium as well as smaller regional centers.

9 OnCore Expands; Opens New Product Design Center

In response to expanding customer interest in deeper engineering partnerships, OnCore has invested in the new Naperville, Illinois design center to house its expanding engineering team. The new team adds capabilities to increase both capacity and enhance design skill sets to engage customers early in the product development process.

10 IBL Acquires R&D Technical Services

"The acquisition of R&D Technical Services expands our existing footprint within North America both in terms of installed users and support. The addition of their rework systems also broadens our technical offerings. From a market impact standpoint, together we are now the world leader in vapor phase reflow systems," said Jochen Lipp, IBL Technologies' CEO.

EVENTS

For the IPC's Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar, click here.

For a complete listing, check out *SMT Magazine's* full events calendar here.

International Wafer-Level Packaging Conference
November 4–7, 2013
San Jose, California, USA

LA/Orange County Expo & Tech Forum
November 5, 2013
Long Beach, California, USA

MEMS Executive Congress US 2013
November 7–8, 2013
Napa, California, USA

Gartner Symposium ITxpo 2013
November 10–14, 2013
Barcelona, Spain

productronica 2013
November 12–15
Munich, Germany

SMTA/iNEMI Medical Electronics Symposium - Tabletop Exhibition
November 12, 2013
Milipitas, California, USA

Aerospace & Defense Programs
November 13–14, 2013
Phoenix, Arizona, USA

MILCOM'13
November 18–20, 2013
San Diego, California, USA

Energy Harvesting & Storage USA 2013
November 20–21, 2013
Santa Clara, California, USA

Printed Electronics USA 2013
November 20–21, 2013
Santa Clara, California, USA

Graphene LIVE!
November 20–21, 2013
Santa Clara, California, USA

OLEDs LIVE!
November 20–21, 2013
Santa Clara, California, USA

Supercapacitors USA 2013
November 20–21, 2013
Santa Clara, California, USA

HKPCA & IPC Show
December 4–6, 2013
Shenzhen, China

Austin (CTEA) Expo and Tech Forum
December 5, 2013
Austin, Texas, USA

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Next Month in *SMT Magazine:*

Our Columnists Speak

Next month, our veteran columnists will discuss the hits and misses of the industry in 2013, including their respective niches, and the people and equipment that made a difference.

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