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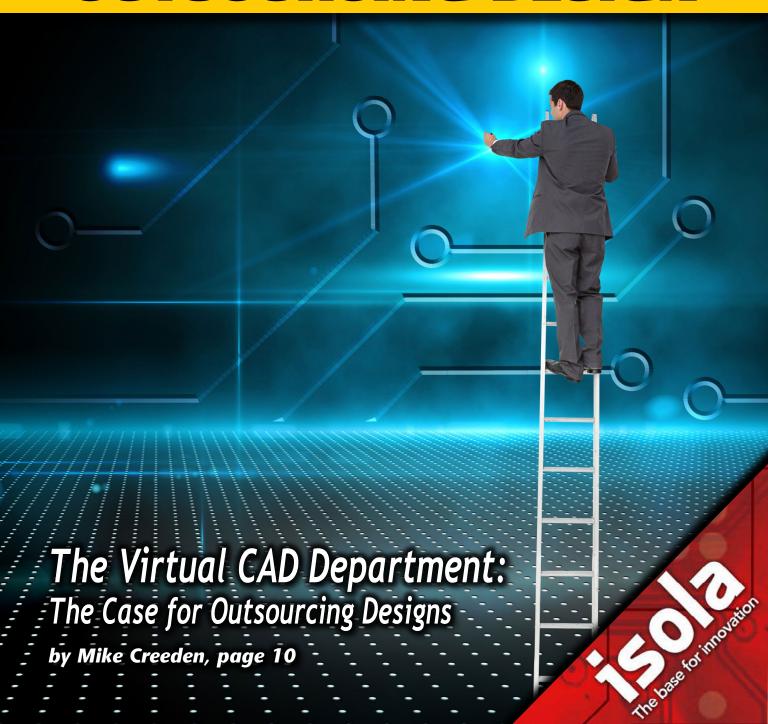
**Adding Value to Your Design Outsourcing Experience** 

by J. Kelly Dack p.18

ALSO:

**Component Selection** for Easier Design and Manufacture of Electronics by Joe Fjelstad p.26

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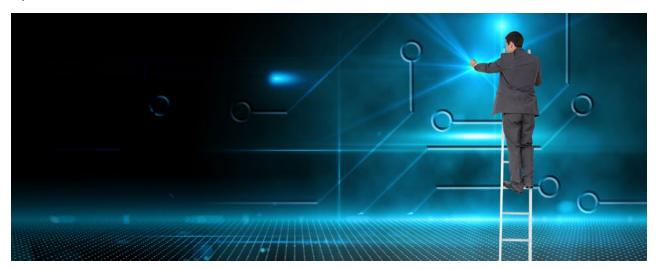


## This Issue: OUTSOURCING DESIGN

## **FEATURED CONTENT**

The term "outsourcing" often conjures up negative images of jobs being sent overseas. But some day, your team may need to send designs out, for a variety of reasons. This month, our expert contributors break down the ins and outs of outsourcing PCB designs.

## 10 The Virtual CAD Department: The Case for Outsourcing Designs by Mike Creeden



**18** Adding Value to Your **Design Outsourcing Experience** 

by J. Kelly Dack



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Df @ 10 GHz	0.0030	0.0017	0.0031	0.0028 - 0.0036
CTE Z-axis (50 to 260°C)	2.90%	2.90%	2.80%	2.90%
T-260 & T-288	>60	>60	>60	>60
Halogen free	Yes	No	No	No
VLP-2 (2 micron Rz copper)	Standard	Standard	Available	Available
Stable Dk and Df over the temperature range	-55°C to +125°C	-40°C to +140°C	-55°C to +125°C	-55°C to +125°C
Optimized Global constructions for Pb-Free Assembly	Yes	Yes	Yes	Yes
Compatible with other Isola products for hybrid designs	Yes	Yes	Yes	For use in double- sided applications
Low PIM < -155 dBc	Yes	Yes	Yes	Yes
NOTE: Dk Df is at one resin %. The data, while believed to be accurate and based on analytical methods considered to be reliable, is for information purposes only. Any sales of these products will be governed by the terms and conditions				

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## CONTENTS



**26** Component Selection for **Easier Design and Manufacture** of Electronics

by Joe Fjelstad



## **COLUMNS**

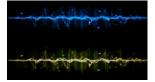
8 Who is Your EDA **Company's Customer?** by Andy Shaughnessy



34 Vertical Resonances in **Ceramic Capacitors** 

by Istvan Novak

40 Signal Integrity, Part 2 by Barry Olney



50 The Qualities of Great Bosses by Abby Monaco



54 The Key to Increasing **Quality: Bribe Your Employees** 

by Bob Tarzwell & Dan Beaulieu



## VIDEO INTERVIEWS

16 Mentor Fine-Tunes its Consulting **Operations** 



32 Imagineering's Dhanji on **Customer-Driven Technology** 



## **SHORTS**

- **39 3D Printing Incorporates Quasicrystals**
- **46 Tiny Carbon Nanotube Pores Make** Big Impact
- 53 New Material Could Pave Way for Flex Electronics, Displays

## **NEWS HIGHLIGHTS**

24 PCB007

48 Mil/Aero007

58 PCBDesign007



## **EXTRAS**

**60** Events Calendar



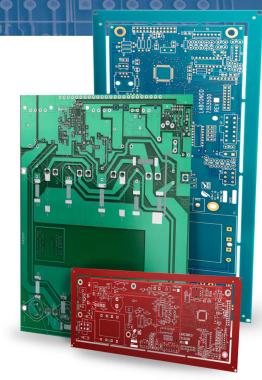
61 Advertiser Index & Masthead

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### THE SHAUGHNESSY REPORT

## Who is Your EDA Company's Customer?

by Andy Shaughnessy

I-CONNECT007

At first glance, that sounds like a simple question, with a simple answer. Some of you may be thinking, "I'm the EDA tool company's customer. My tool provider serves me, the designer."

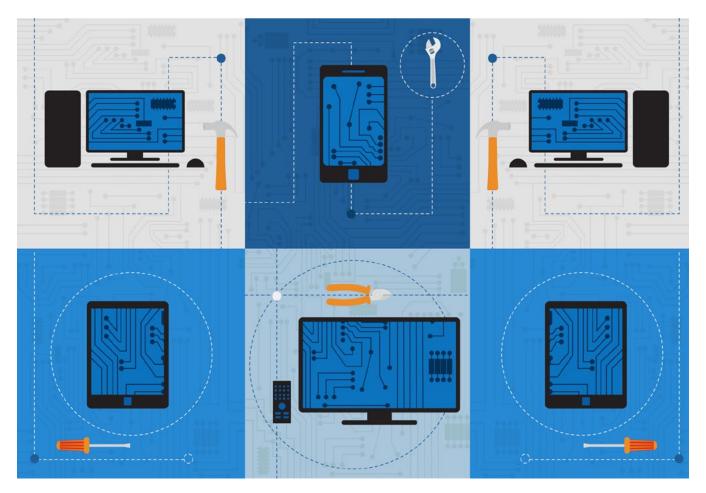
But I've heard from a growing number of PCB designers who disagree. Not all designers are in this group; it's definitely not a majority. But here's a helpful composite of the various stories I've collected from designers lately:

The company's designers discover that their company is considering a new layout tool when the CAD manager tells them. The CAD manager only found out by accident from his boss, or the purchasing manager, CTO, CEO, or any of the other executive types who need to sign off on

this sort of thing. If you're talking about multiple seats of software that runs around six figures (at least officially), the corner office folks will have to be involved.

So, the search for a new PCB design suite is underway. The designers have used other design tools at previous jobs, so they know a thing or two about the tool landscape. The designers do a little research, talk to their designer friends, check out a listserv forum or two, attend a trade show, and recommend the tool suite they think is best for their work.

Then upper management takes over, and upper management is not often composed of ex-PCB designers. Managers fly in reps from various EDA companies, and the three-hour



An EDA company rep

was listing all of the new

features of the latest rev

of their layout software,

and with every bullet

point, the designer would

whisper, "Who would

ever need that? Or that?

Who thought of this crap?

That's useless! So is that!

These features were added

### WHO IS YOUR EDA COMPANY'S CUSTOMER? continues

lunches ensue. Some designers say the execs make the final decision, and the designers are the last ones to know about the new tool.

One designer said his company made a tool purchase solely because his managers were good friends with an AE at a different EDA company. It's good to know the right people, and you should have a close relationship with your PCB design tool company.

None of which would matter if the designers still wound up getting the right tools for their particular projects. But too often, to hear designers tell it, their managers are swayed more by the EDA companies' marketing schemes than by the tools' actual functionality. Managers fall for buzzwords and hyperbole, designers tell me. Yes, I know that's hard to believe.

The result? Designers end just to help sell the tool!" up with a tool that's more difficult to use than their old tool, or just clunky and not right for their designs, and they wonder what the hell happened.

A veteran designer summed it up for me during the Designers Forum at IPC APEX EXPO 2014. An EDA company rep was listing all of the new features of the latest rev of their layout software, and with every bullet point, the designer would whisper, "Who would ever need that? Or that? Who thought of this crap? That's useless! So is that! These features were added just to help sell the tool!"

Other designers wish they could just keep using their old version of the tool and not update. They've spent years using it, become amazingly productive with it, and their company updates to something they consider worse. One constant refrain I've heard, from users of every major layout tool, is, "Why do they keep changing the tool? It was fine the way it was... now there are more steps and it's less intuitive, and it's going to take a while to get really productive."

Which gets back to my original point: Who is your EDA tool company's customer: you or your executive management team?

This is nothing against the EDA tool companies, of course. Without them, you'd still be using Bishop Graphics tape and My-

> lar-well, some of you would probably like that. I have a lot of friends who work at EDA companies, and I wouldn't wish their workload on anyone. These companies are highly high-stress, petitive places to work. The public companies also have investors and Wall Street to contend with, and the Street has yet to show that it under-

> > stands EDA tools.

Their salespeople are constantly on the move, with many of their sales coming by way of converting their rivals' customers. It's a zerosum game, for the most part; there haven't been a lot of new electronics OEMs coming online lately.

And then the EDA companies have to deal with designers like you, who hold their feet to the fire, which you should. How would you like to be the support person you talk to when your layout tool quits working, which always seems to be on the drop-dead deadline?

I enjoy hearing all of your comments and complaints, whatever the topic. And maybe what I'm hearing are just anomalies, in the long run. Outliers.

What say you? Do you have any say in the layout tools you use? Let me know.

Talk to you next month! **PCBDESIGN** 



Andy Shaughnessy is managing editor of *The PCB Design* Magazine. He has been covering PCB design for 15 years. He can be reached by clicking here.



by Mike Creeden

SAN DIEGO PCB

When the subject of outsourcing PCB designs is mentioned, it tends to strike an image that can have 100 different views for 100 different designers. Outsourcing has been a part of the electronics development industry since the dawn of time. Therefore, no one can write or describe a view that covers every perspective.

My thoughts for this topic were to describe some of the common rationale for the majority of outsourcing. Perhaps you can find a perspective that relates to your viewpoint, or you may encounter a new perspective to consider this question: When does design outsourcing makes sense for an OEM? And what are some things you can do to better prepare for outsourcing to succeed at your company?

One of my favorite foods is sushi. When asked what I would like to eat, I may offer sushi as a suggestion. I have found a common response: "Well, I don't like sushi."

I reply, "Have you ever tried it?"

"Well no. I just know I don't like sushi." Other times, I hear, "I think I tried sushi once a long time ago, and it was no good."

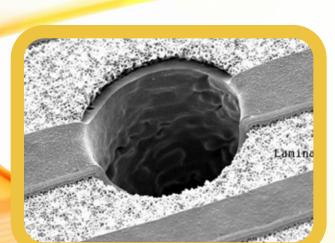
Many of us have a preconceived idea about a subject prior to examination, or based upon a limited past experience. I offer this analogy to invite the naysayer along for this discussion in hopes that I might provide a helpful option to a problem you are facing, or one you may be facing in the near future.

In every facet of development, there will always exist success stories and horror stories. We will look into some of the pros and cons of outsourcing to show that one size does not fit all and that today's issues may not be the issues we may face next year.

## When Should I Outsource?

The state of the electronics industry is a subjective topic. Some designers might say things are going well, but others would argue the

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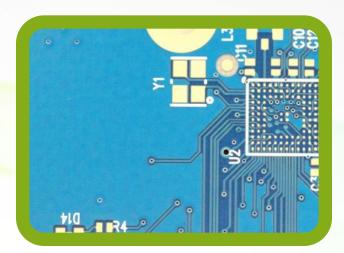
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## THE VIRTUAL CAD DEPARTMENT: THE CASE FOR OUTSOURCING DESIGNS continues



opposite. In good economic times and bad, OEMs still need to accomplish all tasks, complete the PCB design, and ship a product that is high quality, on schedule, and less expensive than the next company. This is the axiom that our competitive industry operates on: Better, less expensive, and we need it sooner!

If your internal staff of PCB designers has plenty of bandwidth and exceeds all of your needs, congratulations. I thank you for your time. But if you and your managers have concerns about meeting your current or future workload, please read on.

How does the need for outsourcing arise? Many different events can cause your firm to consider outsourcing as the solution or complement to your existing PCB design needs. I have listed a few below:

- Many startups have no PCB staff and an engineering development cycle that does not utilize a PCB designer full time. If they did have any designers, they might sit idle for significant periods throughout the year and become a financial burden.
- R&D often creates the need for outsourcing PCB designs. During this phase of prototype development, the need to innovate technology is always demanding in our time-sensitive market space.
- Many companies that have a PCB designer, or staff of designers, might encounter a project that is beyond the bandwidth of the staff.
- The technical requirements may exceed your staff's experience. Often the in-house designers may not be exposed to the latest indus-

try trends in design, software tools or manufacturing processes.

- Some projects have schedules that require multiple boards that must be completed at the same time.
- A particular project may require an accelerated schedule.
- Often there may have been a reduction in staff through retirement or designers relocating to other companies.
- Your engineering staff may wish to keep the work local so the EE can effectively oversee all of the progress.
- Your staff might be new to a software platform and lack proficiency.
- It's hard finding good help these days, especially PCB design talent. Designers are becoming scarcer, and many OEMs seemingly can't hire enough good designers.

Lastly, many companies have tried to hand off layout duties to their engineers, with varying degrees of success. Some software salesmen promise CAD managers that after purchasing their tools, the engineers can merely press the "easy button" and a PCB design will pop out the back. I say this in jest, but after you've purchased the software, the salesman may be long gone and the EE will need to master this tool as well as mastering PCB design.

With the complexities of today's software tools and the frequency of the layout cycle, the EE of today is seldom equipped to be proficient with the software tool, solve the circuit, and master the field of PCB design (you can learn to use a socket set but that does not make you an auto mechanic). Also, I would suggest that this may not be the best use of the engineer's skill set. We have seen many designs where the EE has raised the white flag and said, "Please take this and complete this design." This type of design is often more difficult to repair than starting from scratch.

## What Outsourcing is...and is Not

Outsourcing PCB design is not the same as outsourcing manufacturing. With manufacturing, your product definition is fixed and submitted to a proven manufacturing repeat process. But PCB design is not a commodity; it is **Good PCB designers** 

will serve at the direction

of your engineering staff

in a concurrent manner.

They are an Internet

connection away, whether

they are in the same

building, down the road,

across the country, or

around the globe. They

will incorporate your

initial design input, or

incorporate any changes

made along the way.

## THE VIRTUAL CAD DEPARTMENT: THE CASE FOR OUTSOURCING DESIGNS continues

a development science just like the other engineering disciplines.

When a procurement department sends out a design RFQ to multiple vendors/designers, and then awards the project to the lowest bidder, are they assuming that anyone can design it and will do so with a fixed completion date and receive a fixed price? Although this often occurs, you might ask, "Is the procurement person competent to assess PCB design talent and proficiency?"

In reality, all designers are not equal, just as you would not ask any random EE to perform your circuit engineering. Also, for time considerations, often the scope of the work is still in flux. Changes will occur, as we all know. This is known as scope/schedule creepage. Engineering is, by its very nature, a discovery science. Often during the CAD phase, responsible engineers would like to modify placement and routing to their hearts' content. These unseen and midstream changes, discoveries and modifications make estimating scope-of-work an unrealistic guessing game.

Many designers will answer the call of low-ball fixed price work and perform to a fixed date. When they do so, they are often pushed to ignore quality issues and engineering er-

rors that arise. Why would someone ever do that? Because they would be more than willing to design a second revision; after all, you made the errors and approved the poor quality. Thus, the expression "You get what you pay for." I have also heard someone say, "Price is what you pay up front and cost is what you will pay in the long run."

## What Outsourcing Should Be: A Virtual CAD Department

A virtual CAD department is an on-demand service that does not bill idle hours, but it does

incorporate innovation, experience, training, teamwork, and a good work ethic.

This should not be confused with the sweatshop mentality from days past. That negative concept of "work until you drop" burned people out and created more errors than was acceptable. Good PCB designers will serve at the direction of your engineering staff in a concurrent manner. They are an Internet connection away, whether they are in the same building, down the road, across the country, or around

the globe. They will incorporate your initial design input, or incorpo-

rate any changes made along the way. They are reliable, technically competent, and they will complete your design on time and with a cost that would be appropriate for the amount of engineering changes incurred. Thus, the expression that so many PCB designers know, "A customer will typically return to the last place they received a good layout."

Good PCB design outsource partners do not want just one PCB design; they wants your repeat business as a partner. What trait and attributes should a company look for in a design outsourcing partner? What expectations should companies have as they consider outsourcing?

Since companies come in so many different sizes, the scope of each project must be considered according to budget, technology and schedule. These questions and parameters could have many answers. There are many different solutions to outsourcing PCB design, and no one solution fits all.

Here are some common PCB design outsourcing solutions that may work for you:

• Many companies use only **employment agencies' temp staffers** because they can quickly relieve overburdened design staffs of the task of personnel searching. This may be a

## THE VIRTUAL CAD DEPARTMENT: THE CASE FOR OUTSOURCING DESIGNS continues

quick solution, but it might also result in subpar talent, perhaps someone not well-versed in complex PCB design. But good agencies do a better of finding good design talent.

- Contract labor that companies can find on their own may be successful, but these designers may be sitting at home unemployed. Often, these designers are unemployed for reasons that may make them a bad fit for your project. But if you manage to find a designer who meets your needs, this temporary solution can be a perfect fit.
- Many companies that seek the best deal or lowest rate will engage with what is termed a **moonlighter.** Many of us have been there and done that over the years, so I tread lightly here! These are designers who have a full-time position during the day, and at night or in their spare time they take on other projects. I could elaborate on all the possibilities with this scenario, but I will leave to your own imagination what might happen if push came to shove. This could be a great solution if, for technology reasons, you know any moonlighters who know your particular circuit or design, and they also have an easy schedule during their day job.
- Many firms will find a single designer who is referred to as a "garage shop" operation. This can be a really sweet situation for everyone concerned, because the designer is proficient enough to remain a self-employed sole proprietor. They may have a select collection of choice customers. But if they're really good, they run



the risk of becoming in demand, and a backlog may develop in their queue because they are one-man shows. Thus they may not be able to handle multiple boards simultaneously.

- One often-used solution is the **local ser**vice bureau. This is often a group of designers who successfully have built a following because they are good designers, but can they run a business? If they are utilizing contract help to further outsource your project, and offering a pay-as-you-go to these contractors, it can be a delicate situation. There may be little commitment from this contractor and you may not get consistent quality of work from this carousel approach. However, if the business has a stable group of designers to draw from, they can offer more consistent quality. There tends to be little teamwork or consistency from a collection of lone wolves. Another concern: Businesses that run on this methodology have been known to do the old bait-and-switch. You may deal with a local interface person for the project, but then they may ship the bulk of the work offshore to a true sweatshop. This could be a real concern for ITAR work and protection of your IP.
- Larger design centers have become more popular of late because they offer a more stable environment for their designers, providing secure, well-paid salaried employment, great benefits, and a pleasing work environment. These factors seem to attract and retain the best talent, thus the commercial expression, "Happy cows make happy cheese." With a larger design staff, these firms can provide a team approach that does not burn out the designer, and in the long run the customer has a greater chance of seeing his project completed with high quality, on schedule and in budget. A team approach also tends to facilitate a more consistent look and feel to multiple boards within a project. Often this larger design center will also provide a greater breadth of software platforms.
- Large engineering R&D firms will often sell the simplicity of a one-stop shop. However, care should be taken to ensure that they are not a business whose core competency is engineering with a token design presence.
- Contract manufacturers will, likewise, often sell the simplicity of a one-stop shop. OEMs should ensure these companies do not



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## THE VIRTUAL CAD DEPARTMENT: THE CASE FOR OUTSOURCING DESIGNS continues

have a core competency in assembly, with just a token design presence.

• Overseas service centers have the potential to entice many companies who are looking for a quick, cheap solution. This has been a good solution for some companies, but use caution. Some countries have an untrained labor pool using pirated software in nearly slave labor conditions. You run the risk of finding your IP or product cloned and then facing a much discounted competitor. In this situation, you may find yourself with little recourse. I have watched engineers laugh as the PCB design work went overseas, only to later find that his engineering work shortly followed.

## What it Takes to Succeed at Outsourcing

As you can see, one size does not fit all. In any of these situations, the best governing principle is to establish a business partnership in which you value each other's success. Remember, the PCB designer is an extension of your design team whether they are inside or outside of your four walls. Ideally, the work outsourced should be consistent with internal requirements. One of the key elements to understand is that the PCB design labor pool has been dwindling for quite some time. That does put the competent designer in a more strategic position. Designers might be worthy of some esteem as valued team member crucial to your success.

These views shared are the author's perspective and reflect his attempts at objectivity. I hope this helps you in your outsourcing efforts! **PCBDESIGN** 



Mike Creeden is the owner of San Diego PCB. He has been involved with the PCB design industry for many years as an application engineer, a PCB designer, and an IPC CID

Designer Instructor. He can be reached by clicking here.

## video interview

## **Mentor Fine-Tunes its Consulting Operations**

by Real Time with... **SMTAI** 



Jay Gorajia, director of consulting at Mentor Graphics, joins Editor Ray Rasmussen to discuss the creation of a consulting organization to help customers extract value from their existing assets. The organization's main goal is to help small- to medium sized companies—those who don't continually buy or expand capacity—make the best of what they already have.





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by J. Kelly Dack, CID+

A word to captive PCB designers regarding outsourcing PCB design:

You might be close to having an outsourcing experience if: You get to work and your design team's office floor is covered with lottery ticket stubs, and you overhear the purchasing gal mention she saw them all celebrating on the news the last night.

Resistance is futile! At some point, the company you work for is going to have too much PCB design work to fit through the product development, time-to-market pipeline. Management will begin to notice your bloodshot, worked-all-night eyes and see that you do not have enough bandwidth to do it all. They will not be able to justify hiring another captive designer. They will look into outsourcing.

PCB designers can be a bit possessive of design work. They view it as their livelihood, their raison d'être. Designing a successful PCB can lead to a rush of satisfaction. The thought of sending work out to be designed by another can

make one feel shaky or even feel a bit insecure. But the work belongs to your company, and the responsibility for meeting the schedule is a management call. Your job as a PCB designer is to support their decision and help in every way possible.

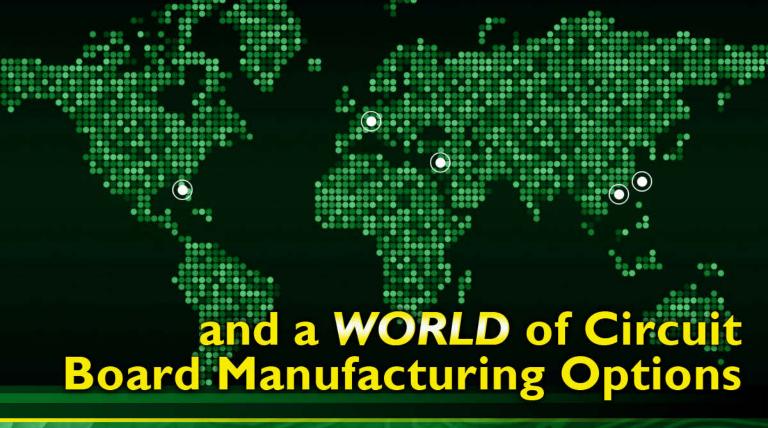
There is a way that you can help your company conquer the occasional design overload challenge. Your first instinct—working longer hours, chasing the "high" of one more night, one more design—is inefficient and unhealthy. But as a PCB design collaborator, you can obtain a different type of high by taking an active part in helping to develop and streamline an outsourcing process.

## **Help Find a Suitable Outside Design Source**

The PCB design community is amazingly well connected. Chances are you know several PCB designers who work at a design service bureau, or own their own design bureau. It's always a good time to make connections. Start with local PCB services in your area, and then take time to review some of the many design bureaus found online.

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### **ADDING VALUE TO YOUR DESIGN OUTSOURCING EXPERIENCE** continues

In the PCB design services world, there is a wide range of business models with key tradeoffs. Small, independent "freelance" layout services—typically run from a home office—have little overhead and can be more cost-effective. However, "independent" can often mean a single designer with limited bandwidth and limited design software capability.

A larger design company—often referred to as a design service bureau—joins together multiple designers who have unique design specialties and probably owns licensing for several design software tools to serve a larger customer base. Doing business with a design service bureau is much like doing business with a team. The price may be a bit higher due to the increased overhead, but the cost of getting your company's project done on time

company's project done on tim could be significantly lower, due to the company's greater PCB design resources and experience that can be directed toward the project.

And there are still larger a basis for expecting options available. For quite a a certain amount of few years now, the PCB industry has seen full-service EMS conformance from a companies move to providing PCB service company. design layout services. Some of these companies started as design service bureaus and have been so successful that they have been able to add parallel services such as engineering, component sourcing and purchasing, along with additional services like assembly, inspection and test.

The price of doing design business with a design and manufacturing operation like this could seem astronomical when compared to a small design service. But if your company is looking for more than just a layout service, perhaps delivery of a handful of working prototypes, or even a market-ready product, a full-service EMS company can make a lot of sense. A business partner like this will have full control of the manufacturing process and can orient the design layout more specifically to the manufacturing processes which they control. The design, engineering and manufacturing groups in these companies work closely together to

ensure success and own the quality of the final product.

## **Help Define the Outsourcing Process**

You are a successful PCB designer within your company. You've probably done so well that the EEs you work with are spoiled to the point of tossing you a schematic on a paper napkin after the morning meeting and expecting a finished layout by lunch, right?

Depending on which design service model suits your company's needs, your engineering group will need to understand what will be required to do business with an outside PCB design service. If this is a first-time outsourcing experience, some people in your department are

going to have to learn a new business paradigm: formalized communication!

If you haven't already, you can help by documenting your own process. Who does what? When? Where? How? What netlist format? What is your layout methodology? What are your naming conventions, design layer conventions, and output requirements? Most design service bureaus are more than happy to start with a design template that you prepare

for them. They appreciate the need for seamless consistency as design data moves from the customer, through the design service process and back to the customer.

With your own company design process documented, you have a basis for expecting a certain amount of conformance from a PCB service company. You have defined which PCB layout tools you use and have established your PCB documentation and archival requirements. It will make more sense to management as they move forward in the selection process to choose a design service company which is compatible with your established process. Hopefully, a good part of the decision will be based on your ability to adapt, change, copy and evolve the outsourced design revisions in the future when you have more time.

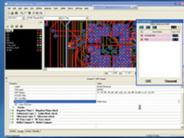
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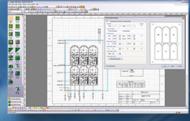


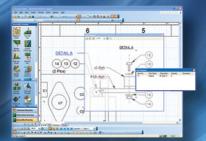




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working "down the

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**Communication can** 

be complicated by

vaque explanations,

misunderstanding

and even varying

time zones.

## ADDING VALUE TO YOUR DESIGN OUTSOURCING EXPERIENCE continues

## **Work With EEs to ID Design Constraints**

Design constraints shouldn't be taken for granted. EEs are accustomed to your special attention to layer stackup, high-speed signal treatments, current-carrying capacity and manufacturability. However, many of these features that you implement into design are taken for granted and hardly discussed

at all. Will an electronics engineer assume that all designers are like you?

Remember, an outsourced designer is not necessarily working "down the hall," so to speak. Communication can be complicated by vague explanations, misunderstanding and even varying time zones. Design constraints need to be formally listed, if not embedded into front-end design tools and templates to clarify what is expected.

## **Define a Set of Deliverables**

Whether ordering a simple layout or a complete design prototype, your company, especially your procurement folks, will benefit from formulating a concise description of what you require from the service provider.

A list of important "deliverables" is best defined and added to the purchase order for the work being done. Obvious deliverables might be a design layout or finished PCB. But all too often, once a layout or PCB is delivered into the hands of an EE, documentation and archival of important data required to reproduce the design becomes forgotten and somehow unaccounted for. This misstep can cause a catastrophic waste of time if the PCB design ever requires a future change and the service provider has gone out of business.

Look at your own design process requirements. Make sure that every file and document required to reproduce, document or otherwise work on the design is provided by the design service as a deliverable and is archived via your department process immediately upon delivery.

## **Keep the Wheels Greased**

It can take a convergence of many factors to establish a successful working relationship with a PCB design service partner. These include time, prototyping budget, contact development, communication, maybe some false starts and maybe some trust-building. Once you've estab-

lished a successful working relation-

ship with an outside PCB design services supplier, it is important to stay in synch. Unless your company periodically practices the process that you've helped them to establish, your efforts could fall by the wayside before the next design overload crisis due to changes in technology, practice or personnel.

Pick a project every so often and send it out. Cause your EEs and your purchasing agents to stay connected with your company's design outsourcing resource and process. Yes, the price seems high when it isn't required. But avoid criticism and comparisons of the price paid for

work done through an outside design service. Comparisons to the "cost for you to have done it" are irrelevant in times of design overload. Funding an occasional outsourced design project can be budget well spent to ensure that your company's outside design source stays in lock-step with your process and engineering culture until you need them again.

There is a saying in the PCB design industry: "Given enough time and layers, we can do anything." While layers come at a price, time stands still for no PCB designer. Be ready to partner with an outside design service that can work with you. You might be helping your company buy back time. **PCBDESIGN** 



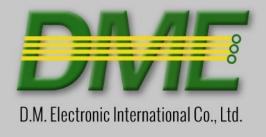
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## **PCB007 News Highlights**



## **PCB Industry Slowdown Continues** in August

"August business results for the North American PCB industry continued slightly below last year's levels," said Sharon Starr, IPC's director of market research, "but the PCB book-to-bill ratio continued hovering near parity and actually strengthened a bit in August. Flat growth is still expected for the remainder of 2014."

## **Colonial Assumes Vermont Circuits' Customer Base**

Mark Osborn, president and founder of Colonial Circuits, announced recently that his company has acquired Vermont Circuits' customer base and will be offering a smooth transition for those former customers.

## **Wurth Elektronik's Flex PCBs Achieve UL Mark**

After a time-intensive and close coordination with the UL engineers, an enormous amount of test patterns and high costs, Würth Elektronik was able to record a big achievement: Four flex-rigid PCBs received the UL Listing.

## **Viasystems Challenges EPA's CDR Cycle**

Congressman Bill Johnson (R-OH) sent a letter to U.S. Environmental Protection Agency (EPA) Administrator Gina McCarthy requesting an analysis of reporting data pertaining to by-products sent for recycling collected during the 2012 Chemical Data Reporting (CDR) reporting cycle.

## **IPC: PCB Market Down 2.2%**; **Production Value at \$59.4B**

The world market for PCBs declined an estimated 2.2% in real terms in 2013, although real growth in North America was positive at 0.8%, according to IPC's "World PCB Production Report for the Year 2013."

## **Q3 PCB/EMS Market Snapshot**

I-Connect007's latest market survey—a one-minute survey designed to provide a snapshot of the current state of the PCB and EMS industries—offers a good sampling to give us a snapshot of where we've been and where we're headed.

## FTG's Circuits Segment Sales Up \$1.9M in Q3

"FTG's momentum has continued in Q3 2014 with strong results across the corporation, particularly at our Circuits business and the two new Aerospace facilities in Tianjin and Chatsworth where we continued to see progress on qualification activities, strong orders, and increased shipments," stated Brad Bourne, president and CEO.

## **IPC Report Shows Moderate Growth** Through 2017

Among PCB product types, HDI/microvia boards experienced the highest growth rate in 2013. Data on vertical markets for PCBs show that communications and military/aerospace are the two largest PCB markets in North America, together accounting for approximately 57% of the North American PCB market in 2013.

## **Germany Records Highest PCB Sales Since 2011**

The automotive electronics sector drove Germany's PCB market in July, helping the industry record its highest sales since 2011, according to ZVEI.

## **Aspocomp Consolidates Operation: May Close Teuva Plant**

As part of Aspocomp's strategic transformation, the company has issued a notice on statutory labor co-determination concerning all its personnel at the Teuva plant regarding the consolidation of production in Finland and the possible closing of the Teuva plant.

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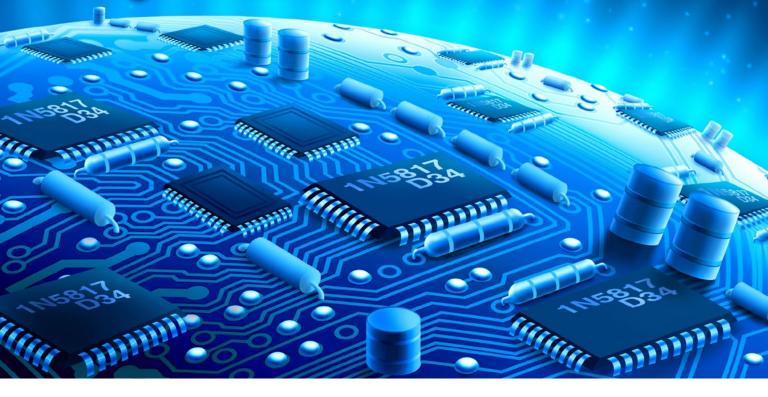
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## Component Selection for Easier Design and Manufacture of Electronics



## **by Joe Fjelstad**VERDANT ELECTRONICS

"Simplify, simplify, simplify."
—Henry David Thoreau

Thoreau penned his simple lifestyle mantra more than 150 years ago and it still as valid today as it was when he first captured and recorded his thoughts on paper. He was not the first to extoll the importance of simplicity, but he said it in a memorable way.

Achieving simplicity has been deemed a worthy objective by many philosophers over centuries, and people often profess to seek simplicity in their lives. In the world of high tech, simplicity is arguably one of the foundational objectives of most of the technologies that surround us today. Certainly this is true in terms of how product designers are trying to create

interfaces that allow even the most nontechnical users to get what they need from electronic products with a minimum of hassle.

However, that interface simplicity is undergirded by a massively complex electromechanical substructure of circuits, sensors and components. Pop open any high-end electronic device and you will be met by an impressive mass of densely packed components and circuits. Presently, those components are available in a wide array of formats, with a number of different lead shapes and forms along with the device's mechanical outline. Presently, there are J-leads, I-leads, gull-wing leads, posts, balls and no leads at all. Mechanical outlines are generally square and rectangular, but the bodies can have a wide range of dimensions in X, Y and Z. While area array technology has helped to make things smaller, it has also upped the complexity factor from a design perspective by mixing grids and land shapes and sizes.



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Why so many options? It is because there is not, nor has there ever been, a truly coherent approach to the process of selecting package structures for ICs or any other components for that matter. Yes, a roadmap for electronic component lead pitch was introduced with the advent of SMT, and that roadmap said that every next-generation lead pitch should be 80% of the size of the previous generation lead pitch.

The number 80% was arbitrary, but it was held to religiously, even when later it became clear that it made no sense, as will be shown. The original proposal was created for peripherally leaded components, for which some sort of planned progression was arguably needed. However, when area array technology became dominant, the rule became an impediment to real opportunity. A simple common grid based on a fundamental pitch was all that was needed. The electronics industry had precedent when the 0.100" grid was the base for all circuit design and assembly.

## The Nexus of Order and Simplicity

If the industry is to find The leads will be plated its way back to its roots and simpler times, there is a need for only one base grid pitch to which all components should adhere. The base pitch which seems most practical is 0.5 mm because below that pitch soldering gets more difficult and solder-based defects climb. While area array lead format, in the form of land grid array devices, is deemed most appropriate for all components, QFN devices can work provided that all of the terminations follow the base grid rule. Few leaded components such as discrete resistors, capacitors and transistor can easily be provided with leads which conformed to the 0.5 mm pitch.

One advantage of using these bottom terminated component formats is that they offer the greatest uniformity in terms of component lead planarity. While soldering may be employed to

affix them if one eschews the use of solder and opts to build circuits on top of the components in the manner of Occam/SAFE technology, it also allows the component supplier to bypass the use of solder or a solderable finish: The leads will be plated to directly, using copper and HDI processes as if the leads were internal lands. Eliminating the finish gives rise to the potential to reduce component cost and increase yield because the devices require fewer process steps. As any process or manufacturing engineer will tell you, where there are more process steps to control, the greater the potential for things to go wrong. And they always, it seems, eventually go wrong.

In order to achieve this order and simplicity, one must first actually believe it is desirable and be willing to make the appropriate changes. In the present case the electronic assembly designer must actively weed through, seek out and use components which not only conform to a common base pitch but also most desirably, conform to a common height.

> The Joint Electronic Device Engineering Council (JEDEC) registers the mechanical outlines of all of the various components which component suppliers wish to supply to users. There are literally thousands of possible component body options if all permutations are accounted for. JEDEC council members have given letter designations that define component heights with desirably low profiles based on established protocol and accepted terminology. These are presently divided into nine different ranges. "Low" component heights begin at 1.7 mm

and extend down to 0.025 mm at the lowest end.

Figure 1 illustrates the differences not only between ranges but within individual ranges. Note that in the graphic, the components are all shown with solder ball terminations. The reason for this is that most components used today have such solder ball terminations. One

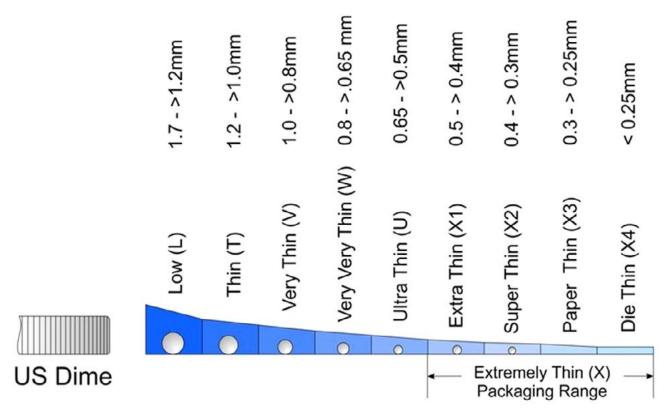


Figure 1: A comparison on JEDEC defined mechanical heights for electronic components. The wide range of thickness is due to a combination of legacy mentality which was not as concerned with height and the fact that solder termination height can vary significantly within and between parts. Note also that roughly half of the height of a component is due to the solder used for interconnection. A component designed for SAFE products can, in many cases, be either a U or X designation because of the elimination of solder.

of the big reasons for the significant variation in component height within each class is that it is a significant challenge to make all of the solder balls sit in a common plane and there is thus an allowance for such non-uniformity within and between such components.

## Why Use a Package at All?

One might be tempted to leap ahead at this point and question the need for a package. There has been, for example, an increasing flow of papers and articles about embedding ICs into modules and PCBs. IPC and IEC have developed or are developing standards for embedded device design and assembly, but they are proving rather confusing because both documents try to include every imaginable variation, some of which are not particularly practical. However,

the underlying issue with using bare die in an electronic assembly is multifaceted and the designer must understand why they should be avoided.

To begin, bare die are difficult to handle and place. They are delicate and can be easily damaged both physically and electrically by ESD. Second, it is very difficult to assure die quality and reliability because burn in of discrete die (or even in wafer form) is difficult and even when done, it is expensive. Moreover, most chip foundries do not like shipping bare die because of these concerns and others related to business as yield can be determined. A third reason why bare die are not a good choice is that they have no standards. Every IC chip is unique and rarely are chips provided with a pad layout that has any kind of standard grid pitch. (There are a few

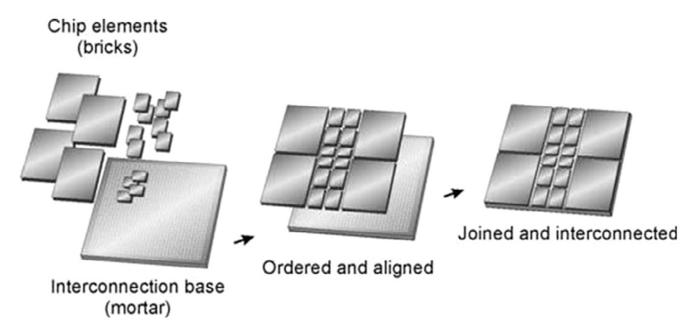


Figure 2: A "disintegrated" circuit comprised of "brick and mortar," in the words of the developers, is essentially a 2.5D interconnection solution which offers unique potential to create ASIC-level performance in a rapid manner by interconnecting functional circuit blocks on an interconnection base which can then be packaged for use at the next level, as suggested by researchers at the University of Washington and the University of Michigan.

exceptions for some high-end processor chips and FPGAs with hundreds to thousands of I/O.)

In addition to these fundamental challenges, when die shrink is carried out with nextgeneration die (most often to improve silicon use efficiency), the pad locations nearly always change. Thus any time there is a die shrink, a redesign of the substrate to which it is attached must be done (except in the case of most wire bonded chips). In contrast, the use of fully tested and burned in components with established termination locations and lead pitch, allows the fundamental component pad out and and PCB design made with it to be reused even if die shrink has occurred. This is not an insignificant point for consideration.

One last point that deceives some in terms of finding our way to a simpler future requires an appreciation of the potential to, at some point in the years ahead, design circuits using basic functional IP blocks rather than purchasing a die of multiple IP blocks integrated into a single chip, which is representative of a significant number of IC chips. This has been suggested by researchers at the University of Washington and the University of Michigan. In the current paradigm, both the designer and the manufacture must provide for every termination of the die, whether the terminations are of use in the final design or not. That means that there is a multiplication of opportunity for defects when there could eventually be a reduction.

The potential benefits are far-reaching, in that designers could build a new product with only the specific functions they want in their design. The design using functional block only would be smaller and better performing. It would also be cheaper and more reliable, potentially much more reliable. One reason for reliability increase is that the IC could possibly be built with an earlier node of IC technology which is intrinsically more reliable due to longer diffusion paths on the chip. An added benefit is that it can be done at higher yield. Figure 2 illustrates this concept.

This solution is relatively simple and the benefits are many, but the challenge will be to get the industry to rethink its approach to in-



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creasing integration on the chip. Moreover, if the elements were manufactured as standardized packages devices with a common base footprint (as hinted at in the graphic), the doors open to the manufacture of minimalist solutions that provide targeted benefits to both the product developer and their customers.

These simple concepts may seem a bit radical given the current state of electronics manufacturing, especially the elimination of solder from the electronics manufacturing process. Some have even characterized the very idea of solderless assembly as utterly unreasonable. Such a stance actually provides some hope for the future, for as Irish playwright and philosopher George Bernard Shaw once observed, "The reasonable man adapts himself to the world; the unreasonable one persists in trying to adapt the world to himself. Therefore, all progress depends on the unreasonable man."

Luckily for the planet, there are increasing numbers of "unreasonable" individuals around the globe because change cannot happen without them. Some are even beginning to rally around the idea decreasing manufacturing complexity by reconsidering design and embracing the common grid concept. When coupled with the prospect of simplifying the manufacturing process through the elimination of solder and the prospect of reduced cost and increased product reliability, it seems that making such a choice should be, at the end of the day, a simple one. PCBDESIGN



Verdant Electronics Founder and President Joseph (Joe) Fjelstad is a four-decade veteran of the electronics industry and an international authority and innovator in the field of electronic

interconnection and packaging technologies. Fielstad has more than 250 U.S. and international patents issued or pending and is the author of Flexible Circuit Technology.

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## Vertical Resonances in **Ceramic Capacitors**

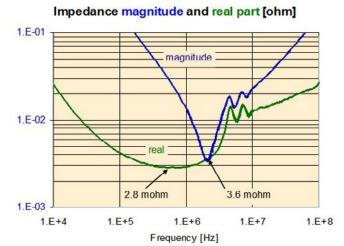
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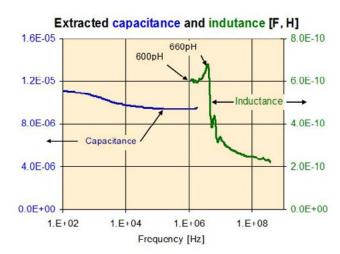
Ceramic capacitors are very popular in power distribution networks (PDN). They are small, cheap and come in a very wide range of available values. Typical ceramic capacitors also have low losses, at least compared to similar-valued electrolytic or tantalum capacitors. Because of their small size, we might think that structural resonances inside the ceramic capacitors do not exist in the frequency range where we usually care for the PDN. The unexpected fact is that the better PDN we try to make, the higher the chances that structural resonances inside ceramic capacitors do show up. This column tells you why and how.

Figure 1 shows measured data [1] on a small 0508 reverse-geometry 10uF capacitor. There are several interesting aspects of these plots that are explained in the paper found in [1]. Here, we focus only on one strange-looking detail: the

double-hump resonance we see on the impedance magnitude and impedance real part curves somewhere in the 3 to 10 MHz frequency range. The test setup made sure that as much as possible the measurement result represented only the capacitor: The little fixture used for the measurement was separately characterized and showed no resonance in that frequency range.

The biggest linear dimension of this capacitor is 80 mils, or 2 mm. The wavelength of 10MHz in free space is 30 meters; this is so much bigger than the linear dimensions of the capacitor that any resonance at such low frequency is really surprising, even if we factor in the high dielectric constant of the ceramic material. To understand what happens, we have to create a detailed electrical model of the capacitor, for instance a two-dimensional bedspring matrix, shown in Figure 2.



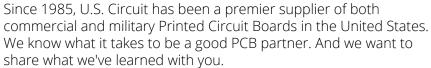


Measured impedance magnitude of a 10uF 0508 MLCC with the real part of the impedance (on the left), and extracted capacitance and inductance versus frequency (on the right).

Figure 1: Measured data from [1].

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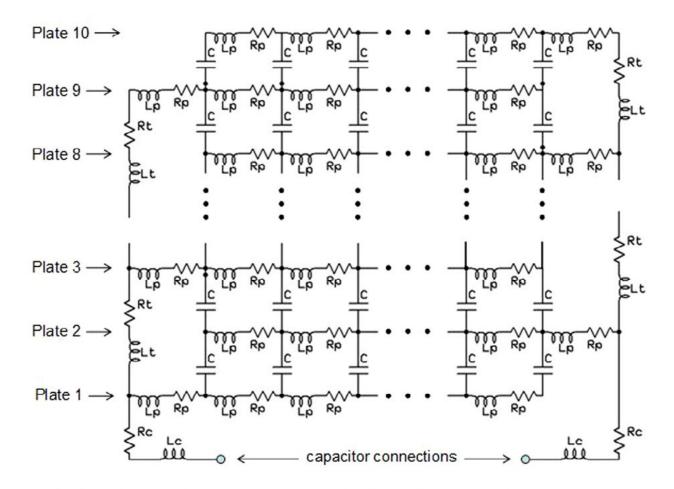
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## VERTICAL RESONANCES IN CERAMIC CAPACITORS continues



Partial schematics of the bedspring capacitor model. The model consists of ten capacitor plates, 1 through 10. The lowest capacitor plate, connecting to the PCB, is Plate 1. Plates 1, 3, 5, 7 and 9 are connected to the left terminal. Plates 2, 4, 6, 8 and 10 are connected to the right terminal. Each capacitor plate is divided into ten equal segments (plus an end piece), represented by series RL networks. At each internal plate node, a capacitor represents the dielectrics.

Figure 2: Bedspring model from [1].

Ceramic capacitors we use for power distribution bypassing have multiple metal plates interdigitated and embedded in a high dielectric constant ceramic material. As shown in Figure 3, the capacitor plates connect alternating to vertical metalized terminals at the two ends of the capacitor body. High-density ceramic capacitors can have hundreds of these capacitors plates. Between adjacent capacitor plates, which are connected to the opposite terminals, there are thin ceramic layers. Many of these sections are connected in parallel by the vertical terminals,

conveniently increasing the total capacitance and reducing the inductance as well as the series resistance of the part. Without cross sectioning we don't know how many conductive plates a particular capacitor actually has, but to model the resonances we see in the measured data, it is really irrelevant. The model in Figure 2 uses a 10x10 matrix: 10 capacitor plates on each terminal and 10 dielectric segments along the plates. L<sub>c</sub> and R<sub>c</sub> represent connection inductance and resistance between the capacitor's terminals and the observation point: these are

#### **VERTICAL RESONANCES IN CERAMIC CAPACITORS** continues

the parasitics of the connecting vias and traces. The model, though it looks complicated, runs very fast in any SPICE tool in AC simulations. Note that since here we are interested in the capacitor's behavior above the series resonance frequency, dielectric losses are not included in the description.

For an illustrating case that creates a series resonance frequency at 10MHz, the simulated impedance results are available in a spreadsheet [2]. The spreadsheet contains the AC sweep SPICE results at 200 frequency points, logarithmically spaced from 1 MHz to 100 MHz, one decade below and above the series resonance. On two 3D charts you can see the current distribution inside the dielectric and in the capacitor plates. On both 3D plots the vertical axis shows current in amperes on a logarithmic scale, the

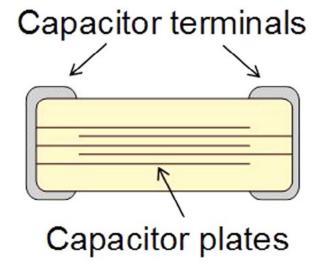


Figure 3: Internal construction of a multi-layer ceramic capacitor.

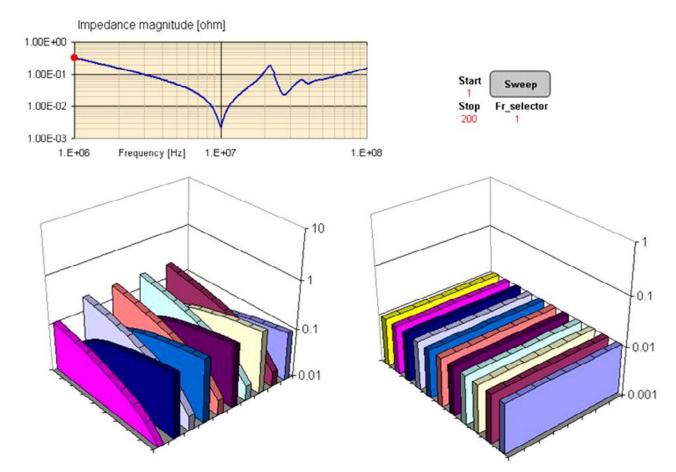


Figure 4: Impedance magnitude on the top left chart. The current distribution is shown at 1 MHz in the capacitor plates (lower left 3D chart) and in the dielectrics (lower right 3D chart).

#### **VERTICAL RESONANCES IN CERAMIC CAPACITORS** continues

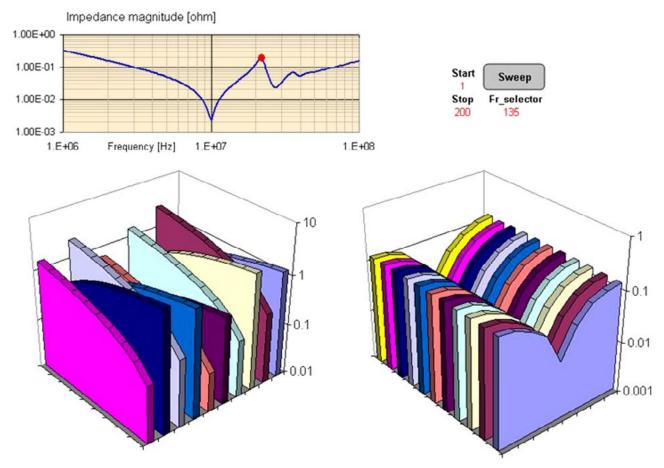


Figure 5: Impedance magnitude on the top left chart. The current distribution is shown at 22 MHz in the capacitor plates (lower left 3D chart) and in the dielectrics (lower right 3D chart).

right axis corresponds to vertical location inside the capacitor with the front center corresponding to the bottom of the capacitor, closest to the PCB it is mounted on. The left horizontal axis corresponds to the left-to-right position inside the capacitor body between the two vertical terminals. With a macro you can sweep through the frequency values or you can plug in a specific frequency selector number.

The current distribution one decade below the series resonance frequency is uniform. This directly shows up in the dielectric current plot being a flat surface. The capacitor plate current shapes look triangular. Since the capacitor plates don't short the opposite terminals, they end in the open dielectric, hence the triangular shape. The equal-height triangular shape in fact corresponds to uniform current sharing among the plates.

When we set the frequency selector to the 135<sup>th</sup> point, which corresponds to 22 MHz, the current distribution plots change significantly. In general, the values in both 3D charts are much higher, already suggesting a resonating scenario. The resonance clearly shows up on the right-hand 3D plot (dielectric current), exhibiting a notch halfway up inside the capacitor body. This comes from a vertical half-wave resonance, also shown as a local peak at 22 MHz on the top left impedance magnitude plot.

If we re-simulate the model with different L<sub>c</sub> values, we will see that the structural resonance gets stronger as the ratio of inductances of the vertical terminal versus the external connection increase. With poor connection, when the connection inductance is much higher than the inductance of the capacitor terminals, this resonance is hardly noticeable. Strangely, as

#### **VERTICAL RESONANCES IN CERAMIC CAPACITORS** continues

we improve the connection of the capacitor by driving  $L_c$  down, we also make these structural resonances more pronounced.

As we demonstrated, in spite of their physically small sizes, ceramic capacitors can exhibit structural resonances, too. If you want to read more on the subject, check out the cited references. **PCRDESIGN** 

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- 1. "A Black-Box Frequency Dependent Model of Capacitors for Frequency Domain Simulations," DesignCon 2005 East, High-Performance System Design Conference, Worcester, MA, September 19–22, 2005, available here.
  - 2. Grid sweep projected view, <u>available here</u>.

3. "Slow Wave Causal Model for Multi Layer Ceramic Capacitors," DesignCon 2006, Santa Clara, CA, February 6-9, 2006, available here.



Dr. Istvan Novak is a distinguished engineer at Oracle, working on signal and power integrity designs of mid-range servers and new technology developments. With 25 patents to

his name, Novak is co-author of "Frequency-Domain Characterization of Power Distribution Networks." To read past columns, or to contact Novak, click here.

# 3D Printing Incorporates Quasicrystals

Automotive, aerospace, and machinery industries, among others, are resorting more and more to the use of 3D printing methods to produce manufacturing components. There is a strong demand that the technologies involved in this process produce parts with stronger functional properties. This requires the development of new adaptable materials.

Researchers at the University of Lorraine in France say that quasicrystals, a type of complex metal alloy with crystal-like properties, can be useful in the design of new composite materials for this purpose.

In a review published by Science and Technology of Advanced Materials, Samuel Kenzari and co-authors summarized recent developments related to the use of complex metal alloys in additive manufacturing.

Additive manufacturing, commonly thought of as 3D printing, is a process that involves the manufacture of components from a digital model. In additive manufactur-

ing, lasers are employed to build layers based on a digital model, ultimately resulting in the final component.

Additive manufacturing methods are becoming widespread and affect many industries. In 2012, they generated global revenues of \$2.2 billion. But the range of materials used is still restricted despite a real demand for manufacturing lighter parts with better functional properties.

Incorporating complex metal alloys (CMAs), such as quasicrystals, in the design of new composite materials can help meet this demand.

Complex metal alloys are promising because of their potentially useful properties such as low friction, relatively good corrosion resistance, and good resistance to wear. They are also, however,

intrinsically brittle, preventing their use as bulk materials. Scientists, reports the University of Lorraine team of researchers, have found alternatives to circumvent this problem. One is to use CMAs as reinforcement particles. The other is to use them as a coating material.

The researchers are currently working on the development of functional parts made using CMAs that have health applications.





# Signal Integrity, Part 2

# by Barry Olney

IN-CIRCUIT DESIGN PTY LTD

In <u>Part 1</u> of my signal integrity series, I examined how advanced IC fabrication techniques have created havoc with signal quality and radiated emissions. This month's column will cover the effects of crosstalk, timing and skew on signal quality.

#### Crosstalk

Crosstalk is the unintentional electromagnetic coupling between traces on a PCB. But crosstalk can also be induced in the return path, which often gets overlooked. Figure 1 shows the crosstalk associated with two parallel trace segments on the outer (microstrip) layer of a PCB.

The red lines represent the magnetic field that couples voltage inductively to the nearby trace and also radiates electromagnetic emissions. The blue lines are electric fields that capacitively couple current into the nearby trace and are somewhat absorbed by the plane but still tend to radiate noise outward.

Crosstalk can be coupled trace-to-trace, on the same layer, or can be broadside coupled by traces on adjacent layers. The coupling is threedimensional. Broadside coupling is difficult to spot, because generally we look for trace clearances on the same layer when evaluating crosstalk, but a simulator will pick this up. Traces routed in parallel and broadside cause greater amounts of crosstalk than those routed side by

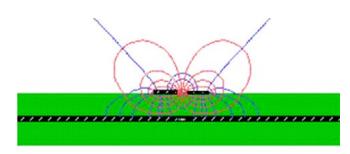
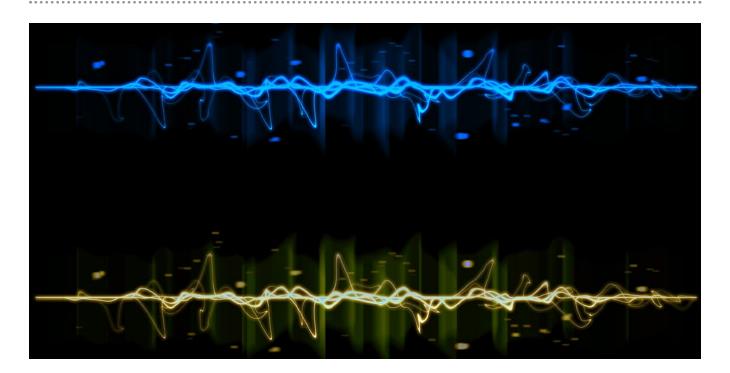


Figure 1: Crosstalk on the outer (microstrip) layer.



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side. This is due to the width of the trace being much larger than the thickness, so more coupling occurs in the broadside configuration. It is therefore good practice to route adjacent signal layers, in the stackup, orthogonally to each other to minimize the coupling region. A better solution is to only have one signal layer between two planes to totally avoid broadside coupling altogether.

Also, these days many stackups use a buildup microstrip layer on the top and bottom of the board. This can be very dangerous as one must take particular care of traces routed on the adjacent layers.

Since crosstalk is induced by one or more aggressors onto a victim trace, it is obvious that the higher the aggressor voltage, the more crosstalk will be induced. It is therefore best to segregate groups of nets according to their signal amplitude. This strategy prevents larger voltage nets (3.3V) from affecting smaller voltage nets (1.5V).

Crosstalk is defined by:

$$Xtalk = \frac{1}{1 + (\frac{D}{H})^2}$$
 Equation 1

The above equation clearly shows that in order to reduce crosstalk, we need to minimize H (height above the plane) and maximize D (distance between traces). The easiest way to reduce crosstalk, from a nearby aggressor signal, is of course by increasing the spacing between the signals in question. Crosstalk falls off very rapidly with distance. Crosstalk plummets roughly quadratically with increased separation. Doubling the spacing cuts the crosstalk to roughly a quarter of its original level.

**Rule of Thumb:** Gap =  $3 \times \text{trace}$  width.

However, in today's complex, dense designs, it is not always possible to use up valuable real estate to satisfy the above. An alternative is to set up parallel segment rules to prevent traces running in parallel for more than 500 mils. Also, the effect of dielectric height above a reference plane on trace-to-trace coupling plays an important role in reducing the crosstalk. A 3 mil thick dielectric material reduces the crosstalk by approximately a quarter, compared to the 6 mil, given the same trace spacing.

**Rule of Thumb:** Couple the signal traces closely to the plane.

Crosstalk is typically picked up on long parallel trace segments. These can be on the same layer as in Figure 3, but may also be broadside coupled from the adjacent layer. It is for this reason that orthogonal routing is recommended on adjacent layers (between planes) to minimize the coupling area. This will not occur with the stackup illustrated in Figure 3 of last month's column, because there is only one signal layer between the planes. So this is very safe as far as broadside crosstalk is concerned.

# **Timing and Skew**

Flight time delay and skew are key pillars in high-speed PCB design signal integrity. One of the driving factors for flight time and skew performance is the placement of components. Maximum placement refers to the placement in which the distances between the devices are the maximum distance permitted. Controlling the maximum placement of devices, combined with the assumption that good general design practices are adhered to, limits maximum trace

JNITS	: mil	l.				Differen	ntial Pairs >	8/21/20 50/100 oh	The second second					Tota	Board Thickness: 6	9.4 mil
ayer No.			n & meter	Description	Layer Name	Material Type		Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
				Soldermask		Dielectric	3.3	0.7								
6	8	4	8	Signal	Тор	Conductive			2.2	10	5.5	0.55	70.13	121.81		Surface Traces & Pad
				Prepreg		Dielectric	3.7	3.4								
2				Signal	Inner 2	Conductive			0.6	10	4.5	0.18	53.5	99.23		Buried Microstrip
				Core		Dielectric	3.6	3								
2	11			Plane	GND	Conductive			0.6							

Figure 2: Layers 1 and 2 have only 3.4 mils separation and are prone to coupling.

delay to roughly the longest Manhattan distance of the signals contained in a specific clock domain.

Why the longest Manhattan distance? This is due to skew matching requirements: All of the shorter nets in a clock domain must be lengthened to skew match to the longest run length. Therefore, flight time and skew—for an entire clock domain—are governed by the maximum placement, along with the routing rules that constrain the matching of the trace lengths.

In the classic high-speed design flow, timing specifications simulation results are compared to determine placement and routing constraints. Given a length constraint, a designer can control signal integrity by controlling the PCB trace topology of the various parts of an interface. Included in this topology are any terminations.

Figure 4 illustrates the timing of the clock compared to the address, control and com-

mand signals of a DDR3 memory design. Also, the skew between data lanes and data strobes should be kept to a minimum and the eyes should be wide open. DDR3 is much easier to route, in fact, than DDR2 as leveling can be used to synchronize the delay of data lanes.

There are many other factors that can influence signal integrity, but basically the stackup planning and the PDN analysis of a PCB are the two main factors that control the stability of a design. Getting these two factors right helps ensure the long-term reliability and performance of any high-speed digital design.

We all know that simulation tools aren't cheap, and there is a learning curve associated with complex software, not to mention that the engineer needs to have years of experience analyzing high-speed designs. By utilizing a board-level simulation service, you can be assured that your PCB will be reliable, manufacturable, will conform to specifications and will pass the rel-

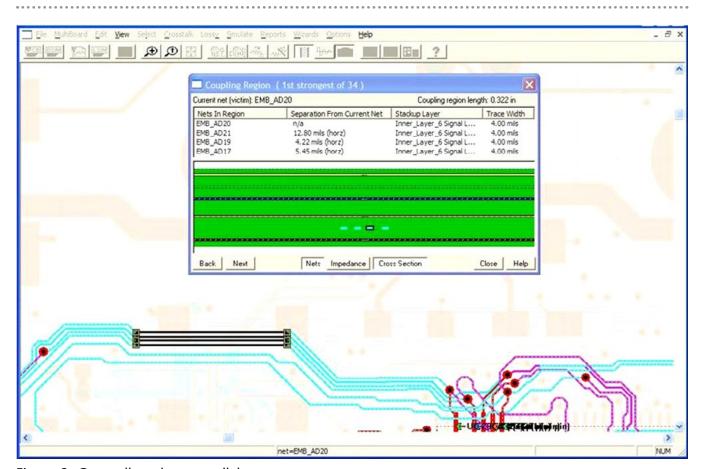


Figure 3: Crosstalk on long parallel trace segments.

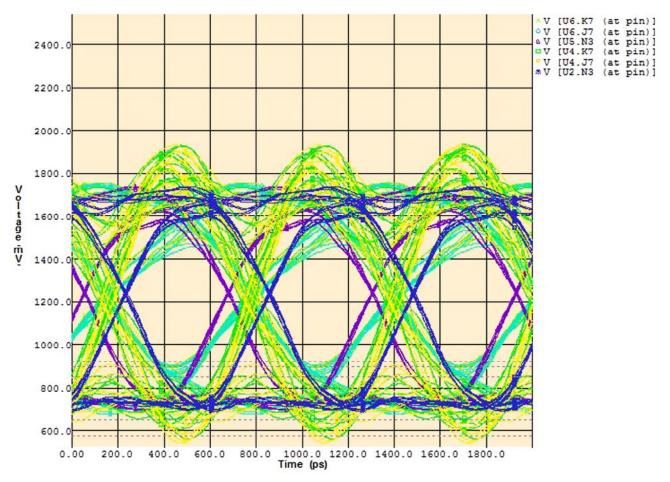


Figure 4: Skew of clock to address, control and command signals of DDR3 memory.

evant compliancy tests, saving you time, money and frustration for a fraction of the cost of board iterations and multiple compliancy testing. Plus, the simulation can be done before the design is finalized (before Gerber output or even earlier in the design process) to further reduce production time and costs.

#### **Points to Remember**

- Crosstalk is the unintentional electromagnetic coupling between traces on a PCB. But crosstalk can also be induced in the return path—which often gets overlooked.
- Crosstalk can be coupled trace-to-trace, on the same layer, or can be broadside coupled by traces on adjacent layers. The coupling is threedimensional.
- The higher the aggressor voltage, the more crosstalk will be induced. It is therefore best to

segregate groups of nets according to their signal amplitude.

- The easiest way to reduce crosstalk, from a nearby aggressor signal, is by increasing the spacing between the signals.
- Reducing the dielectric height will also dramatically reduce crosstalk without impacting on real estate.
- Flight time delay and skew are key pillars in high-speed PCB design signal integrity. One of the driving factors for flight time and skew performance is the placement of components.
- Flight time and skew—for an entire clock domain—are governed by the maximum placement, along with the routing rules that constrain the matching of the trace lengths.
- Given a length constraint, a designer can control signal integrity by controlling the PCB trace topology of the various parts of an inter-



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face. Included in this topology are any terminations.

• Stackup planning and the PDN analysis of a PCB are the two main factors that control the stability of a design.

In Part 3 next month, I will continue to discuss signal integrity, in particular where most designers go wrong with signal integrity and how to avoid the common pit-falls. PCBDESIGN

#### References

1. Barry Olney: Beyond Design: Practical Signal Integrity, Beyond Design: Pre-Layout Simulation, Intro to Board-Level Simulation and the PCB Design Process, Beyond Design: Impedance Matching: Terminations

- 2. Howard Johnson: High-Speed Signal **Propagation**
- 3. Henry Ott: Electromagnetic Compatibility Engineering
- 4. The ICD Stackup and PDN Planner are distributed globally by www.altium.com



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Plan-

ner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.

# **Tiny Carbon Nanotube Pores Make Big Impact**

A team led by the Lawrence Livermore scientists has created a new kind of ion channel based on short carbon nanotubes, which can be inserted into synthetic bilayers and live cell membranes to form tiny pores that transport water, protons, small ions, and DNA.

These carbon nanotube "porins" have significant implications for future health care and bioengineering applications. Nanotube porins eventually could be used to deliver drugs to the body, serve as a foundation of novel biosensors and DNA sequencing applications, and be used as components of synthetic cells.

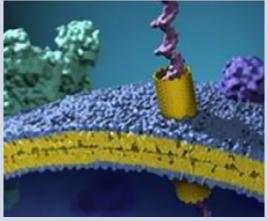
"Many good and efficient drugs that treat diseases of one organ are quite toxic to another," said Aleksandr Noy, an LLNL biophysicist who led the study and is the senior author on the paper appearing in Nature. "This is why delivery to a particular part of the body and only releasing it there is much better."

The Lawrence Livermore team, together with colleagues at the Molecular Foundry at the Lawrence Berkeley National Laboratory, University of California Merced and Berkeley campuses, and University of Basque Country in Spain created a new type of a much more efficient, biocompatible membrane pore channel out of a carbon nanotube (CNT)--a straw-like molecule that consists of a rolled up graphene sheet.

"Taken together, our findings establish CNT porins as a promising prototype of a synthetic membrane channel with inherent robustness toward biological and chemical challenges and exceptional biocompatibility that should prove valuable for bionanofluidic and cellular interface applications," said Jia Geng, a postdoc

who is the first co-author of the paper.

Kyunghoon Kim, postdoc and another coauthor, added: "We also expect that our CNT porins could be modified with synthetic 'gates' to dramatically alter their selectivity, opening up exciting possibilities for their use in synthetic cells, drug delivery and biosensing."



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# Mil/Aero007 **News Highlights**



# **Ventec Supports ESA Proposal for IPC4101D's Appendix A**

The proposed Appendix A, originally drafted in February 2013 and revised in September 2014, aims to define an enhanced quality standard for base materials used in high-reliability PCBs for critical applications, with particular reference to the prevention and detection of foreign material inclusions early in the supply chain.

# **i3 Nets Contract to Supply Substrates** for Military Use

The company has announced that an industry leading aerospace and defense firm has awarded the company an order for the supply of advanced substrates for a military application.

# **Cutting Dynamics Employs Robot to Transform Busines**

Cutting Dynamics has joined the roster of advanced manufacturers using collaborative robotics to transform its business, adding a Baxter robot to a critical part of its thermal deburring line in its Avon, Ohio plant. Baxter works alongside the company's team of aerospace manufacturing engineers, automating the finishing process for its line of high-precision parts.

# **DARPA Unveils Tool to Identify Counterfeit Electronics**

"The Advanced Scanning Optical Microscope one of many IRIS-developed technologies—offers important hardware security and reliability assurance capabilities," said Kerry Bernstein, DARPA program manager. "These tools are optimized to support the mission of ensuring trust in microelectronics in DoD labs such as NSWC Crane."

# **New JEDEC Subcommittee: Focus on Emerging Tech**

JEDEC Solid State Technology Association announced that its IC-13 Government Liaison Committee has formed a subcommittee focused on evaluating new and emerging electronic device technologies for potential future insertion in military, aerospace, and other special use applications.

# **CEA Lauds FAA's Ruling on Drones**

The decision by the FAA is an important milestone as the agency develops rules to allow unmanned aircraft to operate safely in U.S. airspace.

# **Going Beyond X-rays for Advances Imaging in the Field**

Seeking to expand the nation's capability to detect and identify materials that are not easily visualized by conventional imaging technologies, DARPA released an announcement inviting proposals to develop portable, next-generation imaging tools that combine the complementary benefits of Xray and neutron radiography.

# **Electronic Warfare Systems Market:** \$13.2B by 2024

The global electronic warfare systems market is expected to value US \$10.2 billion by the end of 2014, which is estimated to increase to US \$13.2 billion by 2024, representing a CAGR of 2.68% during the forecast period.

# Military Unmanned Aerial Vehicles Market to Hit \$5.26B

New analysis from Frost & Sullivan, "Global Military Unmanned Aerial Vehicles Market Assessment," finds that the market earned revenues of \$3.87 billion in 2013 and estimates this to reach \$5.26 billion in 2022.

# **U.S. GDP to Grow 3% by 2016**; **Defense Spending Rises**

UCLA Anderson Forecast's third quarterly report of 2014 indicates that the real Gross Domestic Product for the United States will grow at approximately 3% over the next two years, following a decline of 2.1% in the first quarter of this year and a rebound of 4.2% growth in the second.



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VT-4A2	2.2W/m.K.	<b>V</b>			
VT-4B1	1.0W/m.K.	<b>V</b>			
VT-4B3	3.0W/m.K.	<b>V</b>			
VT-4B5	4.2W/m.K.	<b>V</b>			
VT-4B7	6.5W/m.K.				

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# The Qualities of Great Bosses

by Abby Monaco, CID INTERCEPT TECHNOLOGY

One Friday morning, coffee in hand, I read an article on LinkedIn by Jeff Haden, titled 8 Qualities that Make Great Bosses Unforgettable.

I didn't think much of it until the end of the day when I had a moment to appreciate how amazing my boss really is. Haden is so right.

Read the article and consider your own company. Does your boss fit this description of a great boss?

My boss certainly does. Based on Haden's article, the following is a tribute to my boss, Steve Klare.

# 1. They believe the unbelievable.

In 1983, Steve founded Intercept Technology. He was employed at Lockheed-Martin at

the time, and saw that his department was either going to relocate him or lay him off. Rather than move his young family, who had just settled into their newly built home in an Atlanta suburb, he decided to put his skills to use as an electrical engineer. He began working contracts privately, and slowly but surely built a business that became an EDA software vendor. The growth was unbelievable. Years of stability have followed, and I have been part of it.

# 2. They see opportunity in instability and uncertainty.

In 2001, while we were at PCB East in Worcester, Massachusetts, I watched the twin towers fall. My boss, a colleague, and I rented



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### THE QUALITIES OF GREAT BOSSES continues

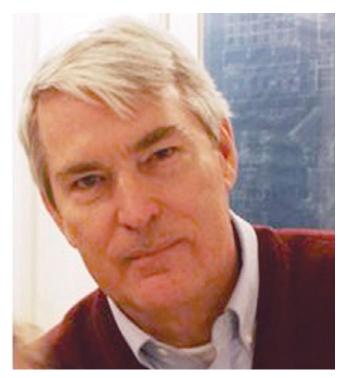


Figure 1. Steve Klare is founder and president of Intercept Technology.

a car and drove in shifts all the way back to Atlanta without stopping. We had no idea what to think. But Steve predicted that military contracts were going to heat up, and that we were going to forge ahead with new products. He hung an American flag at the front door of our office and told us the best thing we could do was get to work. So we did, with pride in our hearts and renewed energy.

# 3. They wear their emotions on their sleeves.

You don't want to be on Steve's bad side, but his acceptance of employees as more than minions certainly opens the door to that side of him. He is very open-minded, and allows us the freedom to speak our minds. Meetings tend to be places of much creative thinking and working out tough problems as a team. There have been many times that I blurted something out that was especially inappropriate, mostly in my earlier days.

One time I suggested that we call a new product "Dominatrix," having no clue what a

dominatrix actually is—yes, I err on the naïve side, but I also like big words. I was laughing my head off in a room full of my completely silent, male colleagues. I honestly thought a dominatrix was just a bossy woman.

It normally takes anywhere from a few days to a week to get back in Steve's good graces, and often avoidance is the only way to live down an offense. For not firing me the several times I had to stick my foot in my mouth, and for understanding that we all make stupid mistakes, I offer my gratitude. My good days have outnumbered the bad, and I'd sure like to keep it that way.

The good side of Steve is two-fold. First, he has a brilliant mind. We'll think we have all the answers, and then he makes one statement that changes the game entirely. I often feel like I'm playing checkers, but he's playing 3D chess. Second, he is a mushy old teddy bear. If anyone has a personal problem, he listens. If anyone has a new baby, it's all he can do not to visit in the hospital to cuddle the little one himself. Many of us look to him as a father figure.

If anyone is misbehaving (like surfing LinkedIn instead of working), he quietly roots out the issue by asking questions to make it obvious that you know he knows. It is that scary skill of catching you red-handed, but not getting mad, that leaves us all so focused and dedicated. And we don't want to let him down. For all the times I was answering a text instead of working, thanks for understanding that sometimes we just need a five-minute break.

# 4. They protect others from the bus.

As Haden says in his article, "Memorable bosses see the bus coming and pull their employees out of the way, often without the employee knowing until much, much later..."

I've seen it happen over and over again. One of us flails our way into a terrible situation, and Steve tells us how to dig ourselves out or creates a strategy to undo the damage with no harm done. He seems to understand that we all do dumb things sometimes, and that working on the solution is so much more useful than flogging whoever got out of hand. He knows we feel like the biggest idiots without him saying a word.

# THE QUALITIES OF GREAT BOSSES continues

# 5. They've been there, done that ... and still do that.

One time, we had a customer conversion contract come in. It sat in the background because we were all too busy to take it on, and then the customer began to ask where his conversion was. Steve asked around, saw the problem, and took on the task himself. I was originally hired to do conversion work in 2001, and here was my boss, doing my menial tasks because he felt that what I was doing was too important. He just jumped onto the team and took care of business.

# 6. They lead by permission, not authority.

None of us want to see Steve retire, and he swears he'll work until he's 85. In Haden's words, we truly are "motivated and inspired by the person." Steve built this company on hard work and hard play, and we are more than happy to be part of it.

# 7: They embrace a larger purpose.

My co-workers and I are treated like human beings, individuals with minds and struggles of our own. If we need a break, we can throw in the towel and cry exhaustion. When we're really grinding, we give up nights and weekends to make sure the team can keep moving without one of us holding up progress. And we do this willingly because we believe as strongly as Steve that we can do it. Ours is a small company tackling big ideas, and it's tremendously satisfying to see our work come to fruition.

### 8: They take real, not fake, risks.

So many times at meetings, I've said, "Why do we need that?" Or, "That's going to take a

lot of manpower." One of our most challenging and successful projects was redesigning our 20-year-old Pantheon suite to meet modern user interface standards. Year after year, we lamented that we couldn't spare the necessary manpower to update our now-clunky tool. Finally, Steve challenged the engineers to stop grumbling and find a way to make it happen. After a month or two of working on it alongside other projects, one of our engineers found a way to cut the project time down to a mere six months. We had estimated three years.

So, after six months of some really hard work by everyone, we released a shiny new PCB software tool. New sales start flowing in, and our existing customer renewals took a jump up. Winning the NPI award at PCB West felt like the pinnacle of all my years of work at Intercept.

What a cool way to work: to be led by example, inspired, and motivated year in and year out. When I look at who I was 14 years ago when I was hired at Intercept, I can't believe the heaps of experience, business acumen, and wisdom I've learned from Steve. I can only hope to continue to live up to his expectations.

Think about it: Is your boss a great boss? If you're a manager yourself, are you one of the great ones? Read Haden's article and give it some thought. It's never too late to strive for greatness. **PCBDESIGN** 



Abby Monaco, CID, is a director of products and marketing for Intercept Technology. She can be reached by clicking here.

# **New Material Could Pave Way** for Flex Electronics, Displays

Researchers from the University of Cambridge have identified a class of low-cost, easily-processed semiconducting polymers.

For years, researchers have been searching for

semiconducting polymers that can be solution processed and printed. These materials are used in printed electronic circuits, large-area solar cells and flexible LED displays.

"These materials resemble tiny ribbons of graphene in which the electrons can zoom fast along the length of the polymer chain, although not yet as fast as in graphene," said Dr. Deepak Venkateshvaran, the paper's other lead author.

# The Key to Increasing Quality: **Bribe Your Employees**

# by Bob Tarzwell with Dan Beaulieu

**DAN:** Back in the 1990s when Bob owned a board shop in Canada, the company was going through a bad stretch, as board shops sometimes will. Yields were way down and they were losing a lot of boards for stupid reasons, many having to do with carelessness and apathy. Bob tried yelling and screaming, but, not being a naturally gifted yeller and screamer, Bob proved ineffective at this method. So he knew he had to try something new.

He thought about it and came up with a bright idea. Knowing that for the most part his workers were inexperienced and not very technical, he decided to bribe them to do better work. He would offer them something they cared about, something they valued, so that they would in turn care about the boards they were building and try to be more careful in the future. So, he determined his team's true areas

of interest and bribed them with booze, food and Loonies (that's Canadian slang for money, named after the common loon pictured on the \$1 Canadian coin).

I'll let Bob tell the rest of the story:

**BOB:** Dan's right. Before I came up with the bribing idea, I had tried the "big mean boss" approach. I used to gather all of the damaged and non-sellable product made during the month, label the boards with their prices so everyone could see how much they were worth, and put them on tables in the lunch room. Then, on top of each pile of boards I would place a picture of what you could buy with what that scrap was worth. On one table sat a picture of a Mercedes Benz; on another there was a picture of a ranch house and so on. Finally, on one table I just put the amount the scrap was worth, which worked





# **DESIGN NEWS**

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November 5	PCB Carolina in Raleigh, NC Presented by the IPC Designers Council Chapter  This full day of education, vendor exhibition, and networking includes breakfast, luncheon, and an evening reception all free to attendees.
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December 3–5	CID+	Redmond, WA
February 20–22, 2015	CID and CID+	San Diego, CA in conjunction with IPC APEX EXPO

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To schedule a session for your team — at your facility — contact Anne Marie Mulvihill, IPC Design Programs Manager at +1 847-597-2827.

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# THE KEY TO INCREASING QUALITY: BRIBE YOUR EMPLOYEES continues

out to be the average worker's pay for a year.

Then I would hold a meeting and point out how much money we had lost, providing examples of what that amount of money could buy. I got mad and started yelling that if they did not straighten up, I was going to start firing people. I actually shouted the old cliché, "Heads are going to roll!"

But that never really worked. You see, in Canada, if you lose your job you get 17 weeks of social payment for unemployment, and then 64 weeks of partial payments. Hell, in that part of rural Canada where the cost of living was so low, getting fired was just like getting a year off with pay.

I realized that the staff did not care if they lost their jobs. That's when I decided to use bribery.

First, I started an "Employee of the Month" program, with my personal parking spot as the grand prize. The employees liked that because it wasn't just that they got my parking spot; I also had to park in the worst spot in the parking lot—the one farthest from the door. They had some fun showing the winner's picture in the cafeteria, with a picture of my car in that bad spot out in the North forty.

While this was going on, I heard other suggestions from employees. One idea was to hold a barbecue if we hit certain quality goals. That sounded good, so we tried that too. We had a few Friday lunch barbecues. We had a good time, and it also gave me the opportunity to talk about our quality improvements, so that worked out well. After we started these projects, our yields were at about 75%.

Once we started the barbecues, I posted a big thermometer in the lunchroom to serve as a scoreboard so everyone could see how we were doing. I marked the thermometer with some goals. When we hit 80%, we'd get hot dogs for lunch; at 85%, steak sandwiches and beer; at 90%, one-inch steaks and beer, and at 95%, we'd hit the jackpot with two-inch steaks and lobsters flown in from Prince Edward Island along with beer and wine. And the best part was that I would barbecue them in my shorts. This was January in Canada and bloody cold. But I did it in sub-zero temperatures...I was outside cooking in my shorts!

But there was one last thing to do to keep the excitement going and the employees engaged. I knew it was one thing to get to 95% yields and quite another to maintain that level of quality forever, so I came up with a bonus program. I not only applied this program to yields, but to on-time delivery as well. Payment for these bonuses was based on levels, department performance, and whole company performance. In this way, the employees not only had to be focused on their own performance, but also the performance of others in their departments and throughout the company. This led everyone to work more closely together to make sure that they all got their bonuses. It also led to employees self-disciplining each other to ensure that no one was slacking off.

And, yes, it worked. We not only maintained our 95% yields and on-time deliveries, but we often hit the 97% and 98% levels too. It was a good deal for everyone.

At sales of \$2 million a year and 75% yields, I was losing a half a million dollars each year. All it took was a little fun and a couple of thousand well-spent dollars, and the employees were a heck of a lot more engaged and the company started making a whole lot of money.

All it took, as Dan would say, was a little common sense. PCBDESIGN



Bob Tarzwell is a PCB consultant who has spent 50 years in the PCB industry, inventing technology and building almost every type of PCB. He is the co-owner of DB Publishing, publisher of the PCB 101 and

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Dan Beaulieu is a well-known industry consultant and coowner of DB Publishing. His column It's Only Common Sense appears Monday mornings in the I-Connect 007 Daily Newsletter. He can be

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# News Highlights from PCBDesign007 this Month

# **Mentor Graphics Unveils Xpedition System Designer**

Mentor Graphics has announced the newest offering and key building block in the Xpedition platform, the Xpedition Systems Designer product for multi-board systems connectivity. Xpedition Systems Designer captures the hardware description of multi-board systems, from logical system definition down to the individual PCBs.

# **Measurement Group Keysight Separates From Agilent**

Keysight Technologies has completed its separation from Agilent Technologies. The newly independent company will begin "regular-way" trading on the New York Stock Exchange immediately under the ticker symbol KEYS.

# **Zuken Enhances Project Management Expertise**

Zuken has reached a corporate development milestone as it expands its project management capabilities across Europe and the Americas. Most Zuken engineers and managers who have customer contact have received additional training based on International Project Management Association (IPMA) methodology. A specialist group has received advanced training to achieve IPMA Certified Project Management Associate status.

# **ICD Adds Dielectric Frequency Compensation**

In-Circuit Design Pty Ltd (ICD), Australia, has incorporated dielectric frequency compensation into its latest software release. This new feature allows the user to correct for the frequency dependency of the dielectric material.

# **Digi-Key, Mentor Graphics** Launch New EDA/CAD Tools

Digi-Key and Mentor Graphics Corporation have launched new professional-level EDA/CAD tools, starting at under \$200 for design starts providing a foundation for long-term product design. The jointly developed Designer Schematic and Designer Layout tools are available from Digi-Key.

# **Partnership Provides PLM Capabilities to ECAD Design Teams**

Altium Limited has partnered with Aras, the next leader in enterprise PLM to provide advanced PLM capabilities to ECAD design teams. "Team collaboration and ECAD design management are fundamental needs in today's electronic design environments," said Jason Hingston, CTO at Altium.

# Aspen Labs, Digi-Key Launch Free PCBWeb Designer

Aspen Labs, a joint-venture partner of Hearst Electronics Group, in cooperation with Digi-Key, launched PCBWeb Designer, a free schematic capture and layout EDA/CAD tool for design engineers. The new software is available globally today as a full-license application with no limitations on number of parts, size or layer count, supporting a standard Gerber output.

# **Cadence Posts Strong Q3 Results**

Cadence reported third quarter 2014 revenue of \$400 million, compared to revenue of \$367 million reported for the same period in 2013. On a GAAP basis, Cadence recognized net income of \$38 million, or \$0.12 per share on a diluted basis, in the third quarter of 2014, compared to net income of \$39 million, or \$0.13 per share on a diluted basis, for the same period in 2013.

# **DesignCon Releases 2015 Keynote Program**

DesignCon 2015, the 20th anniversary of the event, has posted a robust keynote lineup with influential electronic design professionals from Stanford University, Synopsys, and Efficient Power Conversion Corporation that will take attendees through a narrative of the industry's past, present, and future.

# **Altium Designer 15 Eases High-speed PCB Design Woes**

Altium Limited has announced the upcoming release of its professional printed circuit board (PCB) and electronic system level design software, Altium Designer 15. "Altium's R&D engagement with customers is reflected in this software release. We're very happy with the clear feedback and technical advice about high speed PCB design offered by our dedicated beta users over the last 12 months," says Altium's CTO, Jason Hingston.



# EVent

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out The PCB Design Magazine's event calendar.

# **36th International Electronics Manufacturing Technology Conference**

November 11-13, 2014 Johor, Malaysia

# **International Wafer-Level Packaging Conference**

November 11-13, 2014 San Jose, California, USA

# **TSensors Summit 2014—San Diego**

November 12-13, 2014 La Jolla, California, USA

#### **Wearable Sensors and Electronics 2014**

November 12-13, 2014 Santa Clara, California, USA

#### **ELECTRONICA 2014**

November 11-14, 2014 Messe Munchen, Germany

# **High-Reliability Cleaning and Conformal Coating Conference**

November 18-20, 2014 Schaumburg, Illinois, USA

# **Graphene LIVE! 2014**

November 19-20, 2014 Santa Clara, California, USA

# **International Printed Circuit & APEX South China Fair**

December 3-5, 2014 Shenzhen, China

# **DesignCon 2015**

January 27-30, 2015 Santa Clara, California, USA

### **IPC APEX EXPO 2015**

February 24-26, 2015 San Diego, California, USA



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# **ADVERTISER INDEX**

# **Coming Soon to** The PCB Design Magazine:

# **December:**

# **High-Density** Interconnect

In December, we'll dive into HDI and take a look at what 2015 might hold for the PCB design community.