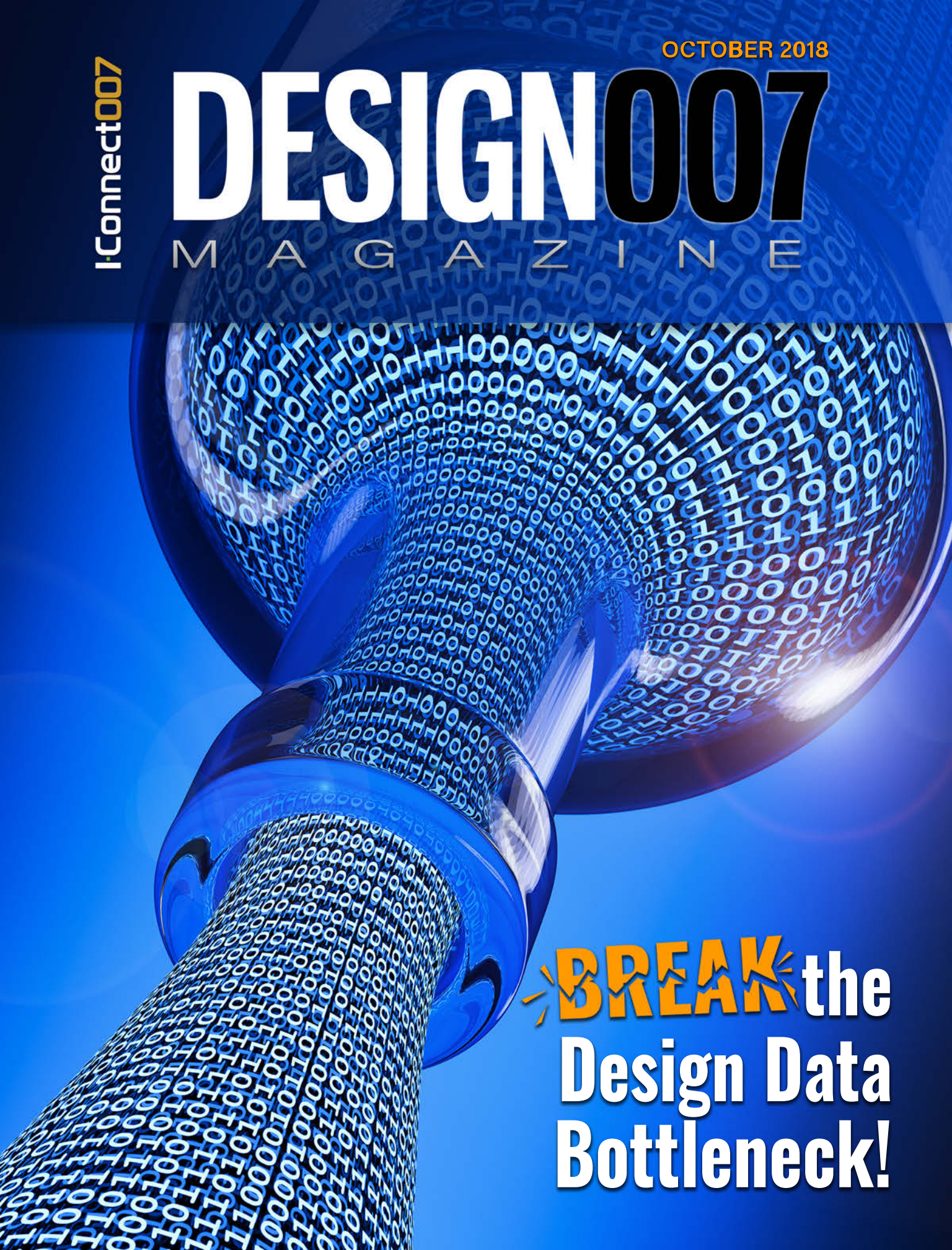
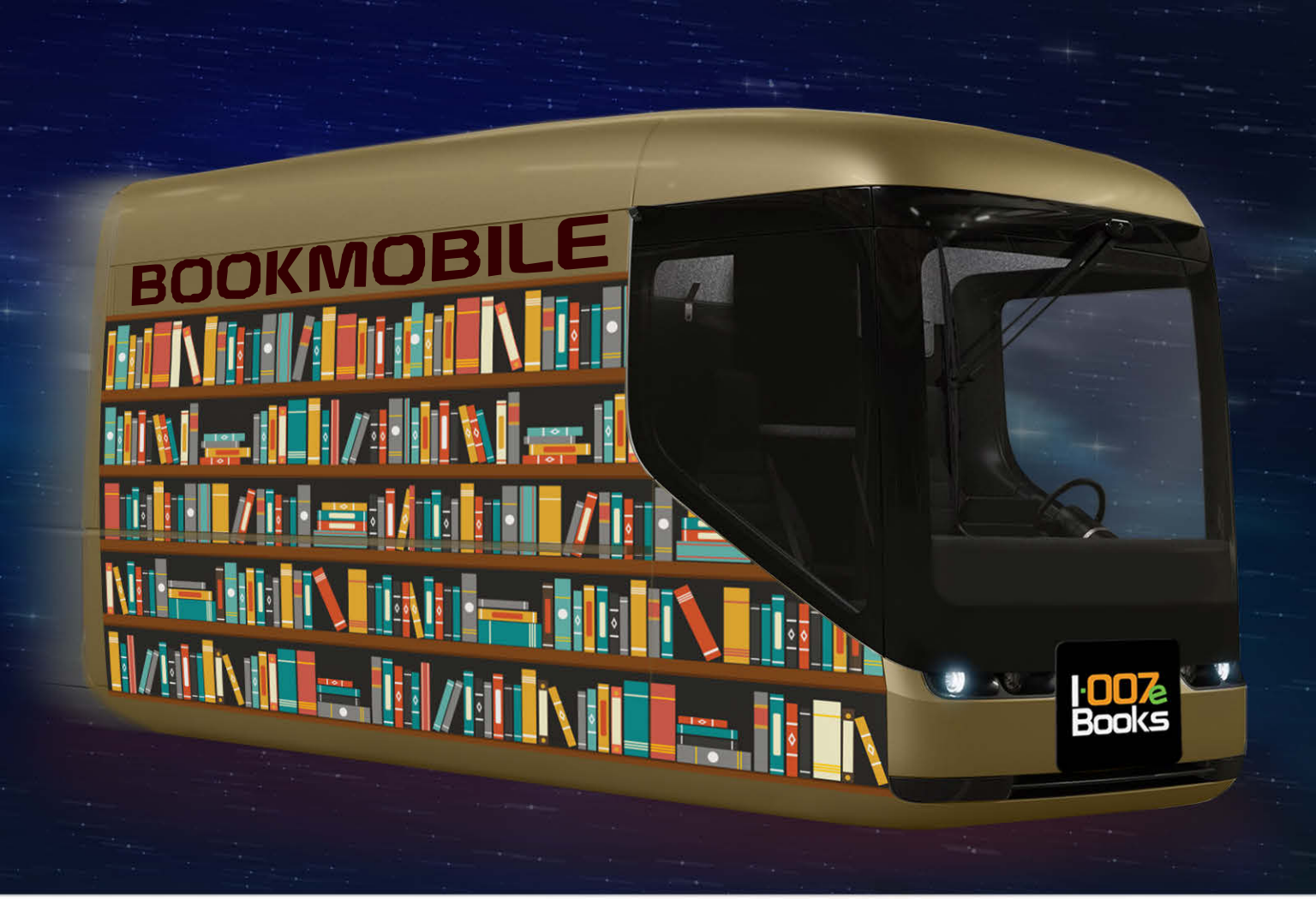
I-Connect007

OCTOBER 2018

DESIGN007 MAGAZINE



BREAK the Design Data Bottleneck!



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Design Data Packages

You've heard the stories. Most CAM departments say that anywhere from 80–100% of designs from new customers are inaccurate or incomplete, often necessitating a Friday afternoon call to the designer, or the job being put on hold. So, what can we do to optimize the design data package and make the handoff to the fabricator as smooth as possible? We asked a variety of industry experts to weigh in on this topic.

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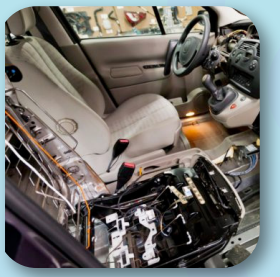

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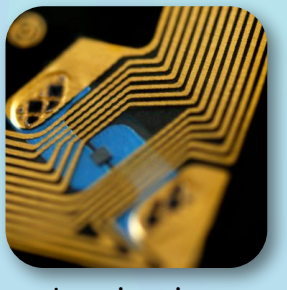

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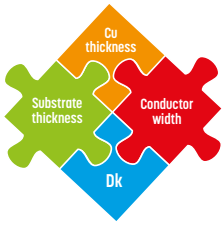

Despite Progress, Design Data Issues Continue

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

It seems so simple —you design a PCB, hand off the design to a fabricator, along with notes describing your design intent, and they manufacture the board. Everyone gets paid, and everyone's happy, right?

Wrong.

Much of the time, that's not how it works out—not even close.

You've heard the stories. Most CAM departments tell us (are they telling you?) that anywhere from 80–100% of designs from new customers are inaccurate or incomplete, often necessitating a Friday call to the designer, or the job will be put on hold.

This has been an ongoing problem for decades, and it doesn't seem to be getting any better—at least from the viewpoint of CAM personnel. The problem is so prevalent that columnist Mark Thompson has built quite an audience by writing about design data packages and sharing his treasure trove of horror stories about data gone wrong.

Most of you are not new to the industry, shall we say. Many of you have at least 30 years of experience designing PCBs. You've done this hundreds of times before. But why are we still seeing so many errors during the post-processing part of the design flow?

You might think that constant improvements to the Gerber, ODB++, and IPC-2581 data formats would make issues like this a thing of the past. However, much of the data package is still dependent upon the designer's ability to describe how they want the board built. It's the little things that trip up a design, such as failing to specify whether a quarter ounce of copper is the weight before or after processing.

Part of the problem is that CAM people often fix the error without telling the designer, so the designer never knows that there was a problem in the first place, which perpetuates the issue.

What can we do to optimize the design data package and make the handoff to the fabricator as smooth as possible? We asked a variety of industry experts to weigh in on this topic.

Steph Chavez, a CID instructor with EPTAC Corporation and IPC Designers Council Executive Board member, explains how designers can break the design data bottleneck, and why it's so critical that designers and fabricators stay in touch throughout the design cycle. Mark Thompson brings us a feature column that explains what fabricators would like to see in each design data package. (Shameless plug: This column details Mark's new I-Connect007 eBook, *The Printed Circuit Designer's Guide to… Producing the Perfect Data Package.*)

Next, CAM engineers JanNell Taylor and Andy Schilloff of GreenSource Fabrication discuss their preparation for the company's upcoming entry into the commercial market, and how they will be able to trigger jobs from their off-site location in a different state. Then, Kelly Dack, CID+, answers the old question, "What's in a name?" He discusses many of the ways that designers are inadvertently shooting themselves in the foot by assigning similar or confusing naming conventions to layers of artwork. We wrap things up with a feature by columnist Jan Pedersen of Elmatica who explains the need to move design data fully into the digital realm. As Jan says, "We're close, but we're still not quite there yet."

This month, we're introducing a brand-new column, "Connect the Dots," by Bob Tise and Dave Baker of Sunstone Circuits, as well as columns from our regular contributors Barry Olney, Vern Solberg, and John Coonrod. We also have an interview with Mike Creeden and Steph Chavez from the IPC Designers Council who discuss their upcoming column "The Digital Layout," which will launch next month.

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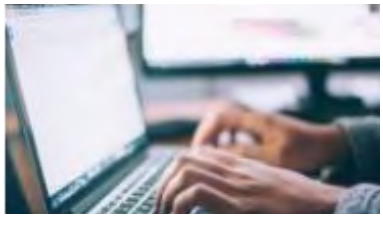
Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 18 years. He can be reached by clicking here.

New Half-Light Half-Matter Particles May Hold the Key to a Computing Revolution

Current computing technology is based on electronics, where electrons are used to encode and transport information.

Due to some fundamental limitations, such as energy-loss through resistive heating, it is expected that electrons will eventually need to be replaced by photons, leading to futuristic light-based computers that are much faster and more efficient than current electronic ones.

Physicists at the University of Exeter have taken an important step towards this goal, as they have discovered new half-light, half-matter particles that inherit some of the remarkable features of graphene, the so-called "wonder material."

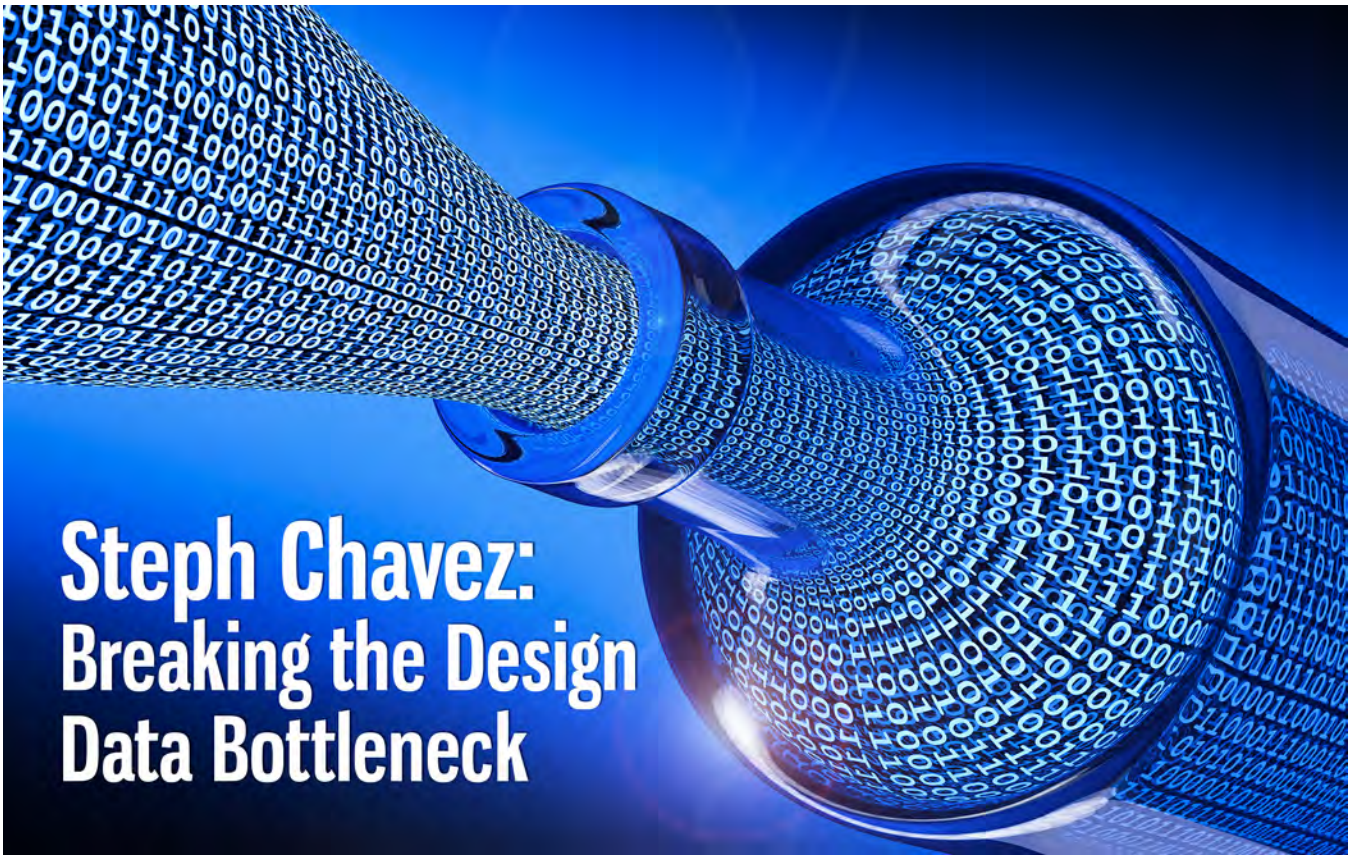


This discovery opens the door for the development of photonic circuitry using these alternative particles, known as massless Dirac polaritons, to transport information rather than electrons.

A unique feature of Dirac particles is that they mimic relativistic particles with no mass, allowing them to travel very efficiently. However, it is very difficult to control them. This fundamental drawback—the lack of tunability—has been successfully overcome in a unique way by the physicists at the University of Exeter.

"Our work has crucial implications for the research fields of photonics and of Dirac particles," adds Dr. Eros Mariani, principal investigator on the study. "We have shown the ability to slow down or even stop the Dirac particles, and modify their internal structure, their 'chirality' in technical terms, which is impossible to do in graphene itself."

(Source: University of Exeter)



Steph Chavez: Breaking the Design Data Bottleneck

Feature interview by Andy Shaughnessy
I-CONNECT007

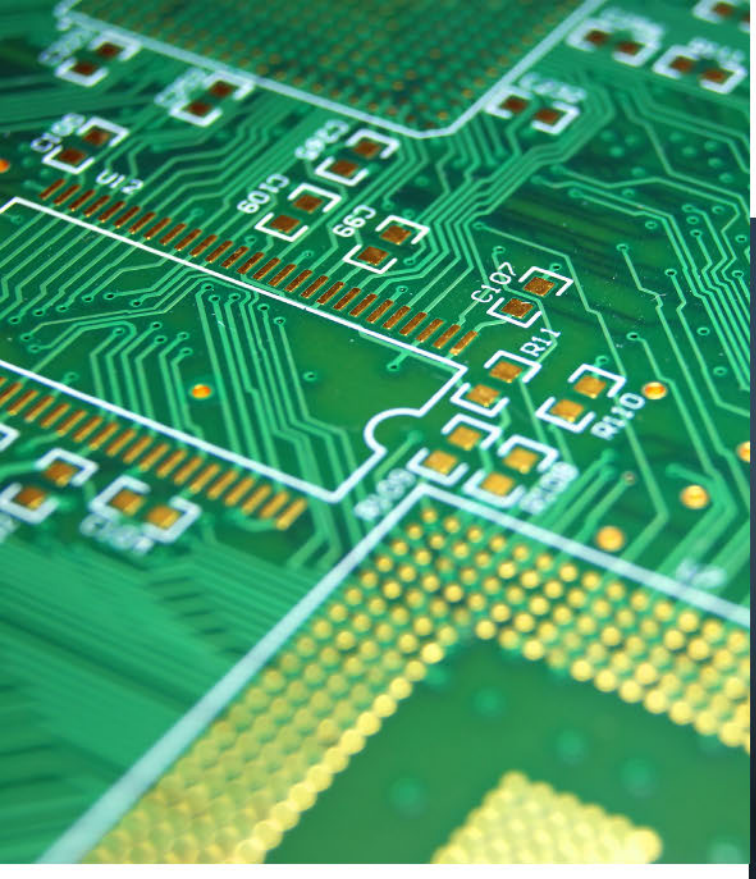
When we started planning this issue on design data, I knew we'd have to speak with Steph Chavez.

Andy Shaughnessy: Steph, can you tell us about your background? Then, we'll talk about what you are seeing and hearing regarding PCB design as a design instructor for EPTAC Corporation.

Steph Chavez: Sure. I hold a seat on the global IPC Designers Council (DC) Executive Board. I am my local area's IPC DC chapter president in Phoenix. I have about 28 years of experience in the industry. I've spent the last 15 years of my career as a lead designer successfully designing a wide spectrum of PCB designs—both simple and complex—including HDI, flex, and rigid-flex. I've also led global PCB design teams, which include managing diverse, multicultural teams in multiple time zones. The foundation of my education and leadership stems from my time in service in the U.S. Marine Corps as an avionics technician. Whenever I'm speaking, I always stress that you should have plenty of knowledge resources in your "bag of magic," so to speak, This includes establishing your professional network, which I believe this is key for your overall success. I-Connect007 is a great resource of knowledge sharing and up-to-date industry content.

Shaughnessy: We appreciate that. We like to publish information that designers can use right away. Speaking of which, one thing everybody was talking about at IPC APEX EXPO 2018 was data. The Design Forum hardly covered anything about how to design a board; it was all about data. You hear from fabricators that 90% of new customers submit design data packages that are incomplete or inaccurate. They don't provide an updated netlist, etc. You said that you've been dealing with a lot of data issues lately. Can you tell us about that?

Chavez: As a designer, when you think about the data you're presenting or handing off to



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Steph Chavez

your suppliers, you should have a basic understanding of IPC standards because that is how you're going to communicate your intent to your fabricator and assembler. At the same time, you need to fully comprehend what you are giving to your suppliers and what you are stating in your fabrication and assembly drawings. Are you correctly stating your fabrication or assembly notes? Do they make sense? Do you have all the required information listed to fabricate your PWB or assemble your PWA successfully? Do you have statements in your drawings that conflict with one another and could cause confusion? Worse yet—and I feel this is the root of the problem—do you understand your company's documentation details, or are you just "rubber stamping" your documentation because "that's how it's always been done?"

These are some of the questions that come to mind when I think about bad data being handed off. Board design construction is key for success and getting the details correct is paramount. Many times, bad data is given because people are not paying attention to the details. Some designers simply don't know what they don't know and pass on bad data.

In my experience, when you get into production runs with a top-tier supplier, they will not change or modify your data without permission. If you send a job over to them with issues, concerns, or missing data, chances are it's going to be put on hold. By the time you receive any feedback that your job has been put on hold, it could be five or more days lost in a schedule before you can address these issues flagged by the supplier. For many companies, that's a huge negative hit. The sad thing is that this usually stems from something that could have been easily mitigated up front in the beginning stages of your design with the supplier.

Shaughnessy: Communication is the key, as we keep hearing.

Chavez: Exactly. Let's discuss PWB classes, for example. If you don't have the requirements for Class III implemented in your design, but you ask the supplier to build to Class III, the supplier will kick your data back and say it's physically impossible and your board isn't designed correctly for it. Then what do you do? Find a board shop somewhere that can build it once if you're lucky, or do you go back and redesign your board appropriately for a Class II design? That's why it's paramount that you understand IPC specifications and bring in your fabricator at the beginning stages of the design process. You should discuss stackups and all the details that make up your board depending on if it's a Class II or III design. This is one piece of information you need to know before starting—not something you find out afterward when your design is finished.

By engaging your suppliers early in the design stage, you'll ensure that everything aligns, is cohesive, and meets the basic industry IPC standards to make the smoothest transition from design to fabrication, assembly, and test. The transitions could be from you as a designer to the manufacturer, or from the fabricator to the assembler, with the least amount of resistance. Then everything is optimized. This is why three perspectives have been identified for a successful design that must be met: layout solvability, performance (routing solvability that includes signal and power integrity), and DFX (manufacturability). I refer to this as the "Designer's Triangle." The end result is making the first revision work!

Shaughnessy: We keep hearing CAM departments complain about receiving bad data—even from senior designers who know how to design a complex board.

Chavez: Just because someone has a senior designer title doesn't mean they truly comprehend what they are doing or are paying attention to all the details. I've come across design-

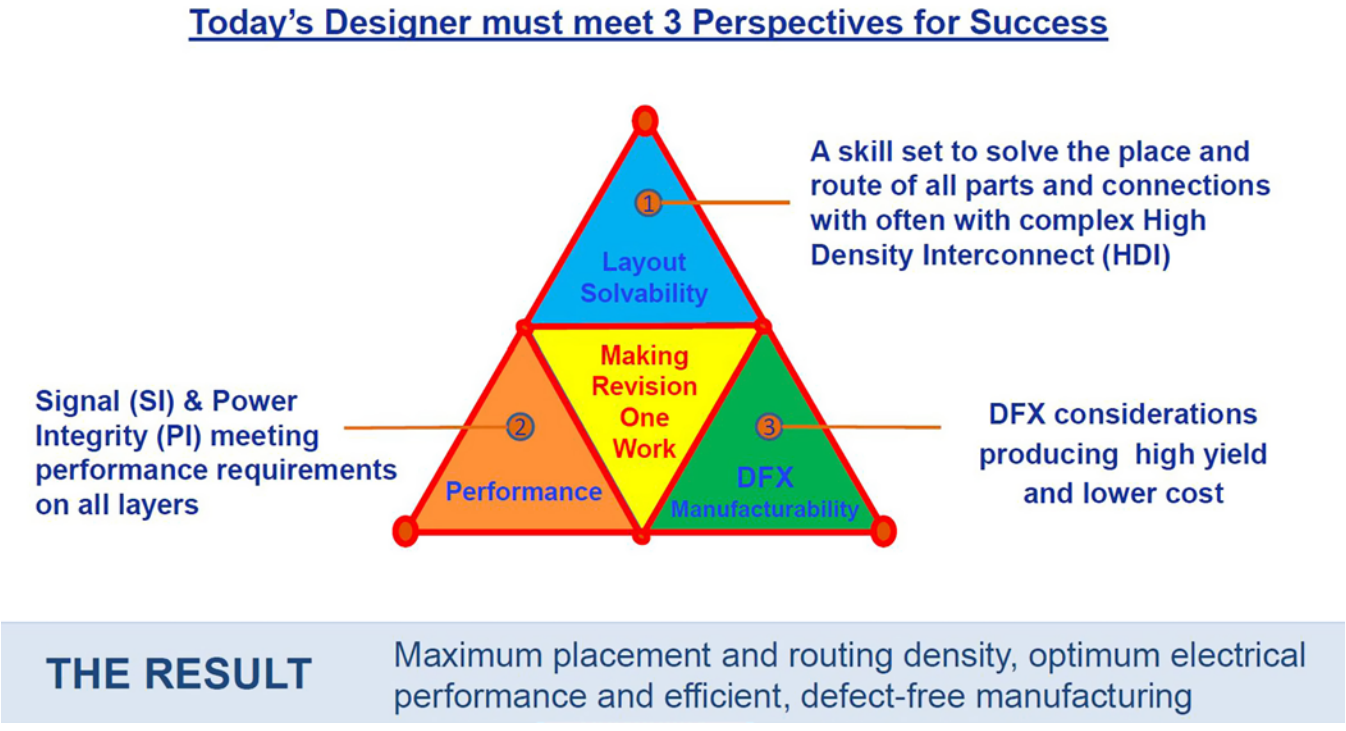

Figure 1: The "Designers Triangle."

ers with many years of experience in my career that have bad habits. Bad habits are major contributors to bad data being supplied to the fabricator. I know from experience and from discussions with my fellow IPC CIT instructors that there are seasoned veterans with many years of experience and complex designs under their belt who fail the IPC CID or CID + certification courses. These senior designers tend to get caught up in their own world, or worse, become legends in their own mind. They think they know everything and don't continue their professional development. Over time, the fabricator bails them out by catching their mistakes from the feedback of the CAM engineers, as you mentioned.

Shaughnessy: I'll often ask designers if they regularly speak with their fabricators, and a lot of them say they never do because they don't know who's going to build it. They don't know who will do the prototypes or build production volumes overseas. Instead, they output in Gerber and Valor—so they're fairly safe—and then they wait for the call about what's wrong.

Chavez: You're absolutely right, when it comes to many companies and how they procure boards. Sometimes you don't know who is building your board. Generally, if you follow IPC standards, you'll minimize your overall risk. You should design your PWBs per IPC standards at a minimum, then no matter where it's fabricated or who is fabricating it, you will have success. When you start deviating from IPC standards, negative issues begin to present themselves. This is why communication is key. To achieve overall success and make revision one work, you should design your board per IPC standards at a minimum. If you do this, your designs will have a much lower risk going into fabrication, and you'll end up with a positive result.

I'm flabbergasted as to why many designers don't pick up the phone and call their supplier. You and your supplier should be on a first-name basis. You don't want to guess in this game.

Recently, I've done some research on outputs regarding data formats. Which output should be the primary output for suppliers—Gerber along with IPC-D-356 netlist, ODB++,

or IPC-2581 data? Which is the preferred format? I gathered information from many suppliers throughout the U.S. as well as globally.

Shaughnessy: What did you find during your research?

Chavez: It was amazing to find out that it was not consistent from one supplier to another, or even consistent within a global supplier that has many divisions throughout the world. One division of a large top-tier company preferred Gerber data along with an IPC-D-356 netlist, while another division of the same company on the other side of the world preferred ODB++ data. That particular division even provided discounts for sending ODB++ data over any other format. When I received the feedback, I thought, "You're all the same company, so why aren't you on the same page and preferring the same data throughout all your divisions?"

From my initial research, it appears that there more people accept ODB++ data over IPC-2581 at this time. However, my research also pointed out that Gerber data along with an IPC-D-356 netlist was still the leading data format that most suppliers prefer. Yes, both ODB++ and IPC-2581 data formats provide more intelligent content that you'd prefer to share instead of Gerber data. Those intelligent formats have everything you need for both fabrication and assembly all in one dataset package. That is what makes those formats better and more powerful to use, but not everybody is accepting these formats.

That is what makes those formats better and more powerful to use, but not everybody is accepting these formats.

Let's say you go digital with one of these intelligent data formats and send it out to your long-term supplier. What do you do when your supplier says, "I'm sorry, I can't use this data format. I don't have that capability. I'd prefer to have that Gerber data along with an IPC-D-356 netlist you've been supplying me all these past years." Do you stop using that supplier and toss aside all the years of establishing relationships and successfully working with them to find a new one? If you work for a large corporation—and believe me, I have experience at several of them—it's not that easy to jump from one supplier to another, especially if getting on a company's approved vendor's list (AVL) is already tough due to required restrictions and certifications that those suppliers need to have in place. Thus, you end up going back to Gerber data along with an IPC-D-356 netlist until your suppliers update their capabilities as well.

As I said, I was amazed at the feedback I received. Gerber data along with an IPC-D-356 netlist was still the leading data format preferred in the industry when it comes to PWB fabrication.

Shaughnessy: Right. You've probably seen the surveys showing that 95% of designs are still generated in Gerber.

Chavez: Yes, I have. I was stunned at the response I received when I was onsite at one top-tier supplier and asked about what data format they prefer. They preferred Gerber data and an IPC-D-356 netlist because they take the supplied Gerber data and an IPC-D-356 netlist and generate an internal ODB++ file. I asked, "What if I eliminate that extra step in the process and provide you the ODB++ file directly from my Mentor software?" They responded, "No, we prefer to receive Gerber data and an IPC-D-356 netlist because we have a solid process in place that is effective and optimized to our internal processes." We still supply them with Gerber data along with an IPC-D-356 netlist.

Shaughnessy: Even though it would be messy to change over, I'm surprised that the industry hasn't locked into one data format.

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Chavez: What it comes down to is that companies want to be successful. It's not easy to change internal processes quickly, especially when you think of a large corporation as a big machine. It takes time and a willingness to be open to change. It will happen eventually. The industry's evolving, and we'll eventually evolve too like everyone else in the industry. It's not an overnight thing. If it were, we would have evolved to a digital flow a long time ago, and we wouldn't even be having this discussion.

Shaughnessy: What advice would you give to a designer regarding design output data formats?

Chavez: Similar to my teaching in CID and CID+ courses, my advice to my students and fellow designers is that you have to communicate with your suppliers constantly. Establishing a long-term relationship with them is a must and communication is key for overall success! You have to stay on top of what's going on in the industry. Continuous professional development and professional networking are extremely important. You should design your PWBs at a minimum of IPC standards. When you communicate with your suppliers and hand over your data to fabricate or assemble, you should speak the same IPC language and be on the same page to set yourself up for success. Regarding IPC, get involved, especially your local IPC Designers Counsel chapter. If you don't have a local chapter, why not start one yourself?

Regarding data formats, if your supplier prefers or can only handle Gerber data, then you must provide that. If it's ODB++ or IPC-2581, then you will have to evolve too, provided your CAD tool can generate those formats. These two formats are very intelligent, and in the long run, are much better formats to use. We can do so much with them, so start embracing intelligent formats and see if you can start migrating to them within your company and with your suppliers sooner rather than later. We'll get there eventually.

Concerning providing bad data to the suppliers, you have to check your data before you send it out. You'd be surprised how many people blindly toss their data over the wall. Many don't even involve their suppliers until after the fact. By then, it's too late, and you're in a world of hurt. Some designers may not even produce a fabrication document; they just send Gerber data over and say, "Build this," without any specifications or instructions. This is why you have CAM engineers pulling their hair out due to bad data being pushed on to them.

Shaughnessy: I appreciate it, Steph. Thanks for your time.

Chavez: My pleasure, Andy. **DESIGN007**

Medication You Can Wear

Drug-releasing textiles could, for instance, be used to treat skin wounds. EMPA researchers are currently developing polymer fibers that can be equipped with drugs.

For the "Self Care Materials" project, fibers are produced from biodegradable polymers using various processes. "The targeted use of the fiber determines which manufacturing process is best," explains EMPA researcher and project coordinator René Rossi.

Delicate, light membranes with a large surface are formed during so-called electrospinning. If robust fibers are required, it is better to draw the melted ingredients. In the end, all processes produce novel fibers, the nano-architecture of which is made up of several layers and components.

"The use of self-care fibers is conceivable for an enormous number of applications," says Rossi. In addition to chemical signals from the body, however, stimuli can also be used that are deliberately set from the outside to control the release of medication by the fibers. Textiles or dressings that release a remedy under slight pressure or a stimulus of light can contribute to the quality of life of patients and at the same time relieve the burden on health care staff.

The system can also be used for preventive measures. The idea behind it: Where active substances can be released, substances are also able to penetrate the fiber in the opposite direction.

(Source: EMPA)

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Getting on the Same Page: A Data Story

The Bare (Board) Truth
Feature Column by Mark Thompson, CID+, PROTOTRON CIRCUITS

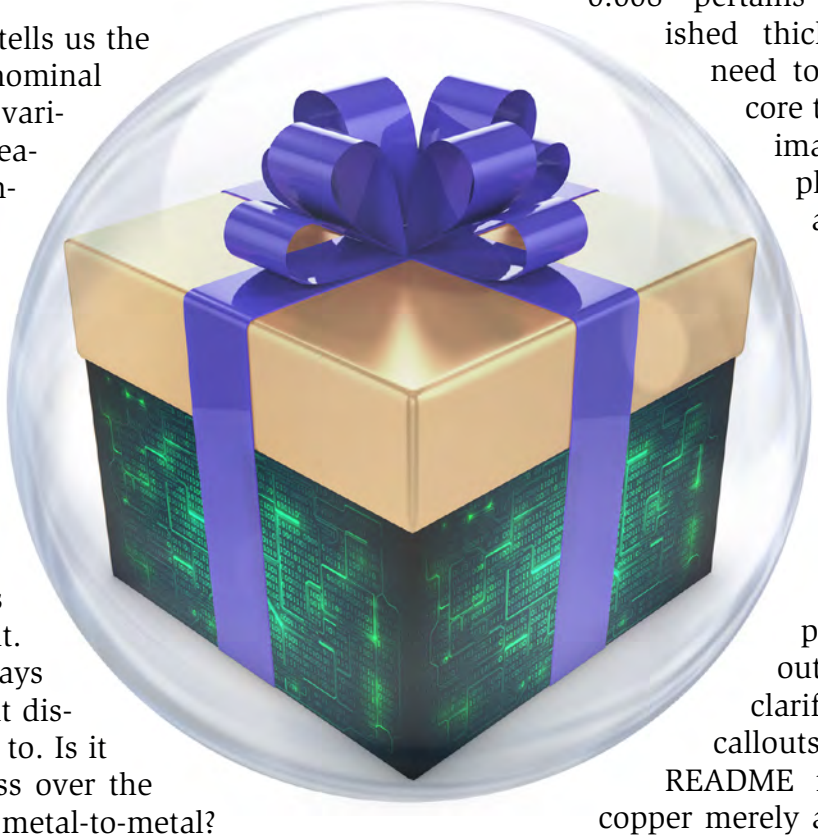
In this month's column, I will write about what makes a great incoming dataset for PCB fabrication.

Drawings and README Files

The overall part thickness should be expressed as the desired thickness measured between two points, including tolerances. For example:

- 0.062" ±10% metal-to-metal including surface finish

This description tells us the part will be 0.062" nominal with an allowed variance of ±10% measured over the finished plated metal and surface finish. If the drawing or README file merely states 0.062", the fabricator must establish whether or not this is a maximum thickness or if a tolerance is associated with it. The note also says nothing about what distance 0.062" refers to. Is it 0.062" glass-to-glass over the material, or is it metal-to-metal? Does this include plate-up and surface finish, or is it an overall dielectric with a tolerance, such as ±10%?



Thickness callouts for single-sided or double-sided orders are even more critical. As a fabricator, we can control the thickness of the multilayer by using different combinations of prepregs/cores. If a customer calls out a single-sided or double-sided job as 0.008", is this the core dielectric or an overall dielectric? If 0.008" represents the core dielectric callout on a 2-ounce finished part, the final thickness would be closer to 0.013". If the callout for 0.008" pertains to the overall finished thickness, we would need to start at a 0.004" core to finish at approximately 0.009" after plate, surface finish, and mask. Again, notes about thickness should ideally describe what the overall thickness is to be and the points from which they should be measured.

Another example of drawing callouts that can require clarification is copper callouts. If the drawing or README file expresses the copper merely as 2-ounce copper, this leaves the fabricator with more ques-

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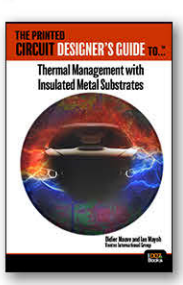

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tions. Is it a starting or finished copper callout? If the part is a multilayer board, is it 2-ounce inners and 2-ounce finished outers? If that's the case, a fabricator will start on 1-ounce copper clad outers and plate to a 1-ounce finish. IPC dictates that there be a minimum of 0.0008" copper in the barrels of the holes for conductivity concerns. Fabricators typically plate up in whole ounce increments to ensure this minimum requirement is met, so a part that started on half-ounce copper foil would finish at 1.5 ounces after plate.

If a note merely reads 1-ounce finish, the fabricator must call the customer to clarify their intentions because starting on 0.05-ounce foil and plating to 1 ounce does not meet IPC minimum requirements for hole wall thickness. A good copper callout note on a drawing or README file should indicate finished copper for both inner and outer layers as well as a reference to minimum copper in holes, such as:

- Copper clad cores and prepregs per IPC-4101/26, 83, 98
- 1-ounce copper weight on internal layers and 0.5-ounce copper plated to 1.5-ounce finish on external layers, unless otherwise specified on stackup

This description tells the fabricator a few things at once:

- Which materials they are allowed to use (4101/26, 83, 98)
- What the inner layer and outer layer starting copper will be, including finished copper

For the holes, a good note could read:

- All holes to meet IPC-6012B Class 2 annular ring
- Plated hole wall thickness to be 0.001" with 0.0008" absolute minimum

This callout gives us criteria for acceptability and a tolerance for hole wall plating. Additional notes about holes could address other items, such as allowed tolerance for true drill position. For example:

- All holes shall be located within 0.0008" diameter of the true position

Another example might describe whether or not certain hole sizes, such as vias, require conductive or non-conductive filling:

- All 0.008" vias to be filled with conductive material and the final surface shall be flat with no dimples or protrusions

This is a typical note for via-in-pad applications where the vias are drilled, filled with the conductive material, and planarized (made flat, so that no dimples or protrusions exist on the surface mount). If done right, there will be no evidence that a via even exists in the surface mount. If any holes require solder mask plugging or tenting, one might say:

- All vias to be filled and covered with solder mask

It is important to remember that the absence of such notes on a fairly complicated board can result in a clarification call or email from the fabricator that can delay the fabrication of the parts.

Too Much is Just as Bad as Not Enough

Is there such a thing as too many notes or details? Yes, an effort to give as much detail as possible can sometimes result in conflicting notes, which will also result in a call or email from your fabricator. For example, one that we frequently need to clarify is where specific dielectrics are shown on a stackup detail on a drawing. In conjunction with this, the notes on the drawing refer to the acceptable types of materials that can be used. The customer will often show a dielectric constant (Dk) value that all impedances are based upon. Many times, the Dk number does not match what the fabricator knows to be the real effective Dk of that particular subsection based on the allowed materials and customer-specified dielectric.

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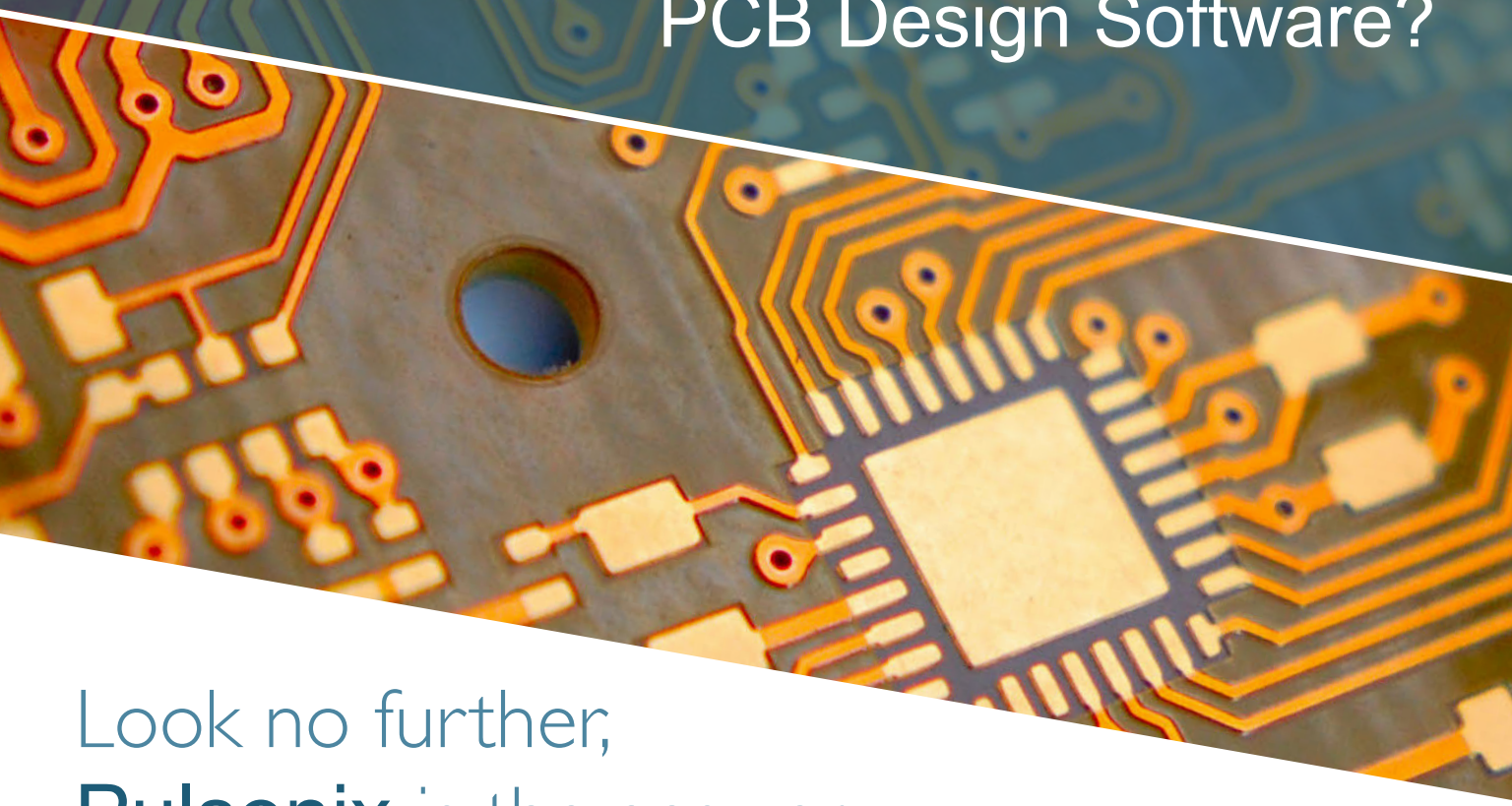

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As you know from previous columns, a general rule of thumb is that the thinner the dielectric of prepreg, the higher the resin content, and the higher the resin content, the lower the Dk. If a Dk is listed for a 0.004" dielectric subsection as 4.5, we must use thin pregs as low as 3.3 for FR-4/406 derivatives and 3.87 for the thinnest pregs on Nelco N4000-29 (a commonly allowed material for RoHS compliance and the elevated temperatures at assembly due to alternative surface finishes) to achieve this dielectric. Ultimately, this can result in the need for either altering the specified dielectrics or resizing impedance lines, which is less desirable.

The bottom line is this—avoid specific Dk or material information unless it is critical to the design. It is better to call out the material type via IPC-4101 or the number used on the material specification. Specifying Dk or dielectric numbers in your stackup may precipitate a call or email from your manufacturer and require a negotiation, which takes valuable time.

The bottom line is this—avoid specific Dk or material information unless it is critical to the design.

Pre-Quote Software

Another example is IPC-2581, which is an all-inclusive consortium package that includes the bill of materials (BOM) and assembly information as well as design and image output data in three formats. As long as there is no conflicting information between the image data—and sometimes there is—this dataset can be used. I am writing this from the standpoint of quick but accurate PCB quotes, not the validity of a given dataset, which means I don't have any issues with an IPC-2581 output for manufacturing.

However, for fast and accurate pre-quote analyses, the additional files in datasets, such as IPC-2581 and others that include multiple image outputs, can slow down the quote process. We have seen as many as six separate ODB++ outputs—some as an ODB folder, some as TGZ files, and some as ODB inside a ZIP file—all in the same dataset. Many fabricators use pre-quote software packages, such as INSIGHT or Integr8tor. Both are outstanding for what they are intended. A pre-quote design check to ensure obvious things like trace and space meet the defined copper weight and that a Drill file exists and matches the drawing.

Even though the datasets should all be the same in theory, input pre-quote packages must be edited so that only one dataset is checked. Multiple sets will stop the operation and ask for more user information, which again, takes time out of the quote process.

Additionally, file naming conventions are another way to streamline the quote process. Many design systems have a default for file names as do drawing stackup templates. Most do not match exactly, and if there are no Z-axes layer designators on the file itself, sometimes it is difficult to tell what each layer should be. For example, the image data file template may call inner plane layers "GP1" for Gerber plane 1, but your stackup may show the real names of the layer functions. Thus, GP1 of your image data may be called "GND" or "PWR" on the stackup describing the layer function more than the layer name.

This is not an issue most of the time if you provide an EXTREP file or extension representation file that describes the layer versus stackup layer names. Much like with multiple image datasets, incoming pre-quote software packages will have trouble with identifying each layer and will pause for the operator to give the system more information to continue with an analysis. As far as the pre-quote analysis is concerned, if the layer names and stackup layers can match and multiple datasets do not need to be culled before running the pre-quote software, the faster the pre-quote software works, the quicker you get your quote. Again, the purpose of this column is not to suggest you do not use IPC-2581, but to suggest you

eliminate duplicate sets of data that slow down the quote process for faster quotes. Neither of the previous examples is showstoppers that do not allow us to build the part, but they do take additional edit time, and if discrepancies exist, address them before fabrication.

Quick Tips

Lastly, here are a few items you should know about that can increase manufacturing costs:

1. Minimize blind vias when they are not needed based on part real estate/ interconnects, because they add approximately eight hours to manufacture time
2. Minimize the number of drill sizes you use and combine those within 1 or 2 mils of one another to save costs
3. If a part is conducive to score, set it up as a score instead of a tab rout because tab routs add additional time and drills for the perforation holes
4. Avoid the use of minimum radius areas where two different rout sizes are needed because it increases the cost
5. Avoid using multiple 0.001" draws on silkscreens because this exponentially increases the data size and takes longer through computer-aided manufacturing (CAM)

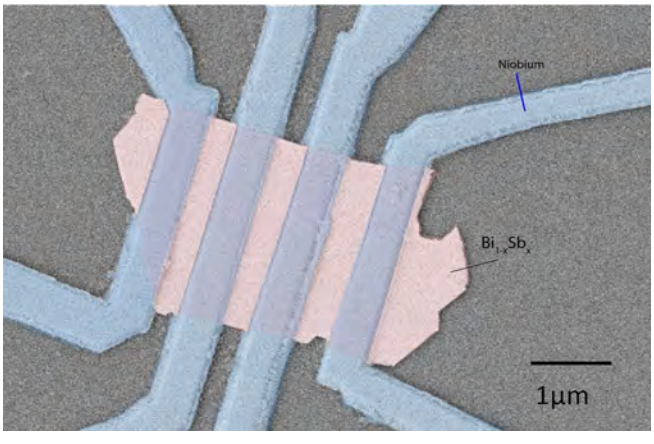
Conclusion

It is important to make sure any drawing notes address customers' reliability concerns in a manner that is clear to the fabricator and minimizes any time lost due to note clarifications or the absence of notes. **DESIGN007**

Mark Thompson is in engineering support at Prototron Circuits. To read past columns or contact Thompson, click here. To download your copy of Thompson's eBook, *The Printed Circuit Designer's Guide to… Producing the Perfect Data Package,* click here.

Superconducting at the Speed of Light

Sightings of Majorana modes are rare and have up to now always involved states at the edge of special, topological materials. As reported in the October issue of "Nature Materials," a new discovery shows that the bulk electronic states of a three-dimensional Dirac semimetal can also play host to topological superconductivity and the related Majorana zero-modes. As these states are protected by fundamental symmetries, their discovery on the inside of a crystal, hidden from the disturbing influences of the environment, is a valuable next step towards their application in topological quantum computation.



Spotting Topological Superconductivity

In a new development, researchers from the universities of Twente and Amsterdam, as part of a Dutch national research programme into so-called topological insulators, have combined forces to show that inside a tuned crystal of bismuth hide the Majorana modes signaling topological superconductivity.

While it may not be found in your kitchen cupboard at home, the heavy atoms of bismuth–in the form of pure crystals–have served as a test set-up for research into the behavior of electrons in a solid for almost a hundred years. For example, it was in bismuth that it was discovered that the electrical resistance of a material can change or even oscillate by applying or changing a magnetic field, a phenomenon which has grown into an indispensable tool in modern materials research.

(Source: University of Amsterdam)

At GreenSource, Lean and Green Starts on the Front End

Feature interview by Andy Shaughnessy
I-CONNECT007

Whelen Engineering's board shop, GreenSource Fabrication, is set to go commercial at the end of the year. But GreenSource Vice President Alex Stepinski has set his sights high from the start.

The Charlestown, New Hampshire, facility may be the board shop of the future. GreenSource is the first new captive shop in America in decades and one of the first waste-free board shops as well. It's almost a "no-touch" operation. The CAM engineers all work remotely, and they can launch a job without ever entering the facility.

I spoke with JanNell Taylor and Andy Schilloff, who work at the CAM office in New York. We discussed what it's like working for a company that plays by its own rules, and what the front-end engineers are doing to get ready for the day that GreenSource officially goes commercial.

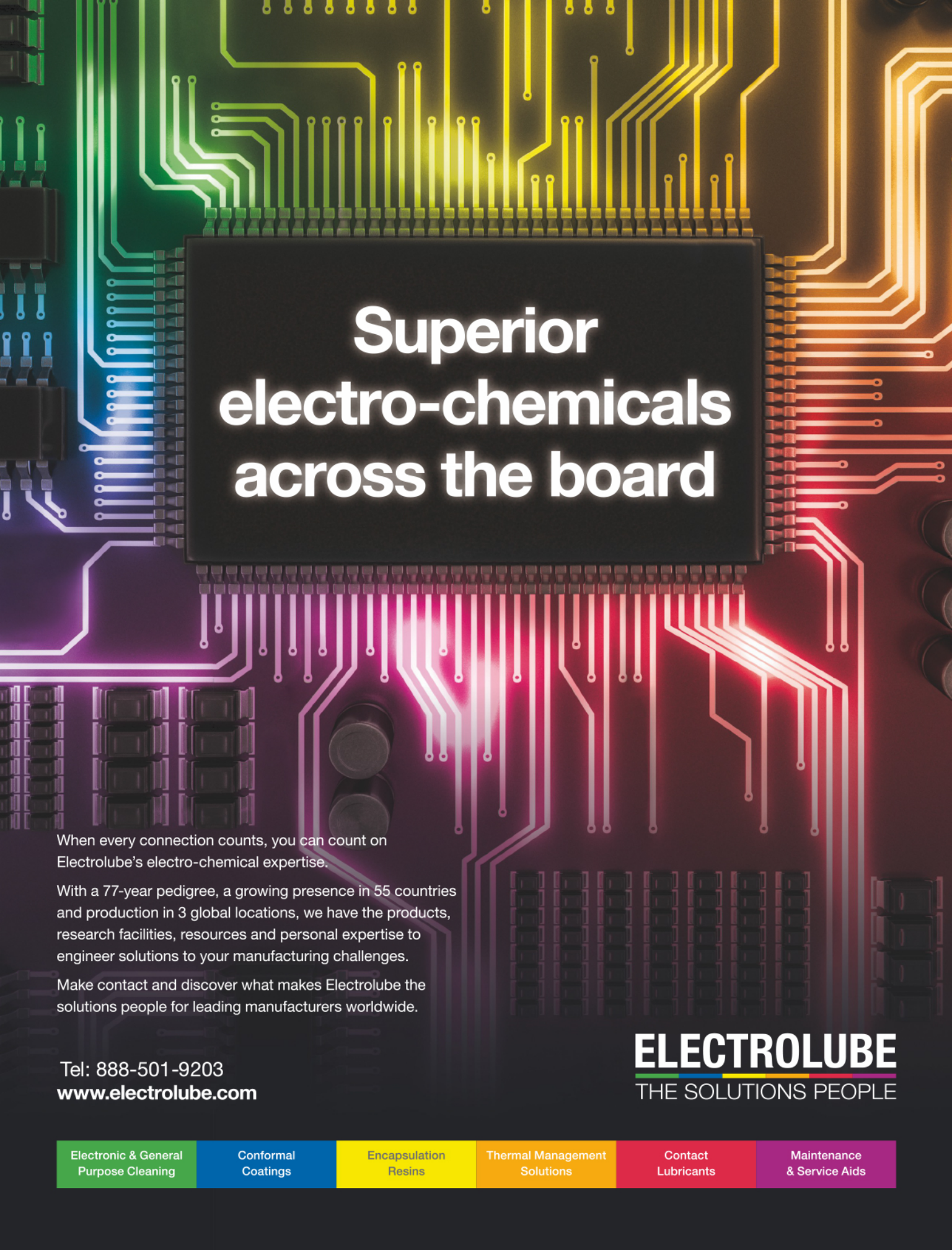
Andy Shaughnessy: JanNell, can you and Andy give us a little background about yourselves?

JanNell Taylor: Sure. I am currently the global product engineering manager for GreenSource Fabrication. I've been in the PCB industry since 1972. My last employer was Sanmina, and I was there for almost 20 years. I was the front-end engineering manager for the past seven years I spent there.

Shaughnessy: Did you knew Alex Stepinski when you were with Sanmina?

Taylor: I actually worked for Alex. That's how I was brought into this project when he first opened Whelen.

Andy Schilloff: I also have prior experience working with Alex at the new product introduction (NPI) group at Sanmina a little over 10 years ago.



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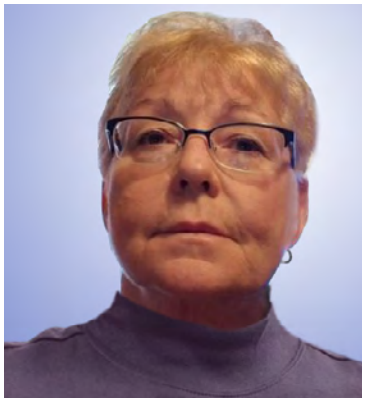
Taylor: Andy and I met while we were working at Sanmina. Andy worked in the NPI group, and I was in front-end engineering. Andy also worked at Sanmina in other positions, including in the front-end for a while.

Schilloff: I have experienced both process and product engineering over a long period of time, which helped me be effective in the NPI group. I've also had experience working for i3 Electronics most recently for a little over two and a half years, and Alex has been building up the crew here to move forward with everything that's happening at GreenSource, and he asked me to come on board. It was definitely the thing to do.



JanNell Taylor

Taylor: In this office, we have eight CAM and product engineering personnel. There is also a customer service rep and sales manager located here. We have three people in Phoenix, and we're currently adding three more. We're also going to be adding another person to the New York office. We'll have 15 total CAM product engineer personnel working remotely.

Shaughnessy: Andy, what's your title?

Schilloff: I'm the lead product engineer, so I deal more with the customer stuff and NPI—things that we haven't come across yet until our capabilities are well established. I'm also a principal engineer. Capability-wise, I'm a good interface between process engineering and the plant by enabling people who work remotely to get the data to where it needs to be. Alex has talked about turn times being much less than what's standard at i3 Electronics, for example, where it might take 10 weeks to build a part. We're going to do it in three weeks, so a part of that has to be an efficient front end, which will be a challenge.

Shaughnessy: Where are you located now?

Taylor: Owego, New York.

Shaughnessy: Sure, near Sanmina. So right now, you all haven't gone commercial yet officially, so primarily what you're doing is in-house captive work, the Whelen work.

Taylor: Correct. We're setting up for the commercial work.

Shaughnessy: What are you doing to get ready for this?

Taylor: We purchased all new software, so we've been busy for the last year configuring our CAM and engineering software. We went to Ucamco for CAM software, and we've spent this year configuring that. We use a system called Bacon from Bacon Software, which is going to be our enterprise resource planning (ERP) system. It is also our engineering system for travelers, process loads, etc. We will not have any paper travelers. It will all be built on barcode readers, and I believe there are 82 different barcode readers. Every barcode reader will equate to an operation on the traveler.

Shaughnessy: We took the tour with Alex, he pointed out all these barcode readers. You'll all be able to trigger a job from off-site without touching the board, right?

Taylor: Yes, it's all remote. All the data is stored at the plant, not off-site. We physically log in to the plant to work.

Shaughnessy: Wow. Are any other companies following this model with CAM people working off-site?

Taylor: When we all worked at Sanmina, we did have remote tooling. We had 11 people in Phoenix at that time who worked remotely for four or five years until they closed it down. We spent a lot of effort making that work, and

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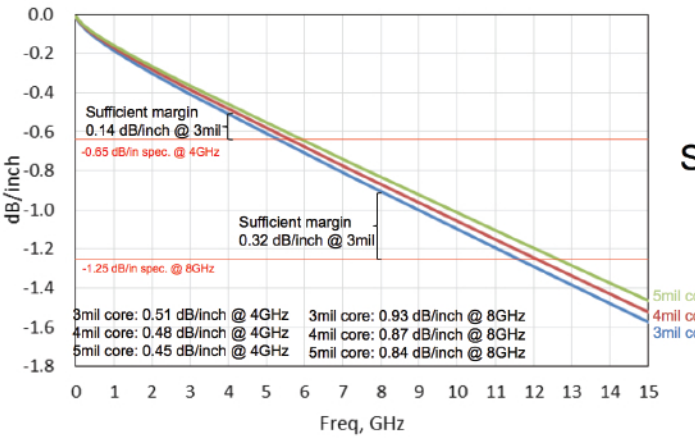
Items	Methods	IT-170GRA1
Tg (℃)	DSC	180
T-288 (w/ 1 Oz Cu, min)	TMA	60+
Td-5%(℃)	TGA 5% loss	380
CTE (%), 50-260℃	TMA	2.4
Peel strength (lb/inch)	1 oz	7.0
Water absorption	D-24/23	0.1
Dk: 2-10 GHz	Bereskin	3.96 – 3.99
Df: 2-10 GHz	Bereskin	0.0073 - 0.0075

IT-170GRA1 Insertion Loss



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we were able to bring those lessons with us to start this group.

When I first got here, I worked alone. We brought in one software engineer, and then another, so we did the tooling and scripted things to make operations more efficient. We were very remote. We have brought in experienced help to be a part of this project, so there are some very talented folks here; we know what to do to make it happen.

Shaughnessy: As far as the data goes, will you accept Gerber and ODB++?

Taylor: Yes, we're capable of both. My preference would be Gerber. If we were using InCAM or Genesis, my preference would be ODB. Now that we've migrated to another CAM software, the preference is definitely Gerber, but we're able to accept either. The problem with taking ODB data from other customers is that it works very well if you have your set-up in-house between your designers and CAM. But when you're receiving ODB from the outside, the attributes are different. You don't re-strip all the attributes from the incoming data, and then it collides with the scripting and automation that you have in yours. Typically, what I've seen is that we receive ODB data and have to strip it down because we didn't use any of the attributes that the design engineers did. It defeats the whole purpose of having the self-contained job.

Andy Schilloff

Shaughnessy: Have you had any new designs come in yet, non-Whelen stuff? I know you're not officially commercial yet.

Taylor: We do have data that we've been performing DFMs on. We're quoting a few test vehicles that we've been building.

Schilloff: We're preparing to release our first HDI films, and working out a lot of the kinks, so that's getting ready to happen shortly.

Taylor: Any time new equipment comes in, or there's something new going on at the plant, we make trips out there. We rotate, go as a group, or a few of us go to check out the equipment and try to find out what they will need from CAM and engineering.

Shaughnessy: I talked to a lot of CAM people, and they say that one of their biggest jobs is educating new customers on data packages.

Taylor: Yes, you must work with your customers to try to streamline your profits. It's always been that way working with customers, trying to get data packages so you can drop them in and not have anything be held up. That will continue for sure.

Shaughnessy: And I heard you all are going to start doing RF?

Taylor: Yes, we are.

Schilloff: A military customer has approached us. Part of that deal is to see how well we do with their constraints, and also for them to get official data and different materials sets, so we're looking at doing that soon.

Shaughnessy: During our tour, we noticed that you have a group of people under 30, and you also have 30-year veterans. It seems like you have a good mix of age groups working at GreenSource.

Taylor: That's the goal here with what we're doing off-site: to hire younger people to pass on knowledge. We started with two, and that's working great. They pick things up quickly and are doing a great job, and we will eventually add more.

Shaughnessy: I understand GreenSource is planning to cross-train the engineers. I know there's a father-son team and some couples are working there, and the cross-training means

that they can take time off to go on vacations together.

Taylor: We're doing that here as well in the front end so that we have the flexibility to rotate based on the demands of our schedule. We don't want to be stuck where we only have two product engineers and four CAMmers, so there's cross-training going on, and everybody here will be capable of performing every task in tooling.

Shaughnessy: You're writing the textbook as you go.

Taylor: We'll see. I'd like to read that book another year.

Shaughnessy: It sounds like an exciting place to work. We were laughing about how usually when we visit a board shop, everybody has a hang-dog look. Everyone at GreenSource was happy to be there.

Taylor: I cannot say enough good things about Whelen and GreenSource. They're the best employer I've ever had. They treat us very well. It's challenging, and it can be frustrating, but finding solutions to the challenges is what keeps me motivated. If you came in every day and did the same thing, it would get very boring. We do not have boring days here.

Shaughnessy: I know you all will be busy when you open the doors in a few months, so it's an exciting time for you. Thanks for taking the time to talk with me.

Taylor: Thank you for sharing our story.

Schilloff: You are welcome at GreenSource any time. **DESIGN007**

Novel Topological Insulator

Topological insulators are materials with very special properties. They conduct electricity or light particles on their surface or edges only but not on the inside. This unusual behaviour could eventually lead to technical innovations, which is why topological insulators have been the subject of intense global research for several years.

Physicists of Julius-Maximilians-Universität Würzburg (JMU) in Bavaria, Germany now report their discovery in the journal "Nature." For the first time, the team has successfully built a topological insulator operating with both light and electronic excitations simultaneously, called an "exciton-polariton topological insulator."

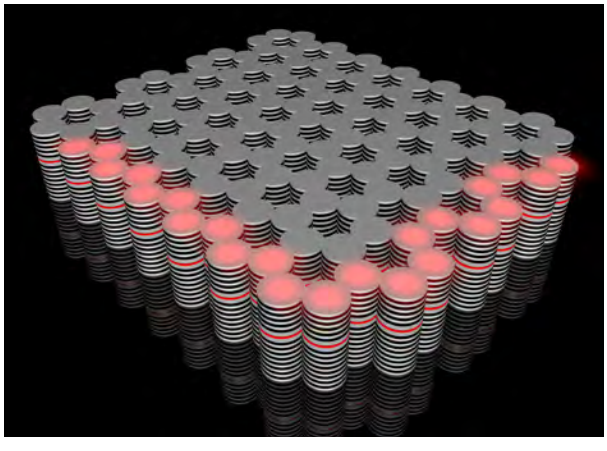
Dr. Sebastian Klembt, group leader at Höfling's chair, said that the topological insulator was built on a microchip and basically consists of the gallium arsenide semiconductor compound. It has a honeycomb structure and is made up of many small pillars, each two micrometres (two millionths of a metre) in diameter.

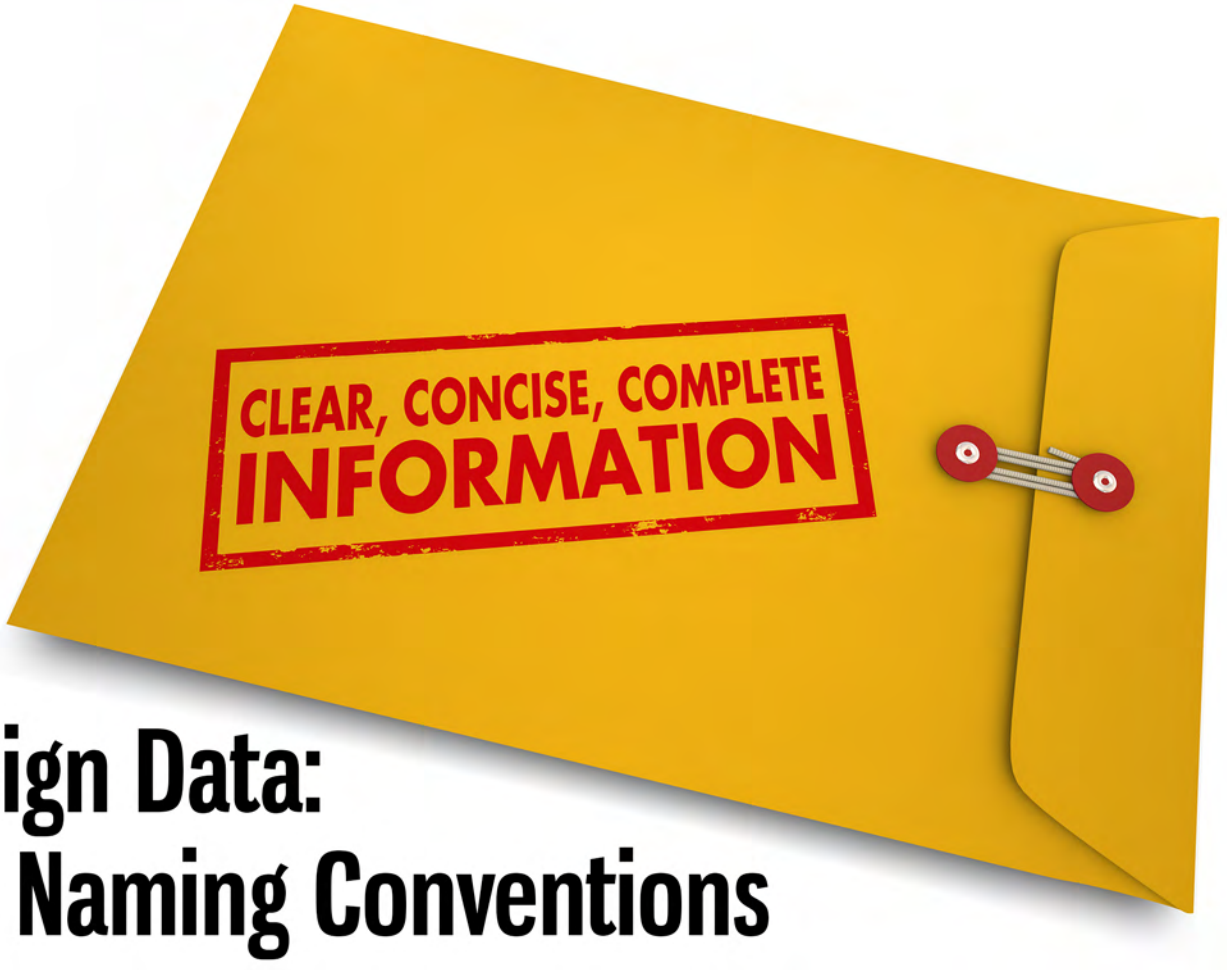
Propagation Direction Can be Controlled

When exciting this microstructure with laser light, light-matter particles form inside it, exclusively at the edges. The particles then travel along the edges and around the corners with relatively low loss.

It is a sophisticated systems which works in application-oriented dimensions, on a microchip, and in which light can be controlled. Usually, this is not so easy to accomplish: Pure light particles have no electric charge and therefore cannot be readily controlled with electric or magnetic fields. The new topological insulator, in contrast, is capable of doing this by "sending light around the corner," in a manner of speaking.

(Source: University of Wurzburg)





Design Data: File Naming Conventions

Feature by Kelly Dack, CID+, CIT
EPTAC CORPORATION

Have you ever Googled your name? Using the internet, I found out there are not many folks named Kelly Dack in the world, though I was surprised to find out there are a few scattered here and there. Now, imagine my shock if I were to be denied a loan, referred to as "Ms. Dack," or passed up for a job opportunity because an auditor used the incorrect profile data from one of the other Kelly Dacks out there during my data verification process.

I have found that when searching for myself on the internet (come on, you do it too), I achieve better results by being more specific in my search criteria. For instance, simply adding "PCB" after my name helps to narrow the search criteria by being descriptive enough to show Kelly Dack the PCB designer and almost anything I am connected to within the PCB industry.

I recently read that up to 90% of the manufacturing data for the electronic design industry's PCBs is still supplied in the non-intelligent Gerber data format. Regardless of the percentage, I know that the EMS provider I work for sees a lot of Gerber data from our customers. And we procure a lot of quality PCBs from our suppliers using Gerber data (unless we can't). Sometimes information on an entire layer or other manufacturing files are missing. Again, Gerber data is not intelligent. It is graphic information only, and if measures aren't taken by the designer to give us clues regarding how the artwork is configured, we must stop, ask questions, and seek clarification, which takes valuable time.

Working for an EMS provider, I am often asked to make sense of customers' PCB design data packages that must be audited for completeness and manufacturability. Quite often, EMS operations receive data to produce a PCB design and begin the auditing process, only to be called off due to customer changes. Sometimes the data is incomplete, or it is missing one or more of the data files required to fabricate the PCB at the supplier. There are also

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occasions where a customer has sent files that were supposed to be the updated version but were not changed at all.

All suppliers of PCBs, including assembly services suppliers, make great efforts to verify that the data they are using to build the product for a customer is the latest up-to-date version. Every manufacturing process is tied to an internal product control number and revision. In production environments, the material does not move forward unless it has been checked, verified, and inspected to the revision control process in place. But what happens when the customer design data is not identified?

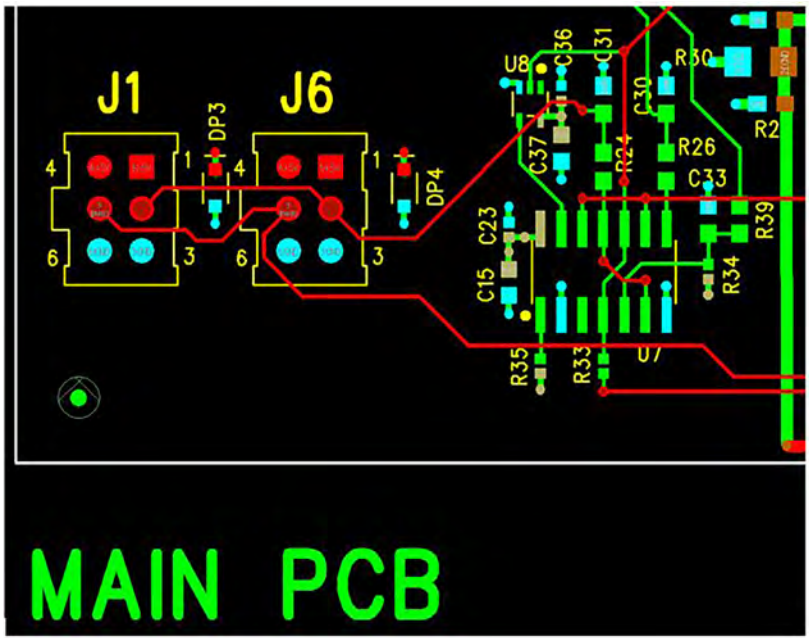


Figure 1: Many PCB designs are named "MAIN_PCB."

It is a fact that designing and engineering PCBs requires changes. But the tragedy is that without organization and control, a quickly introduced change using data that is not clearly identified can wreak havoc on a supplier's manufacturing control systems. All too often in the rush to market a new PCB design, a customer's design layout template is used without the customer editing the file names to be appropriately descriptive.

Here's an extreme example. Many designers send out data files for a "MAIN_PCB" design to suppliers (Figure 1). Within the data archive for this generically named design, the files may also lack descriptive naming attributes. To make a point, let's examine the data archive for this four-layer, single-sided assembly design (Figure 2). As a manufacturing stakeholder, could you quickly pick out the file that reflects the top-side legend (silkscreen)? How about the top-side solder resist artwork? Not a chance without importing the files into a manufacturing file viewer (Gerber) and putting the pieces of the manufacturing puzzle together.

In this case, the only file providing a clue to its functionality is the .NCD file. The supplier will probably assume that this is an NC Drill file. The other files will need further investigation. But even after assimilating the files into a viewer, determining the functional purpose of the files without any descriptive help is a challenge. Let's use the viewer to plunge inside the design files to see if we can determine how to use this data.

Is the view of the MAIN_PCB_1.pho file in Figure 3 the top-side artwork or the bottom side? How would your fabrication stakeholder know? Next, let's take a look at another file in the archive, the MAIN_PCB_6.pho file. It appears to be a power plane. Shall we assume that it resides on an inner layer (Figure 4)? If so, which one? There are two inner layers. I'm getting a headache. This is impossible!

Name	Date modified	Type	Size
MAIN_PCB_1.PHO	5/30/2014 11:53 AM	CAM350 Pho File	146 KB
MAIN_PCB_2.PHO	5/30/2014 11:53 AM	CAM350 Pho File	206 KB
MAIN_PCB_3.PHO	5/30/2014 11:53 AM	CAM350 Pho File	150 KB
MAIN_PCB_4.PHO	5/30/2014 11:53 AM	CAM350 Pho File	147 KB
MAIN_PCB_5.PHO	5/30/2014 11:53 AM	CAM350 Pho File	145 KB
MAIN_PCB_6.PHO	5/30/2014 11:53 AM	CAM350 Pho File	151 KB
MAIN_PCB_7.PHO	5/30/2014 11:53 AM	CAM350 Pho File	149 KB
MAIN_PCB_8.NCD	5/30/2014 11:53 AM	NCD File	1 KB

Figure 2: Name your files in a way that lets the fabricator know your intent.

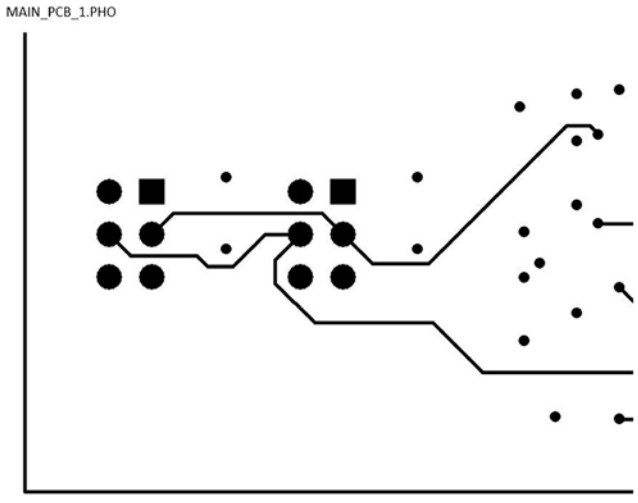


Figure 3: Be sure to label your artwork "top" and "bottom."

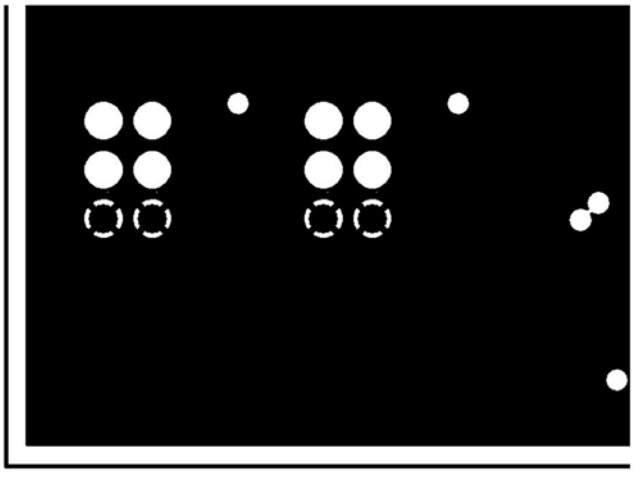


Figure 4: This MAIN_PCB_6.pho file appears to show a power plane. Is it on an inner layer? Which one?

Lord, help our manufacturing stakeholders when the new, non-descriptive revision to the "MAIN_PCB" design is subsequently released by the customer and sent to the supplier for processing. Figure 5 shows the new file, or maybe it is the old file by mistake. How can we know? Both files are named MAIN_PCB_6.pho. Is there a difference? Some may rely on the file's date stamp, but this can be very unreliable. PCB designers, please help. Can you tell us which file is the latest and if it is identical? Have any changes been made?

Without going any further, I think that all PCB designer readers can see the point. Good graphic data without descriptive attributes is confusing and down-right dangerous. There

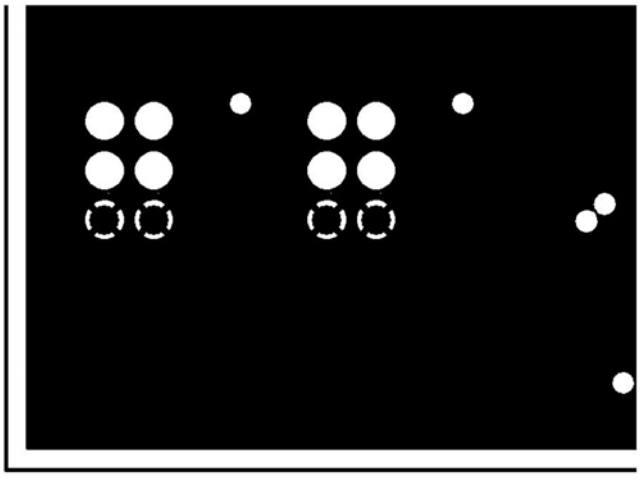


Figure 5: This MAIN_PCB_6.pho file may be the new file. Or is it the old one?

is not an EMS stakeholder alive who would proceed to manufacturing without concrete answers to the many questions that result from trying to process these non-descriptive files.

One thing PCB designers can do to help suppliers in the area of configuration auditing, control, and processing is to add specificity to the data file names when outputting and archiving the PCB data package.

Let's examine what descriptive information can be added to this PCB design data package to make it easier on the stakeholders' configuration auditing and control process:

1. Consider adding a graphic title block to the design database that can be output along with each artwork layer. This is where many informational blanks can be identified, including a descriptive name, part number, revision, date, responsible designer, and EE contact information. The title block can be placed within the design to print on all layers, and edited only once per revision (Figure 6).

PCB, MAIN, MICRO-COMBOBULATOR			
PART NO.: 424242-42	REV: A	DATE: 2018-JAN-01	
DESIGNER: JENNY FINELINE (800) 867-5309		ENGINEER: SPARKY SMITH	

Figure 6: Adding a graphic title block to the design database for output with each artwork layer is a good idea.

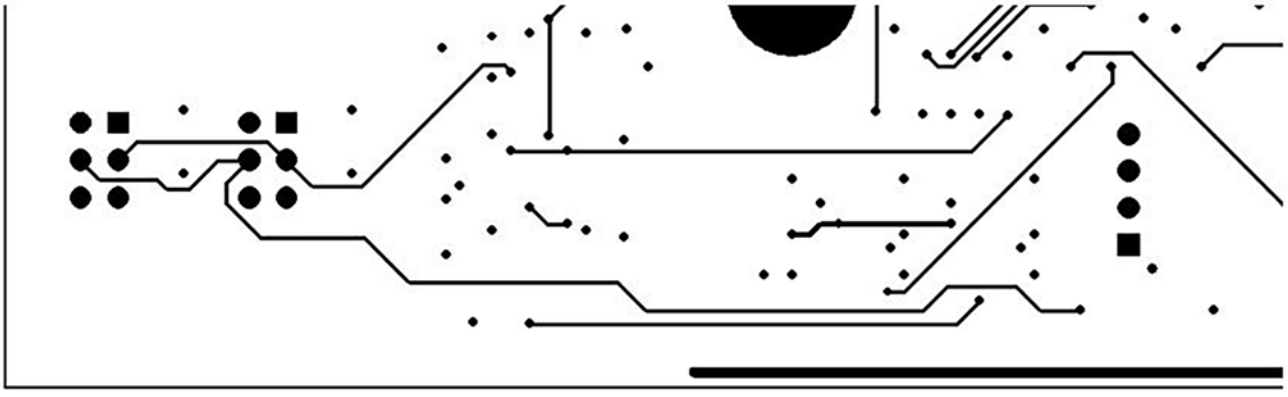
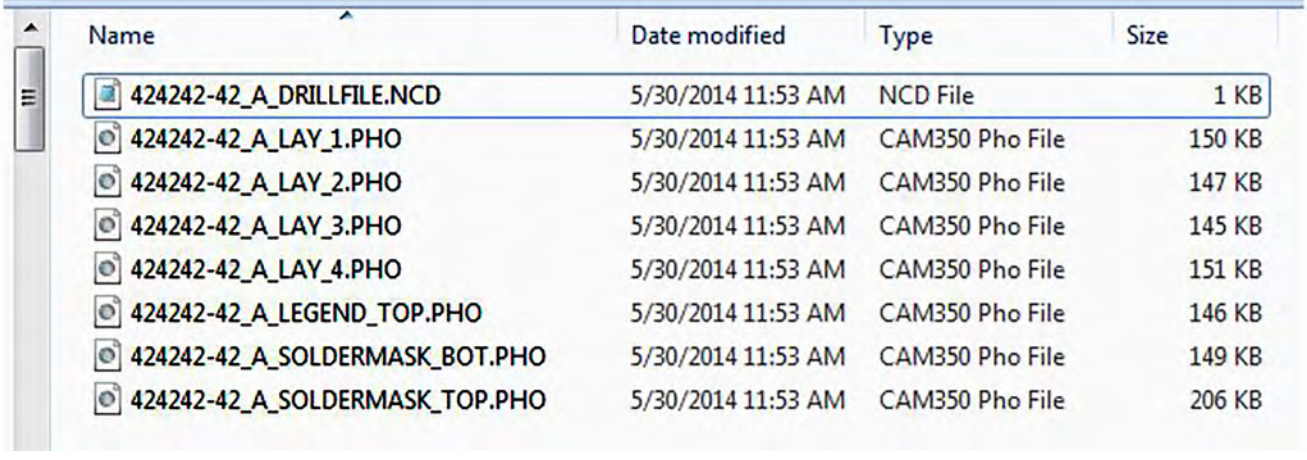


Figure 7: Descriptive nomenclature for each artwork layer helps identify its function.



Name	Date modified	Type	Size
424242-42_A_DRILLFILE.NCD	5/30/2014 11:53 AM	NCD File	1 KB
424242-42_A_LAY_1.PHO	5/30/2014 11:53 AM	CAM350 Pho File	150 KB
424242-42_A_LAY_2.PHO	5/30/2014 11:53 AM	CAM350 Pho File	147 KB
424242-42_A_LAY_3.PHO	5/30/2014 11:53 AM	CAM350 Pho File	145 KB
424242-42_A_LAY_4.PHO	5/30/2014 11:53 AM	CAM350 Pho File	151 KB
424242-42_A_LEGEND_TOP.PHO	5/30/2014 11:53 AM	CAM350 Pho File	146 KB
424242-42_A_SOLDERMASK_BOT.PHO	5/30/2014 11:53 AM	CAM350 Pho File	149 KB
424242-42_A_SOLDERMASK_TOP.PHO	5/30/2014 11:53 AM	CAM350 Pho File	206 KB

Figure 8: Data file names should correspond to the descriptive list on each layer of artwork.

2. Next, consider adding descriptive nomenclature to each specific artwork layer to identify its function, and graphically link it to its associated data file (Figure 7). Upon viewing, there is no question that this artwork represents the bottom-side signal layer as revision A of part number 424242-42 derived from the 424242-42_A_LAY_4.PHO data file.

3. Lastly, name your data files to correspond to the descriptive list on each layer of artwork. With a naming format, files can be audited for completeness and moved to CAM without previewing and deciphering beforehand (Figure 8).

Adopting this simple, but descriptive, naming methodology for any manufacturing design data package will go a long way in helping your PCB manufacturing stakeholders to serve you better. **DESIGN007**

Kelly Dack provides PCB design and manufacturing engineering services for a dynamic EMS provider in the Pacific Northwest. Additionally, he serves on the executive staff of the IPC Designers Council and is employed by EPTAC Corporation as a CID instructor. To contact Kelly, click here.

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I-Connect007
GOOD FOR THE INDUSTRY

Digital Specs for Automated Manufacturing: Find the Missing Link!

PCB Norsemen

Feature Column by Jan Pedersen, ELMATICA

Automation and connected smart factories are the new manufacturing trend. Industry 4.0 and the Internet of Things (IoT) continue to enter PCB manufacturing. However, if we continue down the same path with specifications and requirements written on electronic papers and unintelligent production files, human interpretation is still crucial to avoid mistakes. CircuitData could solve this problem because having one language for automated smart factories is the future!

With the I-Connect007 article about the grand opening of the Unimicron factory in Germany fresh in mind, I also had the opportunity to visit it in June for the 50th anniversary of EIPC [1]. I have seen hundreds of PCB factories virtually, but this was my first time seeing a smart PCB factory in person. The tour showed me how far we have come if we use all available tools. Further, it reminded me of the missing links that disable a true digital chain of information needed to utilize systems in smart factories, such as Unimicron and Whelen Engineering's GreenSource Fabrication in the United States.

Automating PCB Production

Today, most processes in a smart PCB factory can be automated and monitored. Continued innovation is accelerating the Industry 4.0 transformation of the PCB factory. We strive to analyze and share time-production data to be able to understand and act immediately. When I have visited and audited PCB factories lately, I have seen a growing trend—even with more traditional factories—to have connected equipment, such as online and real-time process monitoring, remote production, and maintenance alarms [2].

Observing this, it is puzzling to me that we still feed factories with specifications and requirements written on electronic papers and unintelligent production files. Experts in the indus-

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try continue to claim that a fabrication drawing printed on A3 paper is vital to understand customers' requirements. Corporate requirements—even the measurable parts—are given in an analog way into an increasingly digital environment. In almost every issue of I-Connect007's magazines and other publications, we read about how Industry 4.0 and smart manufacturing are growing and changing the production environment.

However, the missing link is how we transfer and communicate fabrication data between the product owner and the PCB factory. To avoid ambiguous specifications, we need a common language to communicate the specification and use the same terms in all parts of the transmission chain.

To avoid ambiguous specifications, we need a common language to communicate the specification and use the same terms in all parts of the transmission chain.

CircuitData and IPC-2581

CircuitData is the only language available today to digitally communicate a complete and accurate specification with all measurable corporate requirements and standards included, such as the IPC-6011 series [3]. CircuitData is an open source language for communicating PCB article specifications, corporate requirement profiles, engineering change notes, and engineering questions. It consists of a computer-readable file with tools to easily link with your existing software. The file can be updated in real-time from designers to OEMs, EMS providers, brokers, and the PCB factory. One file handles it all with no missing information or misinterpretations.

We also need an intelligent way of presenting the production data. IPC-2581 is one of the systems that communicates the electronic design into the digital environment of the smart PCB factory with sufficient intelligence [4]. IPC-2581 is a generic standard for PCB and assembly manufacturing description data and transfer methodology. Developed in 2004 by IPC, IPC-2581 is used for transmitting information between a PCB designer and a manufacturing or assembly facility. For nearly every step in the industrial process flow, IPC-2581 offers a standard to help companies ensure superior manufacturability, quality, reliability, and consistency in electronics assemblies built for their products.

Garbage In, Garbage Out

With tools like CircuitData and IPC-2581, we can secure correct description data, provide sufficient file intelligence, and enable a full digital data transfer to give value to the smart PCB factory. Without these tools, we retype specifications and accept human errors just like we did decades ago. By using a less intelligent transfer methodology than IPC-2581, we accept incomplete information. Garbage in, garbage out! A chain is no stronger than its weakest link.

Data for the future smart PCB factory requires the same digital quality for transfer between the designer and the smart PCB factory. Automated manufacturing requires digital specifications. Nothing less is acceptable. **DESIGN007**

References

1. *Unimicron Germany Rises from the Ashes with New Smart Factory* by Pete Starkey (I-Connect007) and Michael Weinhold (EIPC), PCB007 online, April 30, 2018.

2. *The evolution of Industry 4.0, through the eyes of the PCB manufacturer* by Shavi Spinzi, Evaluation Engineering online, June 22, 2017.

3. circuitdata.org

4. ipc2581.com

Jan Pedersen is senior technical advisor at Elmatica. To read past columns or contact Pederson, click here.

MEPTEC2018

HETEROGENEOUS INTEGRATION: THE PATH FORWARD

REALIZING THE COST AND PERFORMANCE BENEFITS

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KEYNOTE SPEAKER

Heterogeneous Integration Roadmap and SiP

William "Bill" Chen, ASE Fellow and Senior Technical Advisor, ASE Group

KEYNOTE SPEAKER

Disruption is Coming: Adapt, Change or Be Left Behind

Keith Felton, Product Marketing – IC Packaging, Mentor Graphics Board Systems Division

KEYNOTE SPEAKER

Heterogeneous Integration: Is it Ready for Changing the Packaging Landscape?

Risto Puhakken, President, VLSI

MEPTEC continues to cover leading-edge topics in semiconductor packaging with its Fall 2018 Symposium ***"Heterogeneous Integration: The Path Forward."*** Industry leaders will present the latest updates on technical and business issues related to integration of different types of semiconductor devices. This field has been identified as the next critical area for the semiconductor industry to continue to advance, as progress via Moore's Law scaling becomes increasingly cost-prohibitive or prevented by insurmountable technical challenges. With progress in many areas, cost and performance benefits are finally being realized, and previously impossible combinations of devices are now possible.

Don't miss this unique opportunity to get up to speed at MEPTEC's symposium "Heterogeneous Integration: The Path Forward" on December 5, 2018 in Milpitas, CA.

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PCB007 Highlights

EPTE Newsletter: New Materials for Wearable Electronics ▶

Technology continues to evolve, and wearable electronics are the focal point for many new concepts. The next generation of wearable products for the consumer electronics industry will create a new market with nothing but upside for manufacturers and suppliers.

Flex Talk: Mina–RFID, LED and What Else? ▶

"The science of today is the technology of tomorrow." This Edward Teller quote is an apt description of the Mina product. This advanced surface treatment recently developed to enable low-temperature soldering to aluminum in the RFID market is finding success in that market and quickly finding a home in other markets—including the LED market—where the incentive is both cost and improved LED performance.

PCB Designers: Perfect Your Data Package with New eBook from Prototron ▶

For PCB designers, producing a comprehensive data package is crucial. If even one important file is missing or output incorrectly, it can cause major delays and potentially ruin the experience for every stakeholder. Learn how to perfect your data package with I-Connect007's most recent title: *The Printed Circuit Designer's Guide to… Producing the Perfect Data Package.*

Rogers to Highlight Latest Circuit Materials and Share Expertise at EDI CON USA 2018 ▶

Rogers Corporation will share its experience and expertise on circuit materials technologies at the 2018 Electronic Design Innovation Conference (EDI CON USA 2018) October 17–18, in the Santa Clara Convention Center (Santa Clara, California). EDI CON USA 2018 is entering its third year of serving the high-frequency RF/microwave design engineering community.

Standard of Excellence: Working for the Future–Partnering with PCB Vendors on Innovative Technology ▶

The true test of the vendor-customer relationship comes when you need innovative PCBs—boards that are not easily found in the common marketplace and are so technologically advanced that they require your designers and suppliers to work together to go where neither has before.

Alun Morgan Named Technology Ambassador for Ventec ▶

Ventec International Group Co., Ltd., announced that Alun Morgan, chairman of the EIPC, has been named technology ambassador for Ventec International Group.

American Standard Circuits Launches Fusion Bonding for RF Boards ▶

American Standard Circuits is now offering fusion bonding of PTFE-based materials. Fusion bonding of PTFE-based materials involves using high temperatures (≥700°F/371°C) to bond PTFE directly to the copper circuitry and surrounding PTFE.

Building a Better Board: It Always Comes Back to Communication ▶

For our experts meeting on the August's theme of reliability, we reached out to Colonial Circuits and asked them to participate in a conference call with our I-Connect007 editorial team consisting of Dan Feinberg, Andy Shaughnessy, Patty Goldman, and Happy Holden. Joining the call from Colonial Circuits was Mark Osborn, president and CEO, Kevin Knapp, quality manager, and Rodney Krick, manufacturing manager.

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New Landing Design to Reduce Thermal Pad Failures

Connect the Dots

New Column by Bob Tise and Dave Baker, SUNSTONE CIRCUITS

You've finally finished your design. All the traces are correct, and the integrated circuit (IC) landings are to the manufacturer's specifications. A short run of test boards performs perfectly. For best results, you select a reputable domestic board house for production and a quality assembly shop to do the soldering. When the finished boards arrive, everything looks great. You're in high spirits and congratulate yourself on a job well done.

Then the reports start coming in:

- "My board worked for a week but won't boot up now. I need a replacement."
- "We're seeing a high percentage of failures during quality assurance."
- "My order is dead on arrival. Did you test it before you sent it?"

You've done everything by the book and passed every preliminary test, but things are still going wrong. What's happening here?

We found ourselves in a similar situation while working on a client project. The failure rates were only a small percentage, but in volume, those costs quickly run into thousands of dollars. We poured over every possibility and traced the problem down to a single high-power quad flat package IC where the center thermal pad was not being soldered consistently. Nothing was wrong with the board or the soldering process; the default method for soldering heat slugs to boards was just inherently flawed. Looking at the costs and reliability problems, we knew we had to do better.

After testing a variety of different designs, we found one that was vastly more reliable and

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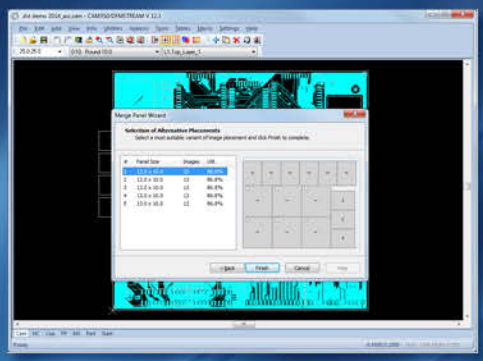

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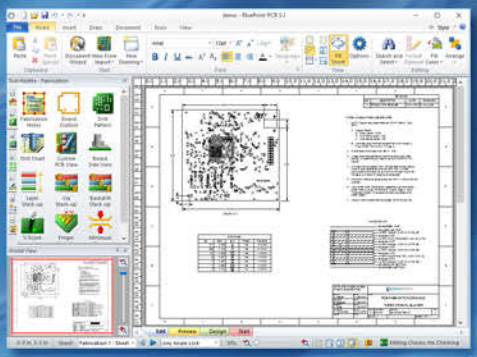

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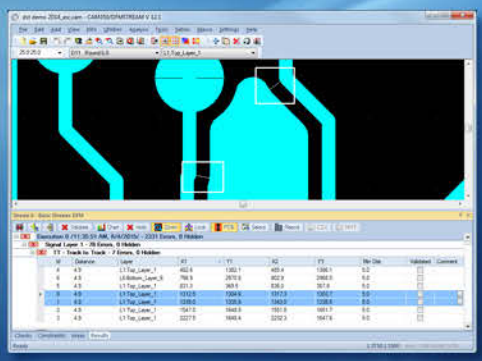

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did not add to the cost of manufacturing. The solution translates well to similar IC packages. We were back up and running again, but what was the problem in the first place?

Problem: Uncontrollable, Unpredictable Solder

At first, we used the standard, manufacturer-recommended method for heat sinking. We placed large copper pads on both sides of the board under the chip, connected them with vias to conduct heat, and applied full solder paste coverage for the best thermal contact. As straightforward and intuitive as the standard approach is, it obviously has some problems.

In this case, the culprit is solder's unpredictable behavior once melted, which puts every board at risk of a poor heat sink connection. We've all seen the result of bad solder connections: Failures in quality assurance or worse—shortened life and failure in the field. The problem is so pervasive you might be tempted to accept it as the unavoidable cost of doing business. But if we look at the causes of the chaos, we can find ways to offset them. There are two main mechanisms that cause these failures: Solder wicking through vias and solder movement under large pads.

Failure 1: Solder Wicking Through Vias

This failure mode is the most obvious. If the landing pad is covered in tiny holes, molten solder can run through them to the back of the board. This leads to less solder connecting the pad and the solder that is in place distributes unevenly. Even worse, the wicking will vary from board to board. Common vias are not precision components, and the amount of copper plated onto them varies. Some may be wider than intended, and others plated partially or fully shut. Identically designed boards that went through the same manufacturing process may now have significantly different thermal responses.

Failure 2: Solder Movement Under Large Pads

Again, we have to consider the unpredictability of solder movement during reflow. If there is not enough solder under the slug or the board is warped, capillary action can pull the solder to one side of the chip. Attempt to correct this by applying more solder, and the chip might float right off the signal pins. Excess solder can overflow the pad and send solder balls out to short or bridge other areas of the board. The varying amount of solder pulled through the vias only exacerbates the problem and hinders attempts to correct for it by adjusting the amount of paste used.

Solution

Fortunately, the solution is as straightforward as the problems themselves. We simply must prevent the solder from wicking through the vias or moving past its area of application. There are two elements to this solution.

First, apply solder mask over the landing pad and open circular "islands" for paste application. If the solder won't behave over a large area, we can break that area up into an array of smaller, better-behaved areas because solder mask restricts the paste to its area of application. While this reduces the amount of solder connecting the chip to the board, it also increases the consistency. The circular solder paste apertures release the solder more reliably than those with sharp corners, which helps prevent loose solder balls.

Second, surround the "islands" with small (~12 mils or smaller) tented vias (covered with solder mask). Removing the vias from the immediate area being soldered and tenting them prevents any stray solder from wicking down to the other side of the board while still providing good thermal transfer to the pads underneath. You should add these vias as close as possible (nearly tangentially) to the islands. The solder mask tenting will block any solder that wicks onto an exposed via due to manufacturing tolerances.

Keep in mind these few key rules when implementing:

- Make sure the pad under the chip is a solid copper plane to spread out the heat
- Use a hexagonal packing pattern for the solder islands to give the heat slug maximum coverage

- The solder mask tents should be the same size as the resist mask opening on these islands and provide 100% coverage. This ensures that adequate solder is present to bond to the chip
- Do not use thermal spokes on any layer of the vias. Thermal spokes will reduce their thermal conductivity
- Vias should be solder mask tented, not plugged or filled. The epoxy in solder mask plugged vias may not cure fully and will tend to expand and erupt if subject to enough heat

Figure 1 shows (a) a top layer—solder mask and paste mask opening; (b) a plated through-hole with no solder mask opening placed very close to, but not tangent with, the solder mask opening; and (c) a copper pad, top layer. Note that the solder mask opening should be greater than or equal to one-half of the thermal area of component body for efficient transfer of heat. Further, all plated through-holes should be vias tied to the same net as copper pour. Vias should not have thermal relief on any layer or have a solder mask opening on the top or bottom layer. Figure 2 shows a different view.

Implementation

The most efficient way to implement this design is to make it part of your package definition, so it is uniformly applied to all similar parts. Unfortunately, many CAD packages do not support the direct addition of vias

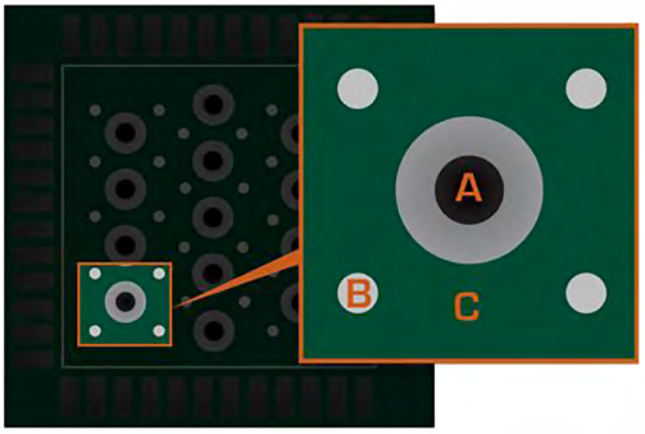

Figure 1: A captive solder pad protected from the wicking effect created by the large diameter via solution.

and copper planes to package designs. An easy workaround is to create square surface mount device (SMD) pads to act as the top and bottom copper sinks, as well as small plated through-hole pads to act as the vias. These can then be set as unconnected pins in your component definition. You may have to create custom paste and solder masks for these pins, but this is usually not too difficult.

Try this design out for your next project, and you will be happy with the results. The benefits of this design speak for itself: Fewer failures and phone calls, a more consistent product, and (of course) a fatter bottom line. DESIGN007


Bob Tise


Dave Baker

Bob Tise and Dave Baker are engineers at Sunstone Circuits.

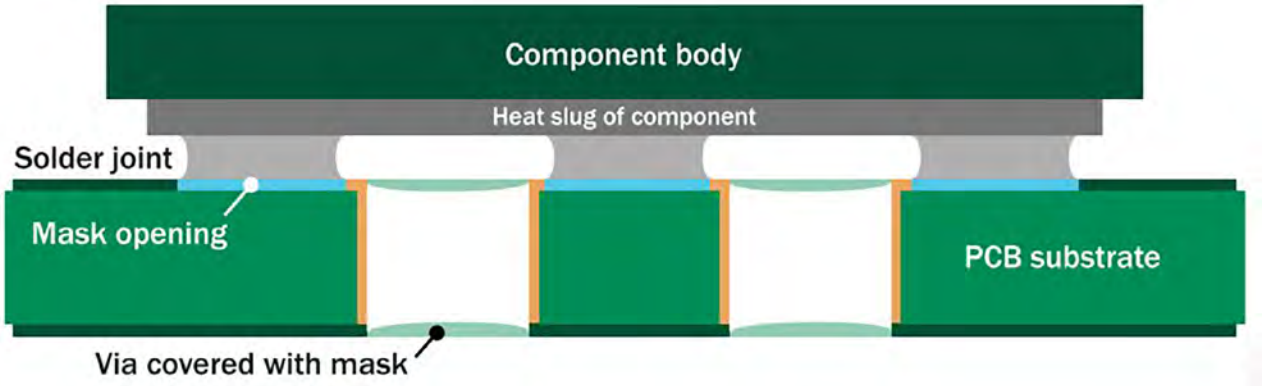

Figure 2: A side view of the board in Figure 1 illustrating placement of joints, mask openings, and vias.

10 Fundamental Rules of High-speed PCB Design, Part 2

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

In last month's column, I introduced the 10 fundamental rules of high-speed PCB design (Figure 1). The first rule was to establish design constraints before commencing the design. This prime strategy sets constraints upfront based on pre-layout analyses or recommendations and guidelines and is integral to the design flow to maintain the established requirements. This month, I will elaborate on the importance of controlling the impedance and floor planning the placement based on connectivity.

II. Control the Impedance: Match the transmission line impedance to the driver and load. Create the stackup and define terminations to match the impedance.

For perfect energy transfer, the impedance of the driver must match the transmission line—assuming there is a high-impedance load. A good transmission line is one that has constant impedance along the entire length of the line, so no mismatches result in reflections.

Digital design typically uses a characteristic impedance of 50–60 ohms. However, this value becomes more critical as the edge rates increase. Different technologies also have specific impedance requirements. For example, Ethernet is 100 ohms, USB is 90 ohms differential, DDR2 memory is 50/100, and DDR3/4 is 40/80 single-ended/differential impedance. Thus, controlling impedance simultaneously on each signal layer with many different technologies can become a challenge. Further, as operating voltages decrease, the associated

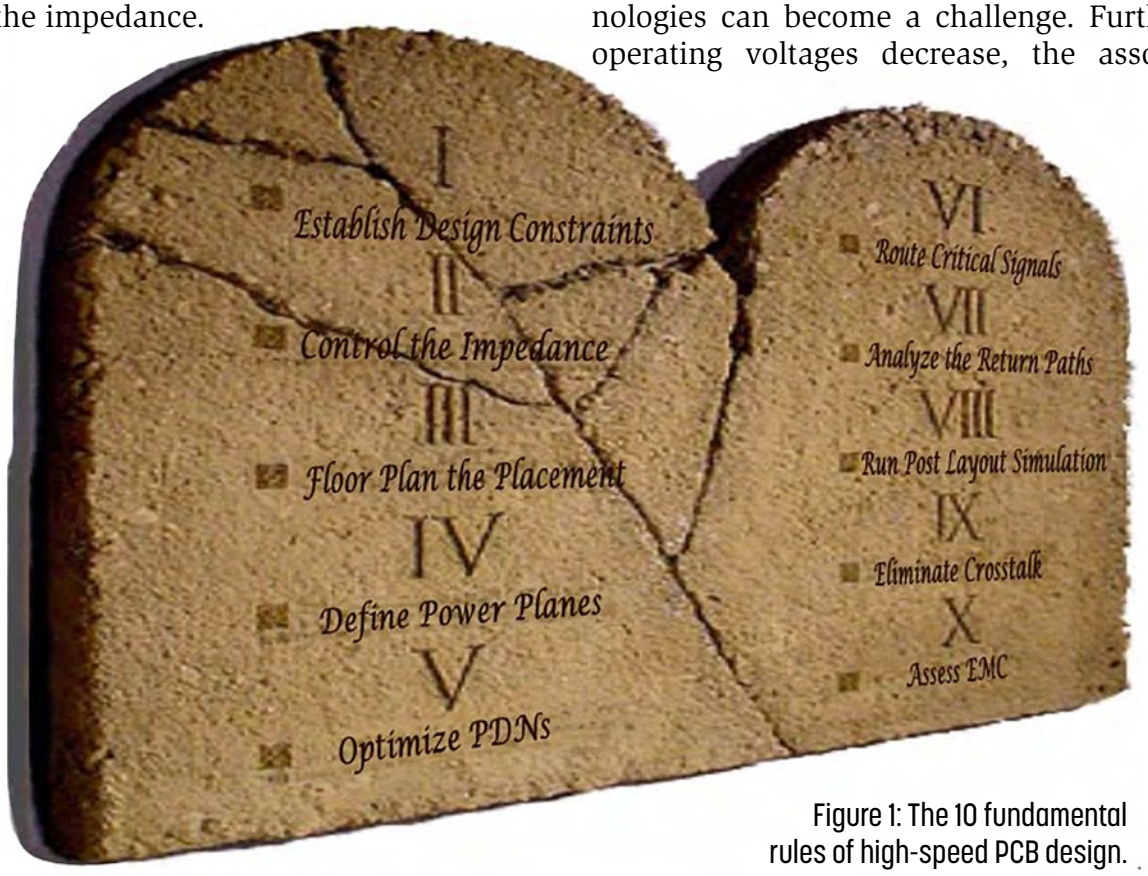

Figure 1: The 10 fundamental rules of high-speed PCB design.

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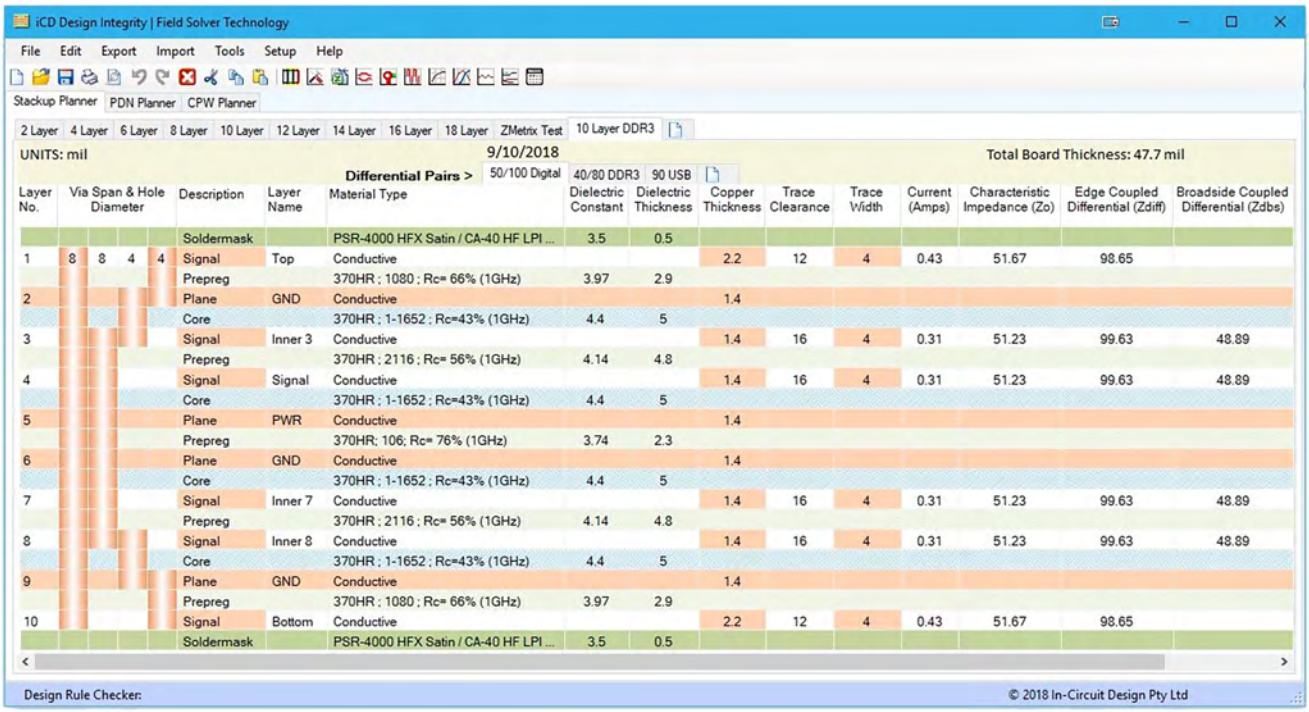


Figure 2: 10 Layer stackup with matched Ethernet, DDR3, and USB impedances (iCD Stackup Planner).

noise margins also decrease, which makes it even more critical to match the impedance. Figure 2 shows differential pairs set up to accommodate three different technologies on the same layers of the substrate.

Notice how the signal traces are tightly coupled to the reference planes. This helps prevent unwanted radiation, particularly on the outer microstrip signals. The center dielectric material (between layers 5 and 6) is also very thin (2.3 mils) and provides low-impedance planar capacitance to the power distribution networks (PDNs).

Unfortunately, drivers do not have the same impedance as the transmission line (typically 10–35 ohms), so terminations are used to balance the impedance, match the line, and minimize reflections. Reflections occur whenever the impedance of the transmission line changes along its length. This can be caused by unmatched drivers/loads, layer transitions, different dielectric materials, stubs, vias, connectors, and integrated-circuit (IC) packages. By understanding the causes of these reflections and eliminating the source of the mismatch, a design can be engineered with reliable performance.

Figure 3 shows how using a 12-mA LVCMOS 1.8-V driver of a Spartan 6 FPGA and an 18.7-ohm series resistor is required to match the driver to the 51.67-ohm trace on the outer

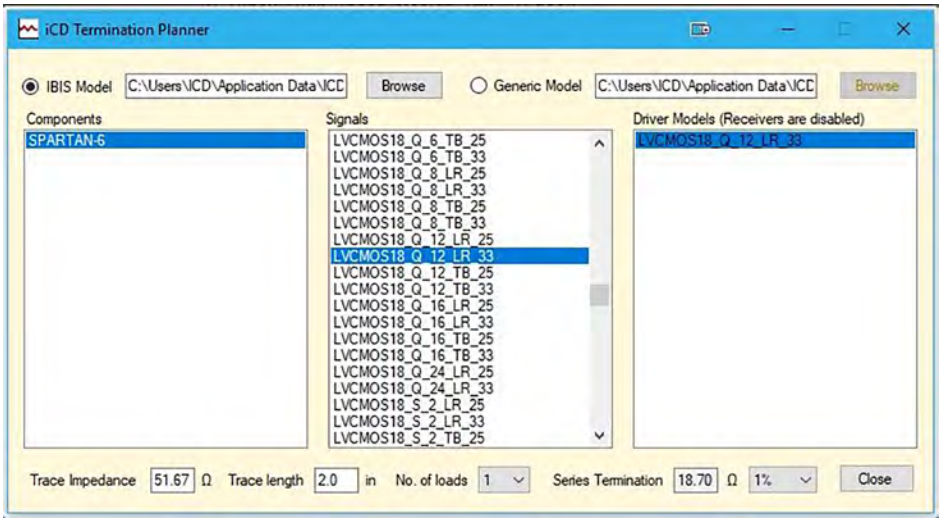


Figure 3: Matching the Spartan 6 driver to the transmission line (iCD Termination Planner).

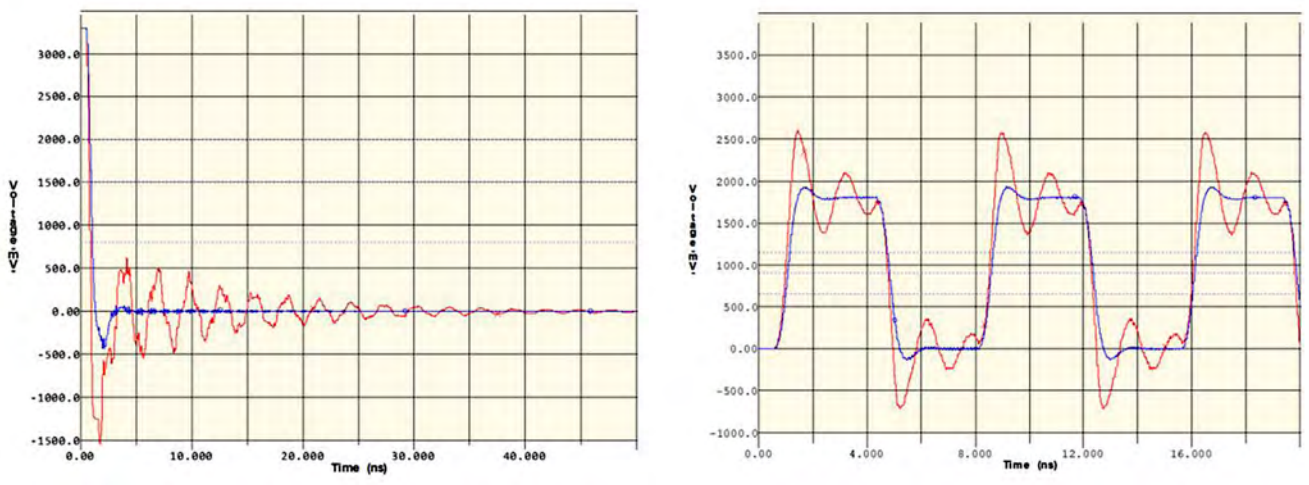


Figure 4: Ringing is reduced dramatically by adding a series terminator (simulated in HyperLynx).

layer. This is automatically derived from the IV curves of the Spartan 6 IBIS model by the iCD Termination Planner.

Figure 4 illustrates the ringing (red) in an unmatched transmission line. This ringing, which is also represented by over/undershoot (right), is dramatically reduced by terminating the transmission line with an 18.7-ohm series resistor (blue). Controlling the impedance of the transmission lines ensures that your product will perform more reliably and exhibit improved signal quality and reduced crosstalk and electromagnetic radiation.

III. Floor Plan the Placement Based on Connectivity: Place components by functionality and analog and digital groups to minimize interaction between different logic families and improve routability and timing.

Since aggressor signals induce crosstalk onto the victim signal, the higher the aggressor voltage, the more crosstalk will be induced. Therefore, it is best to segregate groups of nets according to their signal amplitude. This strategy prevents higher voltage nets (e.g., 3.3 V) from affecting lower voltage nets (e.g., 1.5 V), which have lower noise margins.

It is also preferable to partition these groups by rise time and frequency. Position the fastest devices closest to the connector (Figure 5). The placement should be graduated in descending order of speed down to the analog sections farthest from the connector to avoid noise coupling into sensitive devices.

All analog signals should be routed in the analog section and all the digital signals in the digital section. Of course, control signals must route between them. The segregation method, which I have used for many years, is to employ route fences or keep-outs. Route fences can be defined by placing elongated keep-outs on all layers. They are placed to direct the routing. No signal can cross these fences on any layer.

It is essential to keep in mind that high-speed return currents follow the path of least inductance. For example, if a trace is routed from the digital-to-analog converter (DAC) to

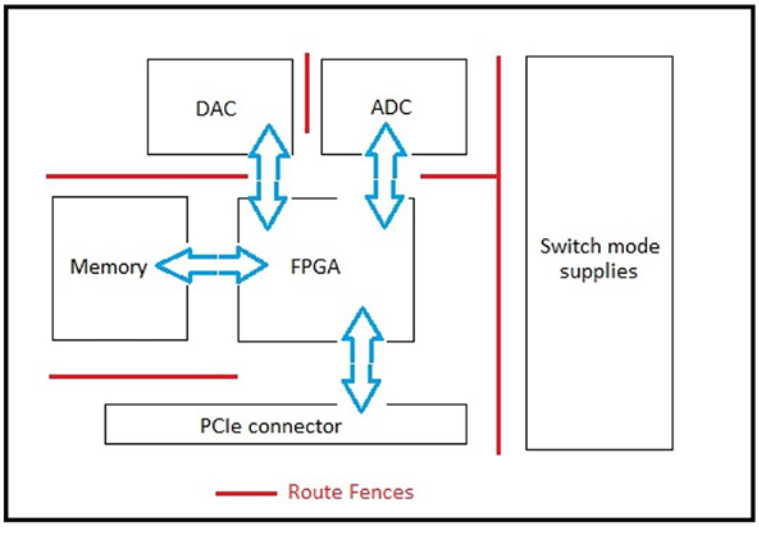


Figure 5: Components are segregated by logic groups and functionality.

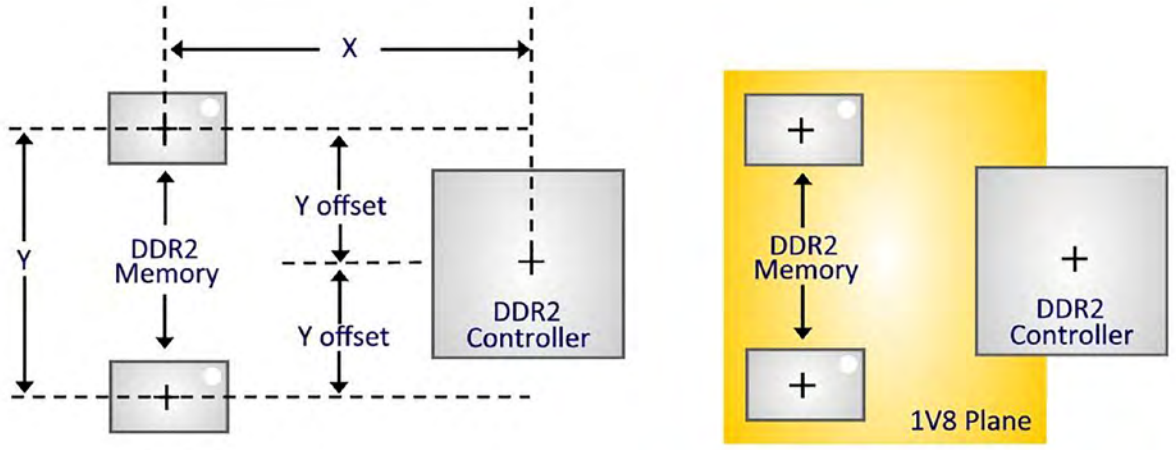


Figure 6: Processor and memory device placement requirements and 1.8-V plane.

the field-programmable gate array (FPGA), the return current path will be directly below that trace and will not wander into nearby sections. Route fences also control the autorouter by preventing signals from crossing and allowing the control signals to pass. Additionally, a disconcerting problem with high-speed boards is that their failure mode may be intermittent behavior across multiple manufacturing runs. In this case, the proper layout of the PCB may mean the difference between a reliable product and a board that performs intermittently.

Moreover, flight time delay and skew are key concerns in high-speed PCB design. One of the driving factors for flight time and skew performance is the placement of components. Controlling the maximum placement of devices, combined with the assumption that good design practices are adhered to, limits the maximum signal delay to approximately the longest Manhattan (X + Y) distance of the signals contained in a specific clock domain. Why the longest Manhattan distance? This is due to skew matching requirements. All of the shorter nets in a clock domain must be lengthened to skew match to the longest run length. Therefore, flight time and skew for an entire clock domain are governed by the maximum placement, along with the routing rules that constrain the matching of the trace lengths.

In the classic high-speed design flow, timing specifications and simulation results are compared to determine placement and routing constraints. Given a length constraint, a designer can manage signal integrity by controlling the PCB trace topology of the various parts of an interface.

Figure 6 (left) shows the required placement for T-topology routing of a DDR2 controller and memory chips. The purpose of the placement guide is to limit the maximum trace lengths and allow for routing and via space, which can be a challenge. This placement does not restrict whether these devices are placed on the top or bottom of the board. The region of the board used for DDR2 circuitry must be isolated from other signals. The DDR2 keep-out region is defined for this purpose and shown in Figure 6 (right). The 1.8-V power plane should cover this entire region, and non-DDR2 signals should be kept out of this region. Controlling the placement of devices minimizes interaction between different logic families, limits maximum trace length, reduces flight time delay and skew, and assists in complying with timing specifications.

Key Points:

- The impedance of the driver must match the transmission line for perfect energy transfer
- Digital design typically uses a characteristic impedance of 50–60 ohms; however, different technologies have specific impedance requirements
- Associated noise margins decrease as operating voltages decrease

- Drivers do not have the same impedance as the transmission line, so terminations are used to match the impedance
- Reflections occur whenever the impedance of the transmission line changes along its length
- Ringing can be dramatically reduced by terminating the transmission line
- The higher the aggressor voltage, the more crosstalk will be induced into the victim signal
- Position the fastest devices closest to the connector and be graduated in descending order of speed down to the analog sections farthest from the connector
- Route fences direct the routing, which prevents signals from crossing and allows the control signals to pass
- The return current path will be directly below that trace and will not wander into nearby sections
- The proper layout of the PCB may mean the difference between a reliable product and a board that performs intermittently
- Controlling the maximum placement of devices limits the maximum signal delay to approximately the longest Manhattan distance
- Given a length constraint, a designer can manage signal integrity by controlling the PCB trace topology of the various parts of an interface

Further Reading

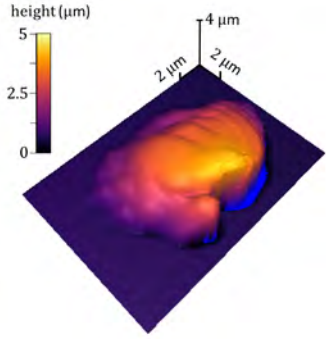
1. *Beyond Design: Stackup Planning, Part 2* by Barry Olney, *The PCB Design Magazine,* July 2015.
2. *Beyond Design: Controlled Impedance Design* by Barry Olney, *The PCB Design Magazine,* May 2015.
3. *Beyond Design: Impedance Matching–Terminations* by Barry Olney, *The PCB Design Magazine,* October 2013.
4. *Beyond Design: Critical Placement* by Barry Olney, *The PCB Magazine,* September 2012.
5. *Beyond Design: Mixed Digital-Analog Technologies* by Barry Olney, *The PCB Magazine,* August 2012.
6. *High-Speed Digital Design: A Handbook of Black Magic, First Edition* by Howard Johnson and Martin Graham, Prentice Hall, 1993.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded from www.icd.com.au. To read past columns or contact Olney, click here.

New NIST Method Measures 3D Polymer Processing Precisely

Recipes for 3D printing, or additive manufacturing, of parts have required as much guesswork as science. Until now.

Now, researchers at the National Institute of Standards and Technology (NIST) have demonstrated a novel light-based atomic force microscopy (AFM) technique–sample-coupled-resonance photorheology (SCRPR)–that measures how and where a material's properties change in real time at the smallest scales during the curing process.



3D printing, or additive manufacturing, is lauded for flexible, efficient production of complex parts but has the disadvantage of introducing microscopic variations in a material's properties. Because software renders the parts as thin layers and then reconstructs them in 3D before printing, the physical material's bulk properties no longer match those of the printed parts. Instead, the performance of fabricated parts depends on printing conditions.

NIST's new method measures how materials evolve with submicrometer spatial resolution and submillisecond time resolution–thousands of times smaller-scale and faster than bulk measurement techniques.

Surprising the researchers, interest in the NIST technique has extended well beyond the initial 3D printing applications. Companies in the coatings, optics and additive manufacturing fields have reached out, and some are pursing formal collaborations, NIST researchers say.

(Source: NIST)

Embedding Components, Part 4:
Passive Component Selection and Land Pattern Development

Designers Notebook

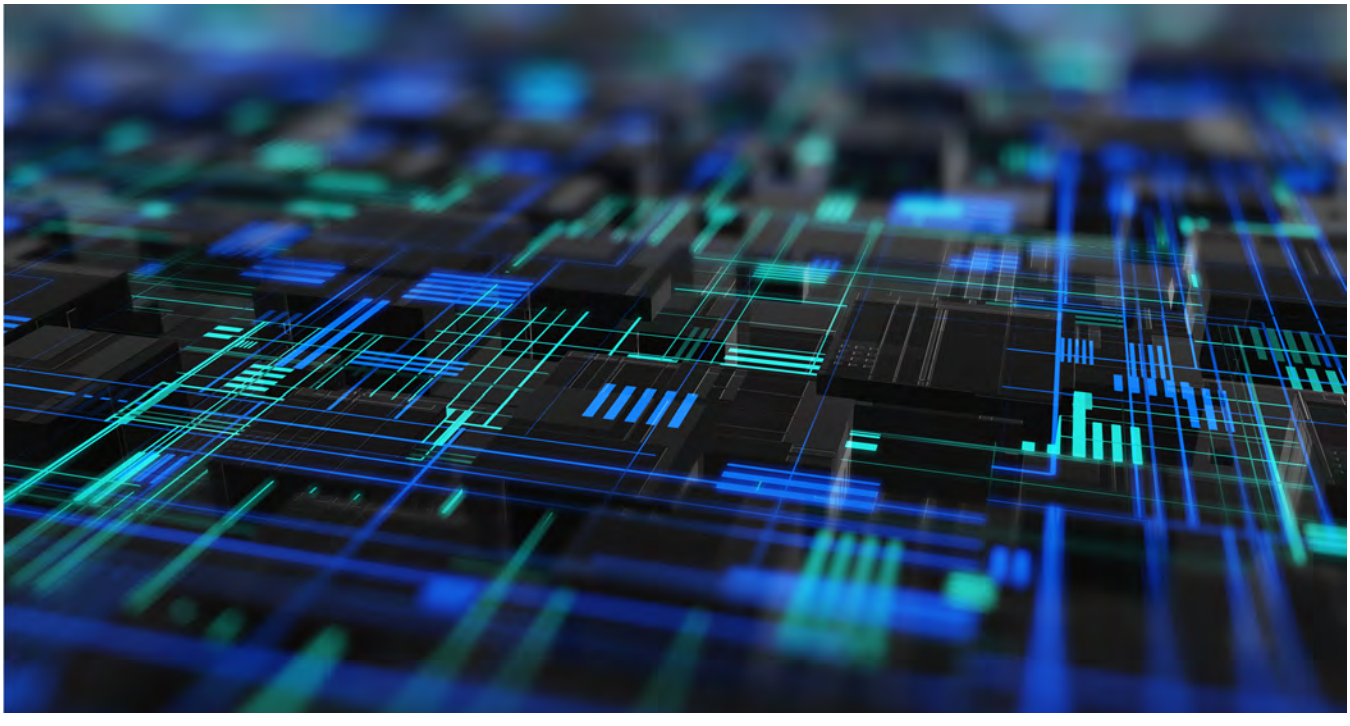
by Vern Solberg, CONSULTANT

This column will focus on land pattern development criteria, and methodology for accommodating low and moderately high-profile passive components within a multilayer circuit board.

As noted in Part 3 of this series, a broad range of discrete passive component elements are candidates for embedding, but the decision to embed these component elements within the multilayer circuit structure must be made early in the design process. While many of these components are easy candidates for integrating into the substrate, others may not be suitable, or they are difficult to rationalize because they involve more complex process methodology.

Substrate Development

Basic material sets selected for this embedded component application defines a 200-µm FR-4 epoxy-glass core base with 18-µm copper foil bonded to both sides. In this example, the buildup material includes pre-impregnated layers of glass cloth with an uncured epoxy resin furnished pre-dried, but not hardened, and layers of 18-µm copper foil. There are more than a dozen thickness options available for prepreg materials, but for this process description, a 200-µm material will be referenced. The prepreg layer and copper foils are sequentially bonded together using a combination of pressure and heat. The process begins with imag-



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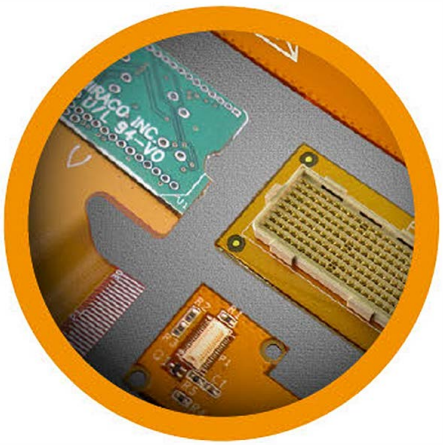

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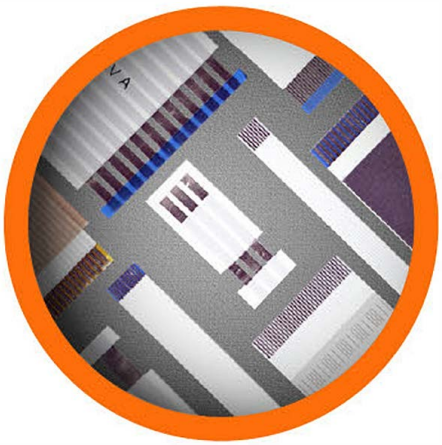

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ing and chemically etching the circuit pattern on the copper foil. The lamination, imaging, and etching processes continue until the layer structure is complete.

When embedding components in the multilayer structure, several factors must be considered:

- Circuit layer selected for attachment
- Component size (length, width, and height)
- Terminal area and metalization
- Location and orientation
- Method for termination

While thin passive components may not require any preparation before lamination, taller components will likely need developing a cavity-like pocket in the dielectric layer to ensure that the overall flatness of the finished multilayer PCB can be maintained. Regarding the attachment method for components, tin-alloy plated terminals will be most compatible with a tin-based solder alloy or a conductive polymer material that is either deposited or stencil printed onto the mounting site.

Land Pattern Development

Land geometry for two terminal passive components must provide 100% terminal-to-land surface contact. When terminating the component with solder or conductive polymer, users recommend extending each land beyond the terminal ends of the components by 0.25 mm (0.010"). This small extension of the land pattern enables the formation of a small fillet at each end of the component and furnishes visual access for inspection of the joining material before the next stage of lamination (Figure 1).

Embedded Component Land Pattern Criteria

Two criteria for embedding component land patterns include enabling component terminals to achieve full area contact and providing a minimum 0.25-mm toe protrusion for inspection. However, the land pattern does not need to be greater in width than the component body and the gap or space between the component's terminals. Further, the land pattern on the surface of the PCB should be equal to the gap dimensions furnished by the manufacturer. Refer to Table 1 for guidance in developing land pattern geometry for the embedded resistor family.

Embedded Component Substrate Development

The discrete component parts selected for embedding within a multilayer circuit board or interposer structure will be subjected to many physical stresses during multiple lamination stages. The initial placement and joining of the device onto the inner layer substrate surface are critical factors. However, the subsequent lamination process can subject the surface-mount technology (SMT) component elements to both thermal and physical extremes not experienced when devices are mounted onto the outer surfaces of the PCB substrate. For example, the pressure on the components and laminate materials during the heating cycle can be as high as 3000 Kg for up to two hours.

When selecting passive components for embedding, PCB designers should first review the outline dimensions of the candidate components, component thickness, and terminal

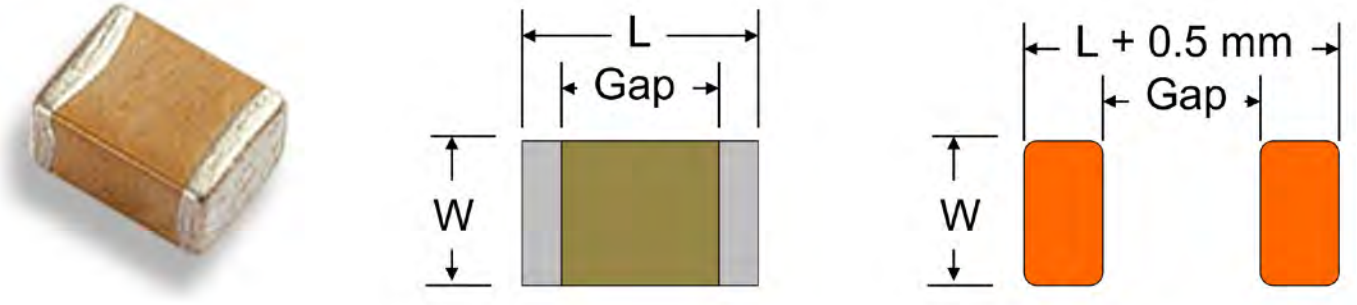
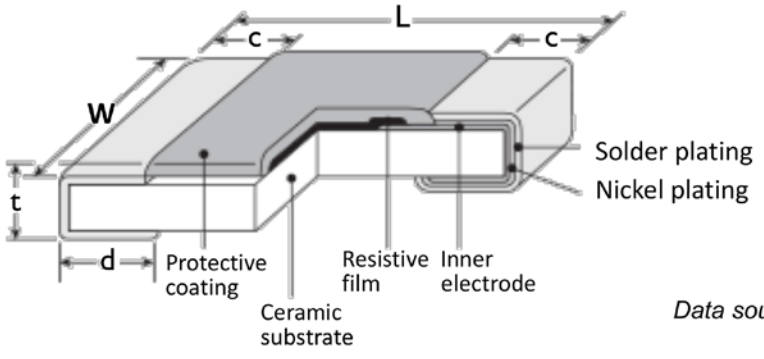


Figure 1: Two terminal passive component land pattern criteria.

Size	L	L + 0.50 mm	W	Terminal	Gap = L - 2t
1206	3.20 mm	3.70 mm	1.60 mm	0.50 mm	2.20 mm
0805	2.00 mm	2.50 mm	1.50 mm	0.50 mm	1.00 mm
0603	1.60 mm	2.10 mm	0.80 mm	0.35 mm	0.90 mm
0402	1.00 mm	1.50 mm	0.50 mm	0.25 mm	0.50 mm
0201	0.60 mm	1.10 mm	0.30 mm	0.15 mm	0.30 mm
01005	0.40 mm	0.90 mm	0.20 mm	0.10 mm	0.20 mm
008004	0.25 mm	0.75 mm	0.12 mm	0.07 mm	0.11 mm

Table 1: Land pattern development for two terminal passive components.

Size	L	W	t	d
1206	3.20 mm	1.60 mm	0.60 mm	0.40 mm
0805	2.00 mm	1.50 mm	0.60 mm	0.30 mm
0603	1.60 mm	0.80 mm	0.45 mm	0.30 mm
0402	1.00 mm	0.50 mm	0.35 mm	0.25 mm
0201	0.60 mm	0.30 mm	0.23 mm	0.23 mm
01005	0.40 mm	0.20 mm	0.13 mm	0.13 mm



Data source: KOA

Table 2: SMT resistor family.

metalization alloy. The smallest outline and thinnest profile devices are the most critical attributes for embedding. As noted in Part 3, the smallest discrete resistor is furnished in a standard 01005 component outline and is available in most standard values. For example, Table 2 shows dimensions for six standard outline variations of the surface mount resistor family. However, due to their excessive thickness, any component larger than the 0402 in this family may not be suitable for embedding.

Discrete resistors are all rectangular in shape with a metal-oxide film deposited onto a high-alumina ceramic base and terminated at electrodes at two ends. For example, the 01005 device in Table 2 only measures 0.40 x 0.20 mm, and the component thickness does not exceed 0.15 mm. This component is 55%

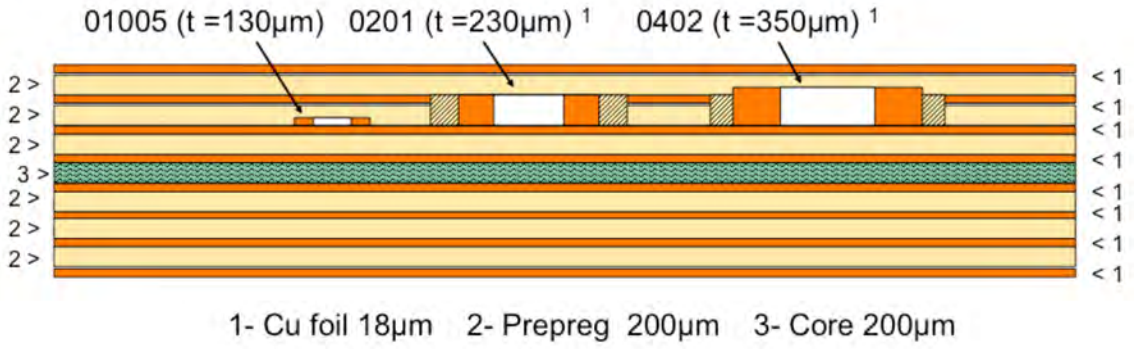


Figure 2: Embedding discrete passive resistor elements.

smaller than the 0201 chip-resistor element. However, when expanding current capacity, a more substantial outline component with a higher watt rating will be required. The height of the component will also increase. To accommodate the higher component profile, it will be necessary to provide additional clearance (cavity) in the PCB layer structure (Figure 2).

[1] *For components with a higher profile, the PCB fabricator will need to delete portions of the prepreg and copper foil material selectively.*

The discrete SMT capacitor family also includes the 01005 outline component and an even smaller 008004 outline device, but value range and sourcing of the smaller component will be limited. Some companies are supplying the 01005 outline capacitor with a thickness no greater than 0.20 mm (the 01005 resistor is only 0.13 mm). Meanwhile, capacitors furnished in the 008004 outline are a mere 0.125 mm in thickness, but as the dielectric volume decreases, the value range also becomes limited. Table 3 details capacitor outline varia-

Size	L	W	T	e
1206	3.20 mm	1.60 mm	0.60 mm	0.50 mm
0805	2.00 mm	1.50 mm	0.60 mm	0.50 mm
0603	1.60 mm	0.80 mm	0.45 mm	0.35 mm
0402	1.00 mm	0.50 mm	0.35 mm	0.25 mm
0201	0.60 mm	0.30 mm	0.30 mm	0.15 mm
01005	0.40 mm	0.20 mm	0.20 mm	0.10 mm
008004	0.25 mm	0.12 mm	0.125 mm	0.07 mm

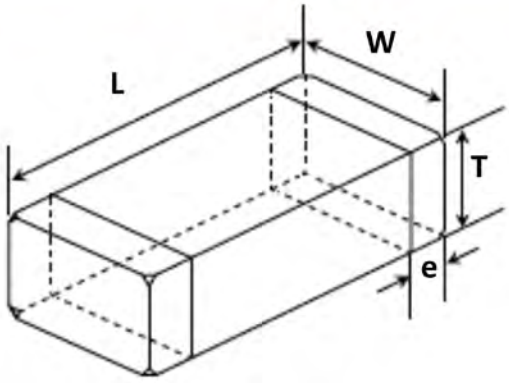


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Table 3: SMT capacitor family.

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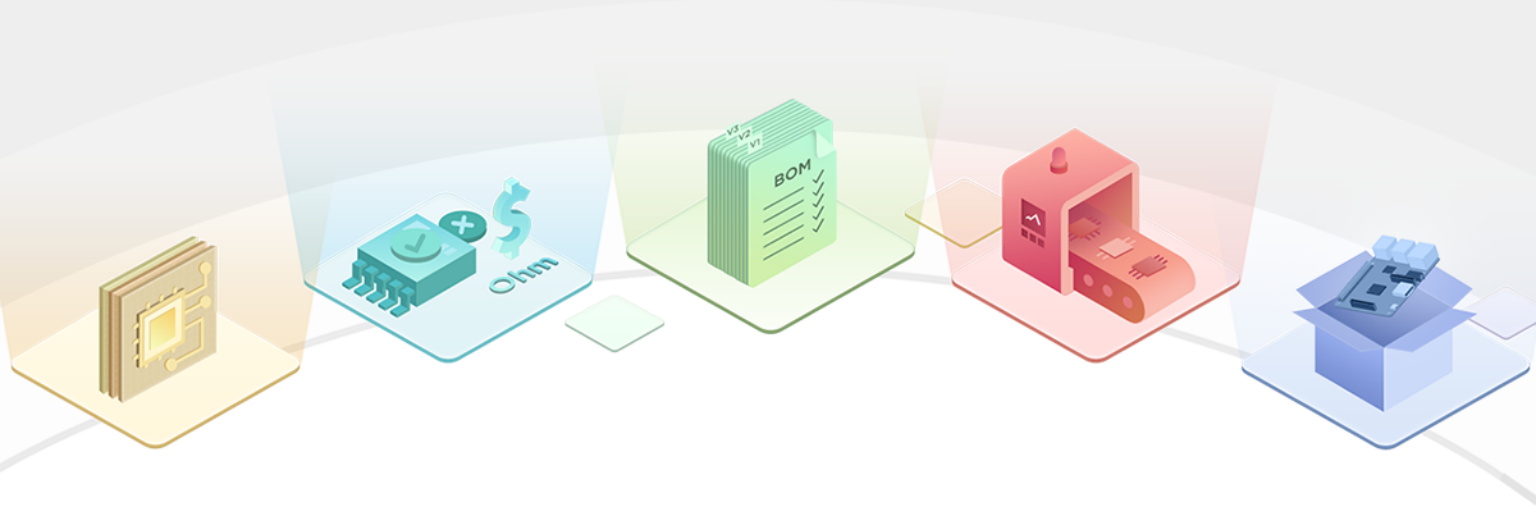

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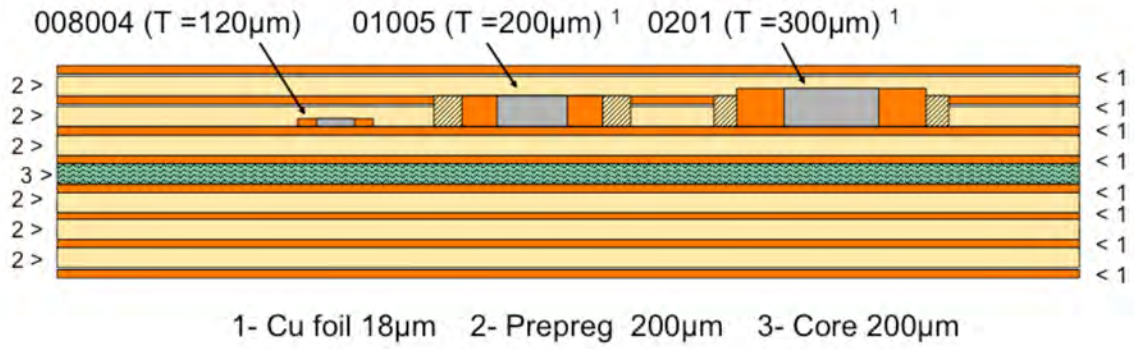


Figure 3: Embedding discrete passive capacitor elements.

Type	L	W	t	d
0402	1.00 mm	0.50 mm	0.35 mm	0.25 mm
0603	1.60 mm	0.80 mm	0.80 mm	0.30 mm

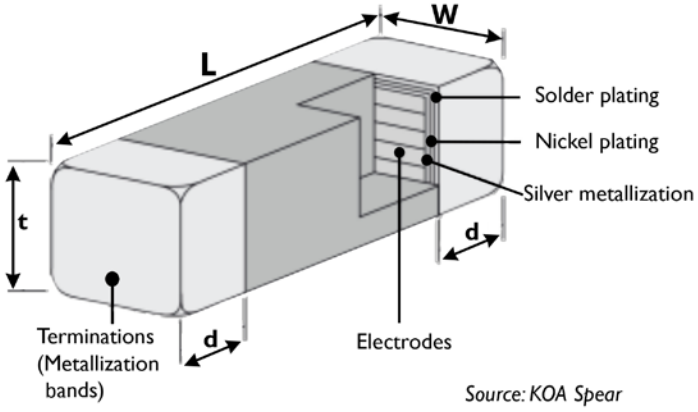


Table 4: Multilayer inductor.

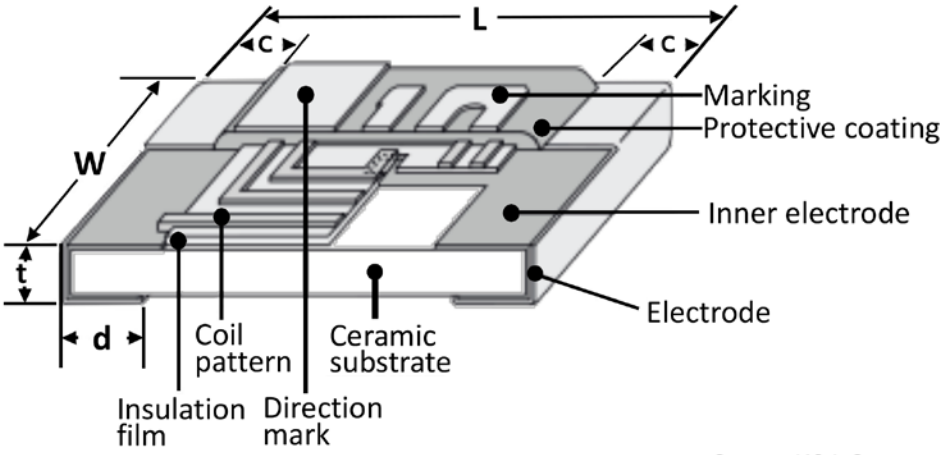
tions developed for surface mounting, but as previously noted, due to the excessive height of components greater than 0402, they may not be a good option for embedding without extending the cavity further into upper circuit layers.

Dielectric working voltages and value ranges for the smaller capacitor outlines may be somewhat limited, and manufacturers warn that ceramic multilayer capacitors, if not properly positioned, can be prone to cracking. To minimize physical stress designers, designers are advised to position capacitors with a standard orientation within the embedded substrate structure. For the larger resistor components, thinner components will usually not need special attention when laminating circuit layers. However, the higher profile component will require that the PCB fabricator modify the copper on the circuit layer directly above the capacitor to create a cavity in the prepreg material around the component's perimeter (Figure 3).

[1] *Prepreg and copper foil material slightly larger than the component outline must be removed before lamination.*

Small outline inductors are also available from limited sources with values ranging up to 100 nH. There are currently only two types of discrete inductor types that are suitable for embedding into the PCB: multilayer ceramic and thin-film multilayer on ceramic. Multilayer ceramic and thin-film inductor products have a relatively small outline, but their thickness

Type	L	W	t	d
0402	1.00 mm	0.50 mm	0.35 mm	0.25 mm
0603	1.60 mm	0.80 mm	0.50 mm	0.30 mm
0805	2.00 mm	1.25 mm	0.50 mm	0.30 mm
1206	3.20 mm	1.60 mm	0.60 mm	0.40 mm



Source: KOA Spear

Table 5: Thin-film inductor.

(t) may be an issue. The example shown in Table 4 represents two multilayer inductors that can be considered for embedding in the circuit structure.

Although the excessive thickness of the 0603 inductor may make it impractical for embedding, the 0.35-mm profile of the 0402 device outline should be acceptable for embedding, even though the greater component thickness will also require a cavity in the circuit structure typical of that illustrated for the resistor and capacitor components. The five multilayer thin-film inductor devices shown in Table 5 represent outline variations characteristic of the resistor and capacitor families. They are said to be excellent for high-frequency applications, have a low DC resistance, high Q, and are furnished with terminal plating most suitable for solder or conductive polymer attachment.

The value range for the 0402 inductor is limited. More values may be offered for the larger outline inductors, but the excessive height of the other four inductors listed in the table will eliminate them for embedded component applications without increasing cavity size.

Embedded Component Assembly

The terminal plating alloy specified must be selected to be compatible with the specific joining method employed. While the tin-plated terminals are more common and compatible with solder or conductive polymer attachment, some discrete passive components can be supplied with copper or gold terminal plating. The copper-plated terminals will be specified when direct microvia termination is required.

Alternative component termination methodologies and PCB surface plating variations will be discussed further in Part 5 of this series. **DESIGN007**

Vern Solberg is an independent technical consultant specializing in surface mount technology, microelectronics design, and manufacturing technology. To read past columns or contact Solberg, click here.

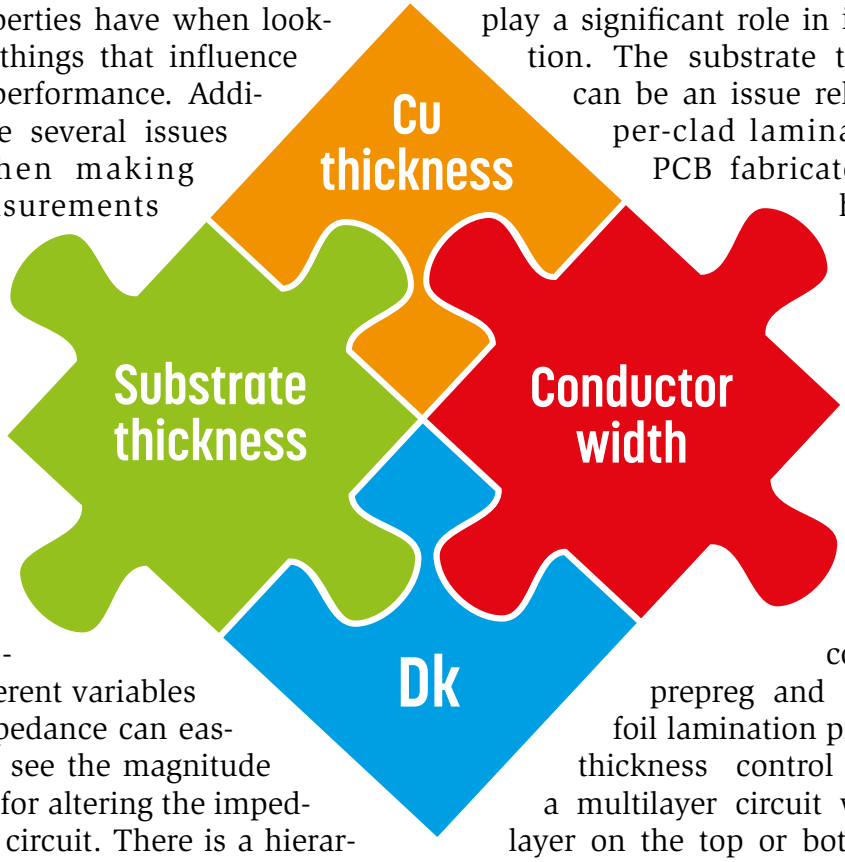
Different Aspects of Impedance for PCBs

Lightning Speed Laminates
by John Coonrod, ROGERS CORPORATION

Many PCBs are specified to have a controlled impedance value. There are several circuit and material properties that impact the impedance performance of a circuit. Some of these properties are obvious to engineers who have worked with controlled impedance boards over the years. However, even experienced engineers are sometimes surprised to find the level of impact these properties have when looking at all of the things that influence PCB impedance performance. Additionally, there are several issues to consider when making impedance measurements to ensure the values are accurately captured.

As a reference, consider a microstrip transmission line circuit. When an impedance model is generated for a PCB microstrip construction, the different variables that influence impedance can easily be changed to see the magnitude each variable has for altering the impedance value of the circuit. There is a hierarchy of the influences of these variables on PCB impedance. For a microstrip transmission-line circuit, the most to least influential variables include substrate thickness, conductor width, copper thickness, and dielectric constant (Dk).

As a material supplier, we are often asked to investigate the Dk of our material when a circuit has an issue with incorrect impedance. In reality, the Dk is the least impactful variable for impedance. It is much more common for substrate thickness and conductor width to play a significant role in impedance variation. The substrate thickness concern can be an issue related to the copper-clad laminate and/or the PCB fabricator, depending on how the circuit construction. In general, the substrate thickness control is better for a microstrip circuit using the copper-clad laminate compared to a microstrip that a PCB fabricator might construct using a prepreg and copper foil for a foil lamination process. Due to the thickness control issue—assuming a multilayer circuit with a microstrip layer on the top or bottom of the structure—a circuit with a demanding impedance specification is usually best when made with a laminate from the material supplier as



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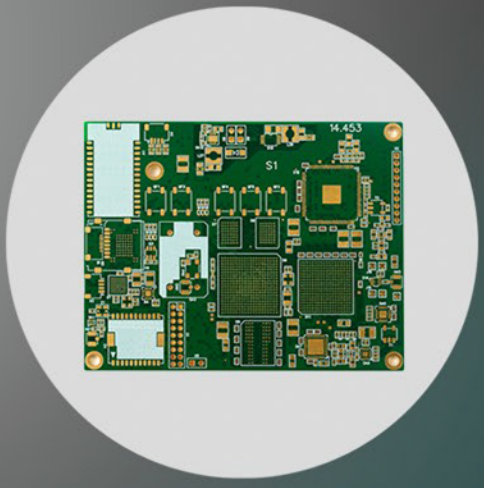

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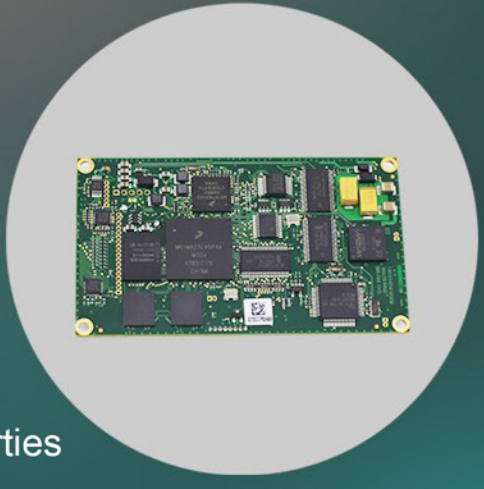

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opposed to a foil lamination at the PCB fabricator.

Controlling the signal conductor width is more critical for circuits that use thin substrates because thinner substrates usually have narrower conductors. A normal conductor width tolerance is ± .5 mil, but this can depend on the copper thickness and circuit density. For a circuit using a thick substrate and a wide signal conductor, the common conductor width tolerance has less influence on impedance variation than a thin circuit with a narrow conductor. The impedance of a circuit using a narrower conductor is impacted more by the conductor width tolerance than a circuit using a wider conductor.

The impedance of a circuit using a narrower conductor is impacted more by the conductor width tolerance than a circuit using a wider conductor.

Copper plating is applied in the process to generate plated through-hole vias and has some thickness variation. Even though the copper thickness variation can impact the impedance performance of the circuit to a lesser degree than substrate thickness and conductor width, a larger concern is usually how thicker copper can increase the conductor width tolerance. Thicker copper cannot be etched as accurately for good conductor width control as thinner copper; however, there are exceptions, depending on the image and etching processes.

The most influential variables should be considered for impedance control. If the PCB design has a tight specification for impedance, a substrate with strong thickness control should be considered along with a well-controlled process for generating the signal conductor width. Copper thickness control and Dk control are important as well, but these are typically less critical for impedance accuracy. However, Dk consistency is extremely influential for the phase response of the radio-frequency (RF) circuit.

Additionally, the measurement of impedance has many issues to consider. Typically, a time-domain reflectometer (TDR) is used to measure the impedance of a PCB. There are many types of TDRs with different capabilities. In general, the rise time of the TDR is essential and a faster rise time will allow more accurate impedance measurements. Further, there can be an issue with masking, which is a term used to explain that a large impedance anomaly can mask the true impedance anomaly behind it.

The basic operation of a TDR is to send a pulse down a circuit and look at the reflected energy to determine the impedance. It is not uncommon to have a large impedance anomaly where the test probe meets the circuit being tested for impedance. This impedance anomaly will reflect a lot of energy back to the TDR, and less energy will propagate down the circuit. This makes other impedance measurements after the impedance anomaly somewhat altered.

It is relatively easy to evaluate this issue by testing a circuit that has a good impedance anomaly where the probe meets the circuit, then use a tool to alter the circuit pattern in the area where the probe touches the circuit and causes a worse impedance anomaly. After this, retest the circuit and a change in impedance will often be detected. Depending on the TDR's capabilities and the circuit construction, the impedance of the trace will change from the original measurement. In some cases, it may be very little, and in others, more significant. **DESIGN007**

John Coonrod is technical marketing manager at Rogers Corporation. To read past columns or contact Coonrod, click here.

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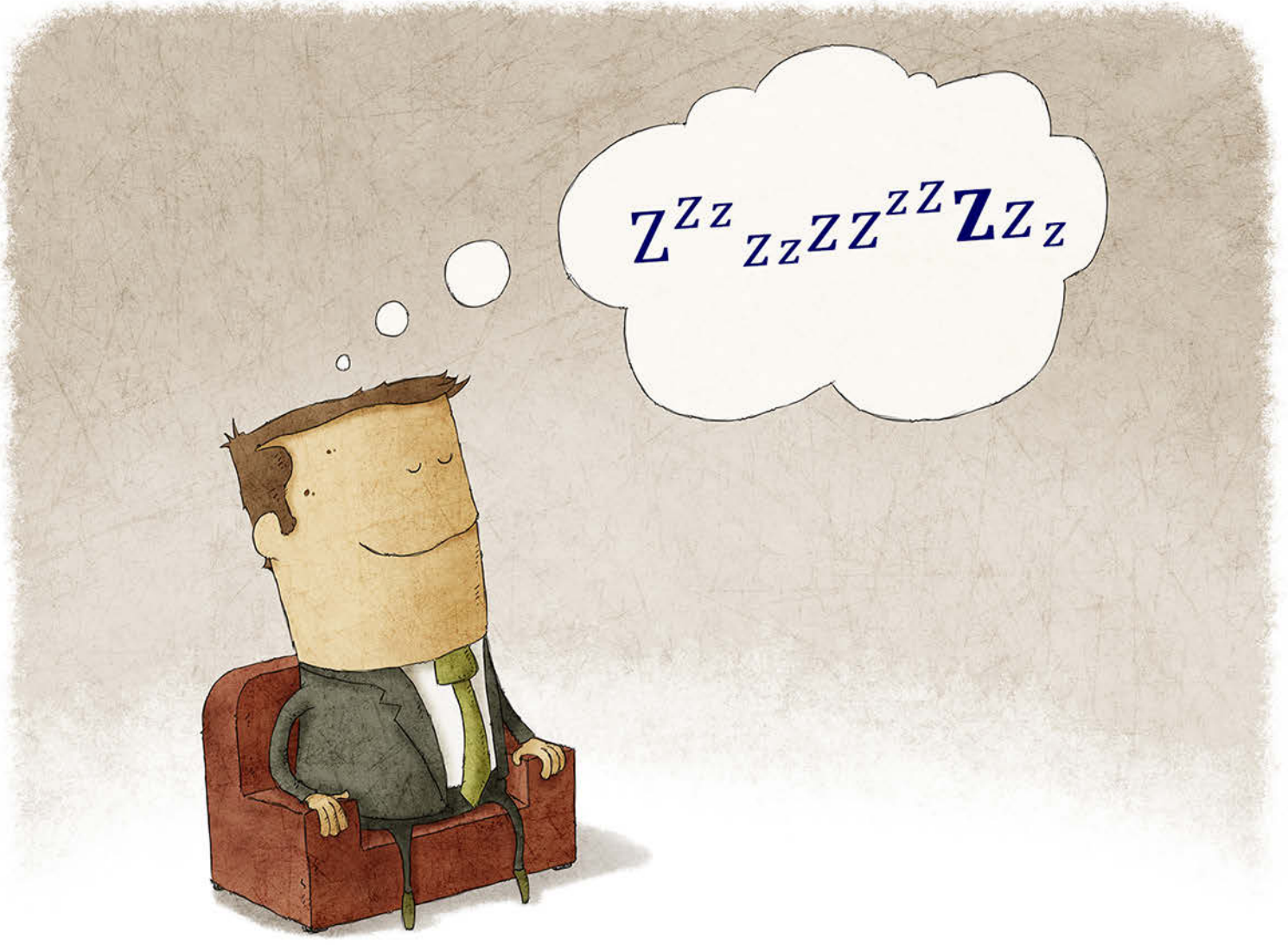

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MilAero007 Highlights

ERAPSCO Inks $64.6M in Navy Sonobuoy Contracts ▶

Sparton Corp. and Ultra Electronics Holdings plc announce the award of subcontracts valued at $64.6 million to their ERAPSCO joint venture for the manufacture of sonobuoys for the United States Navy.

Michael Clarke Named CEO of Sanmina ▶

Michael Clarke, a member of the board of directors of Sanmina Corp. since 2013, has been appointed the new CEO of the company effective October 1, 2018.

API Names Michael Schwarm Global VP of Sales and Marketing ▶

API Technologies Corp. (API) has named Michael Schwarm as vice president for global sales and marketing.

John Karkoski to Lead Zentech's Mil-Aero and Space Market Initiative ▶

John Karkoski has joined Zentech Manufacturing Inc. as director of business development for the military and aerospace markets.

OSI Systems Reports Record Q4 FY 2018 Revenues ▶

OSI Systems Inc. has reported revenues of $287 million for the fourth quarter of fiscal 2018, an increase of 14% from the $252 million reported for the fourth quarter of fiscal 2017.

Nortech Systems Approves Stock Repurchase Program ▶

Nortech Systems Inc.'s board of directors has approved another installment of a stock repurchase program similar to the company's inaugural repurchase program that expired last month.

Circuitronics Promotes Ken Mount to Quality Manager ▶

Ken Mount, a Certified IPC Trainer and a Lean Six Sigma Green Belt with expertise in 5S, 5S + 1, and DMAIC, has been promoted to quality manager of Circuitronics.

IEC Electronics Names New CFO ▶

IEC Electronics Corp. has appointed Thomas L. Barbato as senior vice president of finance and CFO.

Infinite Electronics Names Laurie Addison as VP of Marketing ▶

Infinite Electronics Inc. has named Laurie Addison as vice president of marketing for the company.

ACDi Celebrates Milestone with $10,000 FCPS Donation ▶

American Computer Development Inc. (ACDi) has presented a donation of $10,000 to the Frederick County Public Schools (FCPS) to mark a major milestone in the firm's history—its 10,000th design order. The donation is targeted to support STEM—science, technology, engineering and math—programs and inspire students to pursue STEM careers.

IPC President Commends White House for Assessment of US Defense Industrial Base ▶

On behalf of the electronics industry, I commend the White House for the release of a sweeping and detailed assessment of the nation's defense industrial base. IPC and its members look forward to studying the report and its recommendations in the coming days and weeks, and we welcome the report's larger conclusion that the U.S. electronics industry needs to be strengthened.

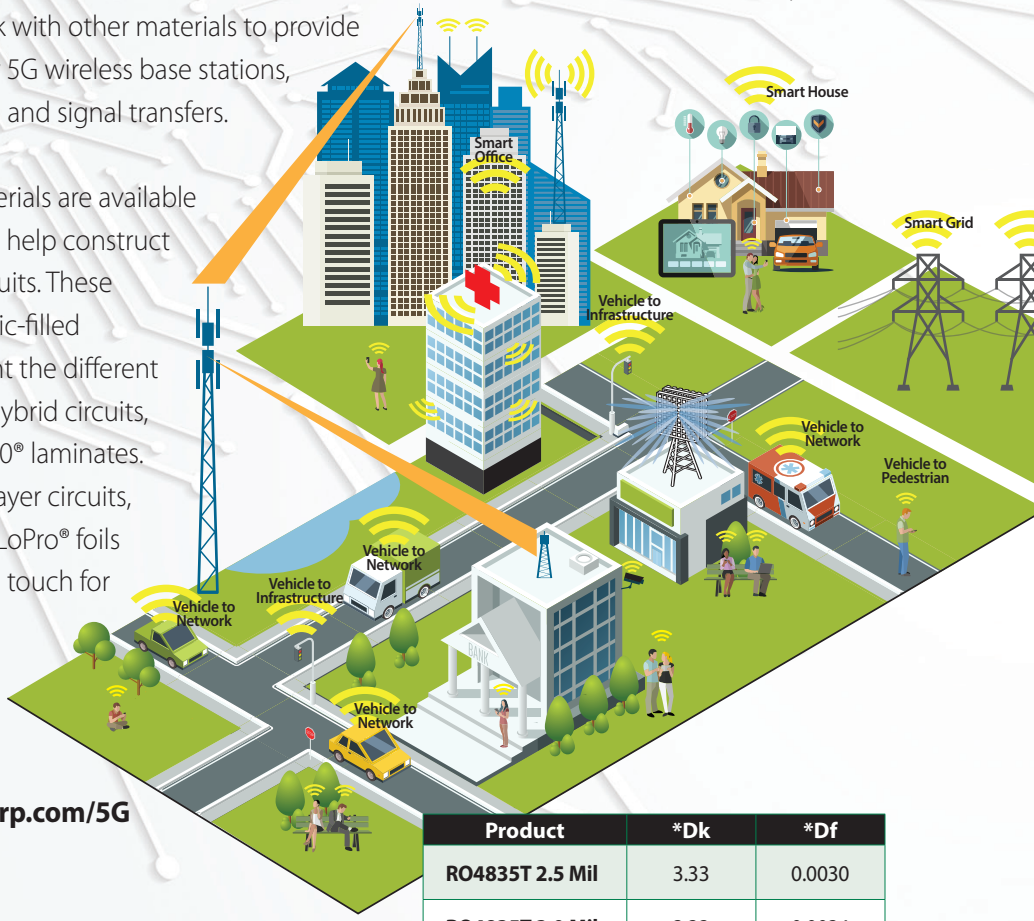
5G: Higher Frequencies!

Do you have the **right** circuit materials?

Frequencies at 28 GHz and higher will soon be used in Fifth Generation (5G) wireless communications networks. 5G infrastructure will depend on low-loss circuit materials engineered for high frequencies, materials such as RO4835T™ laminates and RO4450T™ bonding materials from Rogers Corporation!

Rogers RO4835T spread-glass-reinforced, ceramic-filled laminates are low-loss materials in 2.5, 3.0, and 4.0 mil thicknesses. They are well suited for millimeter-wave frequencies as part of the inner cores of 5G hybrid multilayer PCBs. They can work with other materials to provide the many functions needed by 5G wireless base stations, including power, signal control and signal transfers.

Rogers RO4450T bonding materials are available in 3, 4, and 5 mil thicknesses to help construct those 5G hybrid multilayer circuits. These spread-glass-reinforced, ceramic-filled bonding materials complement the different materials that will form these hybrid circuits, including RO4835T and RO4000® laminates. And for many 5G hybrid multilayer circuits, Rogers CU4000™ and CU4000 LoPro® foils will provide a suitable finishing touch for many hybrid multilayer circuit foil lamination designs.



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RO4835T 4.0 Mil	3.32	0.0036
RO4450T 3.0 Mil	3.23	0.0039
RO4450T 4.0 Mil	3.35	0.0040
RO4450T 5.0 Mil	3.28	0.0038

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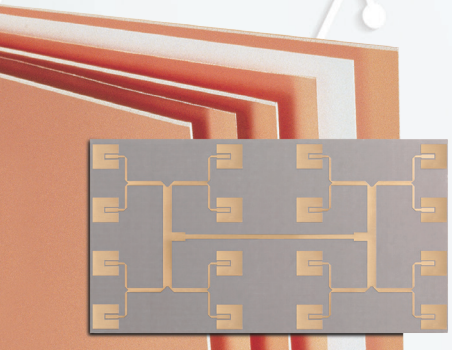

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New Designers Council Column: The Digital Layout

Article by Andy Shaughnessy
I-CONNECT007

The IPC Designers Council is launching a new column in *Design007 Magazine:* "The Digital Layout." I recently asked two IPC Designers Council (DC) Executive Board members, Mike Creeden and Steph Chavez, to discuss the content and objective of their new column, and how this all ties in with the DC.

Andy Shaughnessy: Mike, what can we expect in this new Designers Council column?

Mike Creeden: I'll give an overview of PCB design layout and some of the transitions that we're experiencing. Our new column is called "The Digital Layout." The design profession has evolved over the years, and to meet today's challenges, all designers need to view layout from three concurrent perspectives. The first is layout solvability, which entails mastering the CAD tool and solving the layout. With today's technologies, using HDI is becoming commonplace and is often a complicated puzzle to solve. Second, there's the performance of the circuit; EMI, signal integrity, power integrity, and thermal performance must be considered. Third, designers should use DFX in all areas of manufacturing.

In our industry, there are a significant number of EEs being asked to take on the layout portion. Many EEs and designers, especially those who work remotely, may not be aware of the IPC Designers Council and what it can do for them.

Our hope is to make people aware of the resources and events that the IPC Designers Council provides. IPC is not a "them"; it's an "us." IPC is a reflection of the industry. When I volunteer on the committee meetings, I see participants from across the industry, the country, and the world who are all contributing to the standards.

Shaughnessy: Standards are always a good topic. Pro or con, it's a great conversation.

Creeden: Sure. I've heard a lot of people say recently, "Why do we need standards? Just

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build it!" What you need to realize is that we ask our supply chain to build to standards. We legally hold them accountable to produce a Class 2 or Class 3 board, and then we design to the requirement of an IPC Class with a producibility level. The producibility level affects yields and profit margins, so these are very important aspects to the standards.

This month you're covering data. What I would say about data is that a manufacturer must work with the data designers supply. Designers should understand the manufacturing process and how to support the manufacturers while ensuring that circuits will to perform properly.

There's a lot of activity going on with IPC. There's a new platform called "The IPC Edge" that is essentially an online learning platform. Steph and I are both certified IPC instructors for the CID and CID+ classes. We are also members of the executive board for the Designers Council. There are also local chapters spread across the globe where designers can participate.

Mike Creeden

The whole purpose of the Designers Council is to facilitate an orderly exchange of design concepts concerning printed board manufacturing and design.

The whole purpose of the Designers Council is to facilitate an orderly exchange of design concepts concerning printed board manufacturing and design. IPC offers technical education and events both on-site and online. We have conferences, workshops, webinars, and professional certification programs. Further, there's no fee to join. Members have access to design-related events, programs, communications, and technical support, as well as the DC forum and bulletin board.

There are a lot of networking and technical education opportunities. You can participate in the development of standards. We make these standards; IPC doesn't make the standards. We make the standards by participating in the industry. Remember that IPC membership is for your organization, but the Designers Council is for the individuals doing design layout.

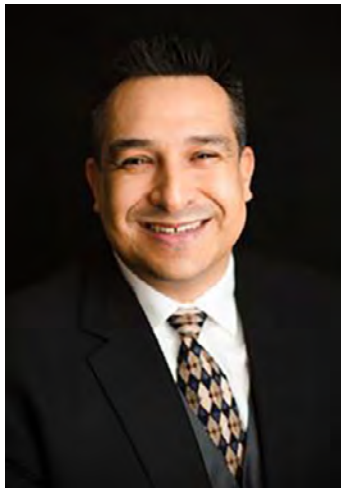
Because many people can't attend these events for a variety of reasons, we've decided to partner with our friends at I-Connect007. We'll be providing an ongoing, monthly column to cover these topics. To be fully transparent, we will also have a similar presence with UP Media's publication. Steph has been named the communications officer and head of the steering committee. Steph, why don't you take over?

Steph Chavez: Sure, Mike. First, let me start by saying that I couldn't agree with you more on what you shared or say it any better than you just did, so I'll add some additional content to what you've already laid out. The biggest point we want to make is that we want this communications committee to be a center point to help facilitate and guide the local area chapters and global designers to start communicating and collaborating more with each other. There are about 25 of us along with many other IPC chapter leaders that are volunteering our time to do this, and we're always eager to help foster positive energy and collaboration moving forward.

Global communication is key for overall success as a united industry community. With this committee, we will provide general IPC and Designers Council news and updates to everyone globally. We will also provide an overview of information on training centers like EPTAC Corporation and others that are available for

continued education and professional development. We'll share schedules and locations where the IPC designers certifications are taking place. We'll also share up-and-coming industry events, seminars, conferences, and workshops.

As Mike mentioned, he and I both are CID and CID+ instructors, so we teach regularly. We fly around the country—and in some instances, around the world—to teach these classes. A lot of students we meet simply don't know what they don't know. They don't have a good resource or professional network to tap into, or they don't know where to look to find specific industry information, or when the next professional development class is going to held. Since you can't go to a major university and find a curriculum specifically dedicated for PCB design, we are creating this committee to become a main hub of up-to-date information and resource content from the DC globally regarding professional development and local chapter activities. The biggest point we want to make is to start communicating between chapters and designers so we can function as one big community rather than isolated islands. As the saying goes, "There is strength in numbers."


Steph Chavez

Creeden: That's right. We really want to communicate with the readers. We encourage you to participate as a listener, and potentially as a writer. I encourage Designers Council members to write to Steph, and he'll show you exactly how to participate in the column. I also encourage you to share this information with your peers and friends in the industry, and let's collectively make this our success.

Shaughnessy: Will this column have a rotating list of contributors?

Creeden: Correct. We've asked members from different local chapters to contribute articles and events. For example, there's a very strong Designers Council in the Research Triangle area in North Carolina. They will hold a show called PCB Carolina on November eighth of this year so we can give them time slots in the column around that show. The same thing can be true with the Silicon Valley group around PCB West or the San Diego chapter around IPC APEX EXPO.

Additionally, the Orange County DC chapter boasts a membership of over 100 in attendance. We'd like to acknowledge their long-standing success. They are valuable to their local electronics community.

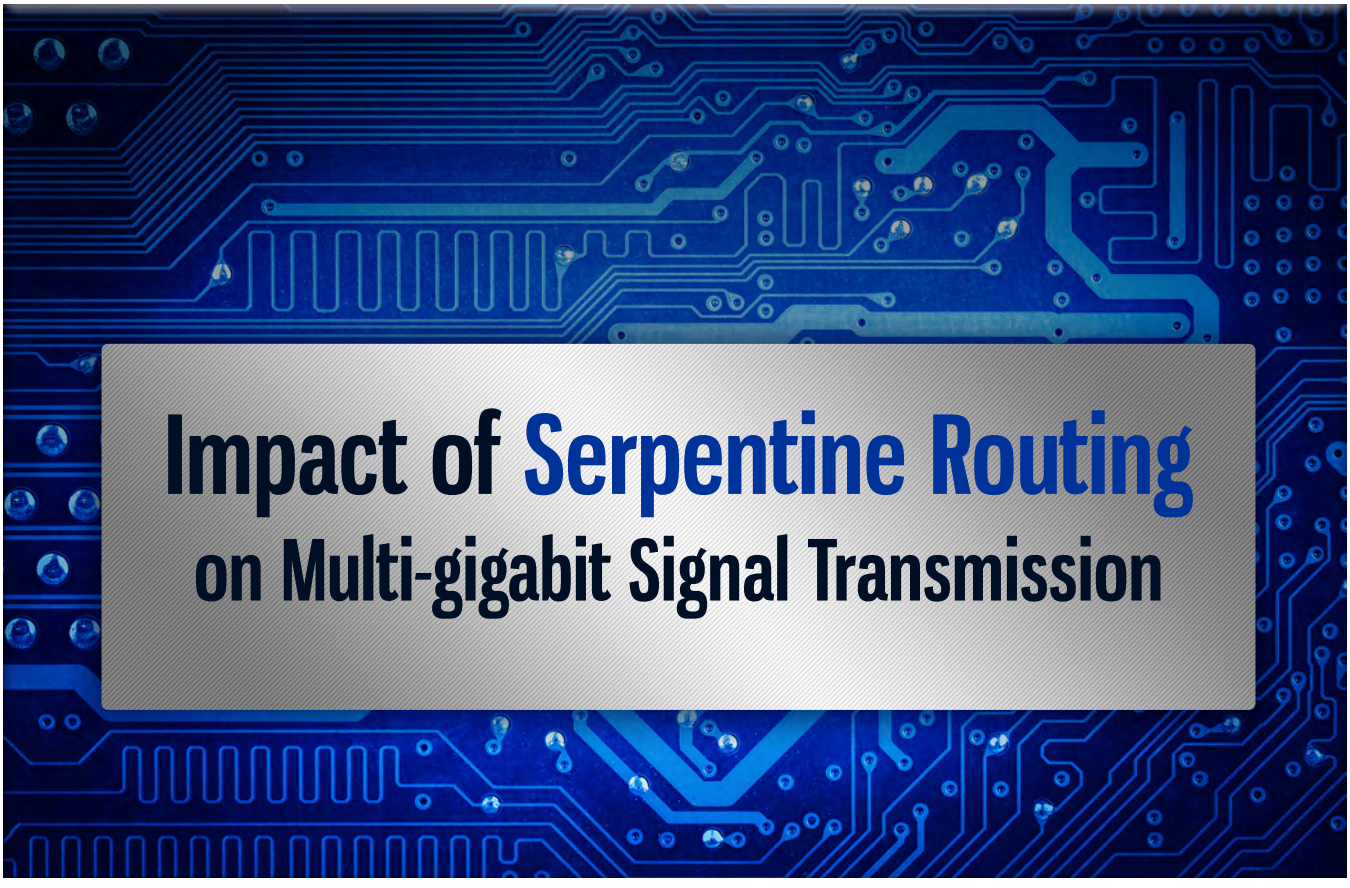
Another one of our goals is to encourage people to form their own DC chapter. It truly takes a champion to lead that effort locally, but we have some infrastructure that we can lend in the formation of a new chapter. We'll support you as you grow.

Chavez: There is a lot of great industry content and professional networking opportunities that come from local chapter meetings. With this column, readers can gain industry knowledge, get local area chapter updates, and be a part of a chapter, even if they don't have a local one in their area. Another great opportunity from this column is to get on the email list of each identified respective local DC chapter so that you can gain access to all available professional development content that is being shared with chapter members.

Shaughnessy: I'm looking forward to working with you guys on your column. We're always happy to support the Designers Council. Thanks for speaking with me.

Creeden: Thank you very much for your time, Andy.

Chavez: Thanks for this opportunity. **DESIGN007**



Impact of Serpentine Routing on Multi-gigabit Signal Transmission

Article by Chang Fei Yee
KEYSIGHT TECHNOLOGIES

Abstract

This article discusses the impact of PCB serpentine routing on high-speed signal integrity in terms of impedance discontinuity, insertion loss and eye diagram opening and differential to common mode conversion for signal transmission at one Gbps (i.e., lower-speed grade) and 10 Gbps (i.e., higher-speed grade). This investigation is performed using Keysight ADS.

Introduction

Serpentine is a technique to minimize skew or misalignment of differential pairs [1] (Figure 1). The number of segments and intra-pair spacing of serpentining impacts the high-speed signal transmission. As the intra-pair gap is enlarged for serpentining, the characteristic impedance of the PCB trace in differential mode will rise, as governed by Equations 1 and 2 [2]. This leads to impedance discontinuity, signal reflection, and ultimately, attenuation. The signal attenuation is heavily dependant on the number of segments and intra-pair spacing of the serpentine. Besides impedance discontinuity, increasing the intra-pair spacing at serpentine segments also loosens the electromagnetic coupling within the differential signal pair, and eventually worsens the differential to common-mode conversion that weakens the immunity of the channel against common-mode noise or crosstalk.

(Equation 1)

$$Z_{DIFF}\,(\Omega) = 2 \cdot Z_0 \cdot \left(1 - 0.748 \cdot e^{-0.96\frac{s}{h}}\right) \text{ for microstrip}$$

(Equation 2)

$$Z_{DIFF}\,(\Omega) = 2 \cdot Z_0 \cdot \left(1 - 0.748 \cdot e^{-2.9\frac{s}{h}}\right) \text{ for stripline}$$

s = intra-pair spacing
h = dielectric thickness
Z_0 = PCB trace characterisric impedance in single-ended mode

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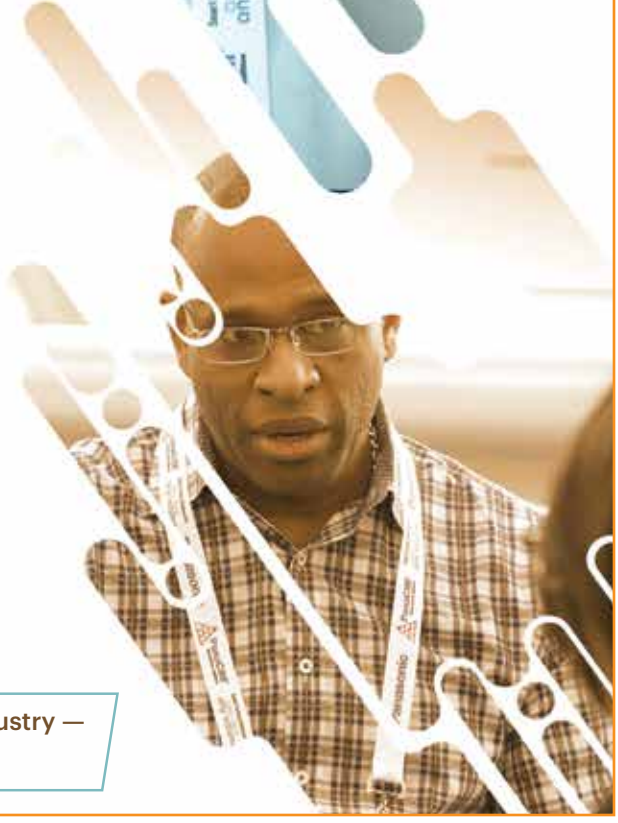

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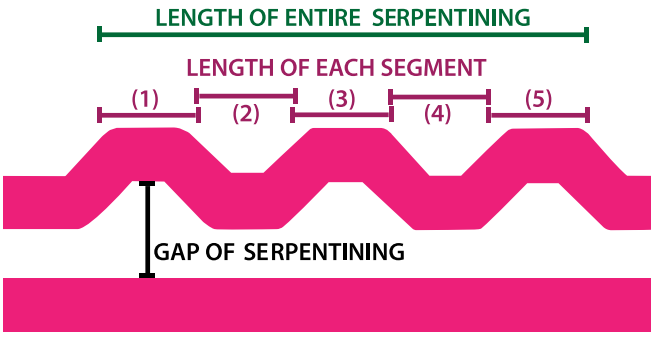

Figure 1. Top view of a serpentine on a PCB.

The impact of the number or total length of the serpentine segments and the intra-pair spacing on signal attenuation is discussed in case study 1 and 2. The analysis is performed using 2DEM simulation. The results cover time domain reflectometry (TDR), differential insertion loss (Sdd21), eye diagram, and differential to common mode conversion (Scd21).

In both case studies, simulation models involve differential pairs for microstrip and stripline with 100-ohm impedance. The microstrip pair has 1-oz. copper thickness, 6-mil trace width, and 5-mil intra-pair spacing with 4.5-mil dielectric thickness. Meanwhile, the pair of symmetrically centered striplines has 1-oz. copper thickness, 5-mil trace width, and 6-mil intra-pair spacing with 9.5-mil dielectric thickness. Medium-loss dielectric is applied as substrate. In channel analysis that generates an eye diagram, a transmitter injects a signal with an amplitude of 600 mVpp at one Gbps (i.e., with 35 ps rise/fall time) and 10 Gbps (i.e., with 5 ps rise/fall time). Pre-/de-emphasis and equalization are disabled.

Analysis and Results

A. Case Study 1

This test case investigates how the number of serpentine segments impacts the signal integrity in term of insertion loss. All the simulation models are listed in Table 1. The entire transmission channel is 5 inches long. Each particular serpentine segment is 200 mils long. For microstrip, model 1A does not have serpentine routing at all, while models 1B, 1C, and 1D have3, 5 and 9 serpentine segments. Meanwhile, for stripline, model 1G does not have serpentine routing at all, while models 1H, 1I, and 1J have 3, 5 and 9 serpentine segments. A larger number of segments contributes to the increasing length of the entire serpentine portion for the transmission line model. The models' intra-pair spacing for the serpentine segment is set as 2x the non-serpentine portion (i.e., 10 mils for microstrip and 12 mils for stripline).

Plots of TDR and Sdd21 for microstrip and stripline are shown in Figures 2 and 3. When the number of serpentine segments or its total portion length increases, more inductive impedance discontinuities are encountered by the signals. This in turn leads to the occurrence of resonant dips at 10, 30, and 50 GHz for microstrip models. The resonant dip or attenuation gets intensified with a longer total serpentine routing. A similar scenario is experienced by stripline models.

Sim model	PCB layer	Length of entire serpentine portion (in)	Total T-line (in)	Intra-pair gap for serpentine segment (mil)
1A	Microstrip	0	5	N/A
1B	Microstrip	0.6	5	10
1C	Microstrip	1	5	10
1D	Microstrip	1.8	5	10
1G	Stripline	0	5	N/A
1H	Stripline	0.6	5	12
1I	Stripline	1	5	12
1J	Stripline	1.8	5	12

Table 1: Simulation models for case study 1.

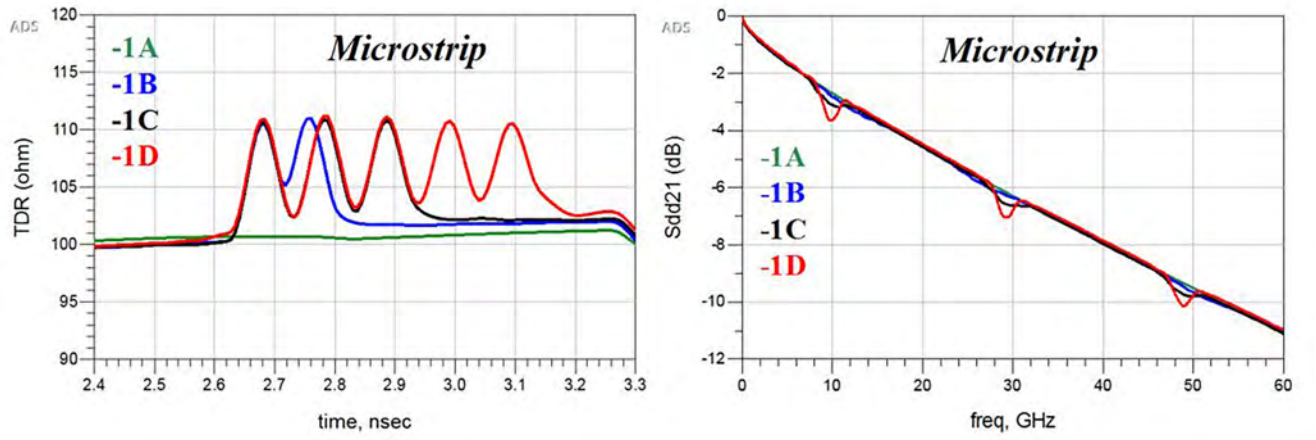

Figure 2: TDR (left) and Sdd21 (right) for microstrip.

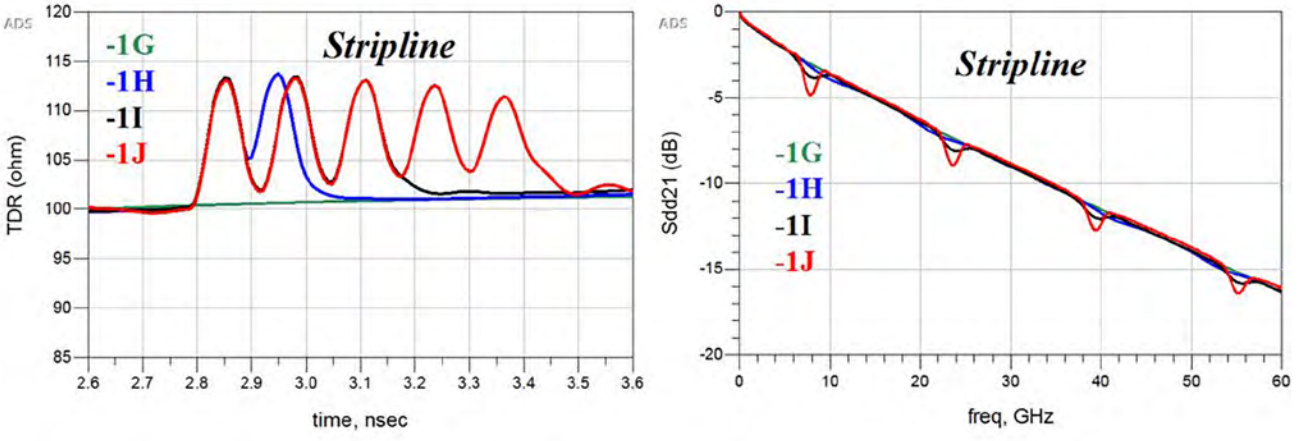

Figure 3: TDR (left) and Sdd21 (right) for stripline.

Sim model	PCB layer	Eye height (mVpp) at 1Gbps	Eye width (ps) at 1Gbps	Eye height (mVpp) at 10Gbps	Eye width (ps) at 10Gbps
1A	Microstrip	553	995	510	98.5
1B	Microstrip	553	995	486	98
1C	Microstrip	545	995	483	97.5
1D	Microstrip	537	995	475	96
1G	Stripline	553	990	511	98.5
1H	Stripline	553	990	499	97
1I	Stripline	549	990	490	96.5
1J	Stripline	541	990	467	93.5

Table 2: Results of the eye opening.

Results of the eye opening are summarized in Table 2. At the receiving end with one Gbps (i.e., lower-speed grade) transmission, besides 8% attenuation caused by dielectric loss, an additional attenuation of less than 5% is caused by 1.8 inches in total serpentine length. On the other hand, at the receiving end with 10 Gbps (i.e., higher-speed grade) transmission, besides 15% attenuation caused by dielectric loss, an additional attenuation of less than

5% is caused by the one-inch total serpentine length. With the same total serpentine length, signal transmission at 10 Gbps or higher-speed grade gets attenuated at a larger magnitude versus one Gbps or lower-speed grade.

The plots of differential to common mode conversion (Scd21) for microstrip and stripline are shown in Figure 4. A smaller absolute magnitude of Scd21 in dB indicates differential is more easily converted to common mode, which is encountered by a transmission channel with longer serpentine portion on the PCB. This weakens the immunity of the channel against common-mode noise or crosstalk.

B. Case Study 2

This test case observes how the intra-pair gap of serpentine segments impacts the signal integrity in term of insertion loss. All the simulation models are listed in Table 3. The entire transmission channel is 5 inches long. Each particular serpentine segment is 200 mils long and all models have five serpentine segments, equivalent to a one-inch total serpentine length. For microstrip, model 2A does not have serpentine routing at all, while models 2B, 2C, and 2D have intra-pair air gap of serpentine segment of 1.5x, 2x, and 3x versus non-serpentine. Meanwhile, for stripline, model 2E does not have serpentine routing at all, while models 2F, 2G, and 2H have an intra-pair air gap of serpentine segment of 1.5x, 2x, and 3x versus non-serpentine.

Plots of TDR and Sdd21 for microstrip and stripline are shown in Figures 5 and 6. When the number of serpentine segments or its

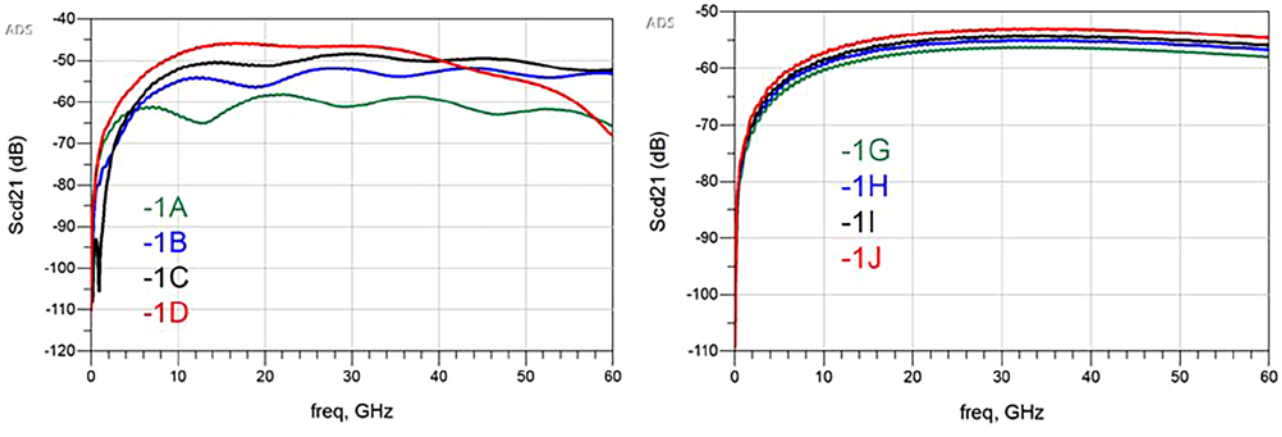

Figure 4: Scd21 for microstrip (left) and stripline (right).

Sim model	PCB layer	Length of entire serpentine portion (in)	Total T-line (in)	Intra-pair gap for serpentine segment (mil)
2A	Microstrip	N/A	5	N/A
2B	Microstrip	1	5	7.5
2C	Microstrip	1	5	10
2D	Microstrip	1	5	15
2E	Stripline	N/A	5	N/A
2F	Stripline	1	5	9
2G	Stripline	1	5	12
2H	Stripline	1	5	18

Table 3: Simulation models for case study 2.

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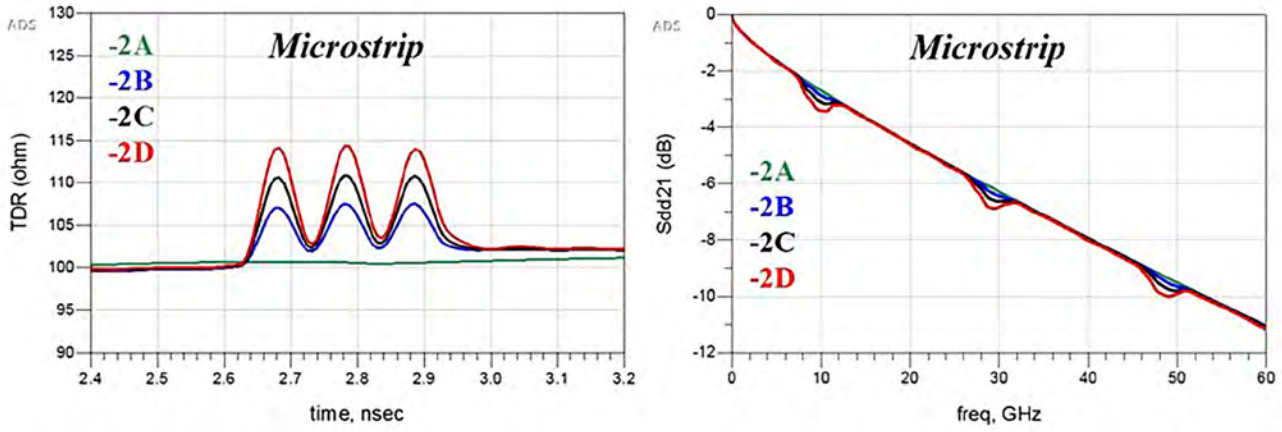


Figure 5: TDR (left) and Sdd21 (right) for stripline.

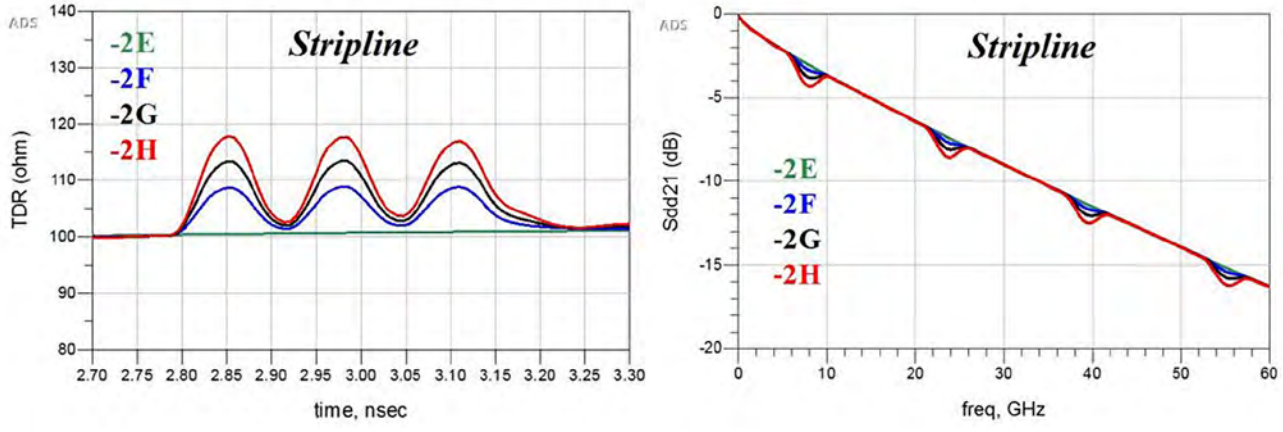


Figure 6: TDR (left) and Sdd21 (right) for stripline.

Sim model	PCB layer	Eye height (mVpp) at 1Gbps	Eye width (ps) at 1Gbps	Eye height (mVpp) at 10Gbps	Eye width (ps) at 10Gbps
2A	Microstrip	553	995	510	98.5
2B	Microstrip	549	995	499	98
2C	Microstrip	545	995	483	97.5
2D	Microstrip	541	995	479	96
2E	Stripline	553	990	511	98.5
2F	Stripline	553	990	500	98
2G	Stripline	549	990	490	96.5
2H	Stripline	539	990	474	95.5

Table 4: Results of the eye opening.

total portion length increases, more inductive impedance discontinuities are encountered by the signals. This leads to the occurrence of resonant dips at 10, 30, and 50 GHz for microstrip models. The resonant dip or attenuation becomes intensified with a larger intra-pair spacing of the serpentine segment. A similar scenario is experienced by stripline models.

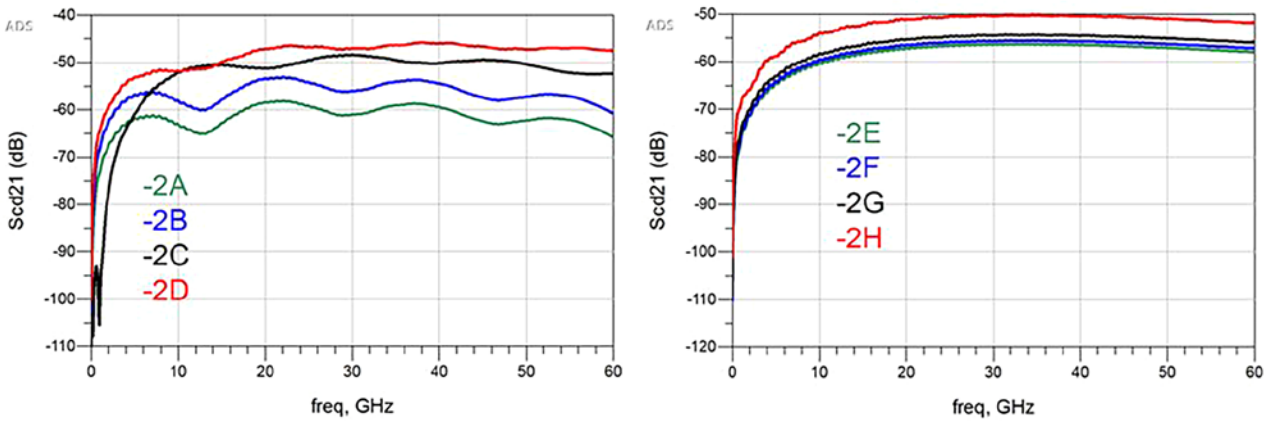


Figure 7: Scd21 for microstrip (left) and stripline (right).

Results of the eye opening are summarized in Table 4. At the receiving end with one Gbps (i.e., lower-speed grade) transmission, besides 8% attenuation caused by dielectric loss, an additional attenuation of less than 5% is caused by intra-pair spacing of the serpentine segment being triple versus non-serpentine. Meanwhile, at the receiving end with 10 Gbps (i.e., higher-speed grade) transmission, besides 15% attenuation caused by dielectric loss, an additional attenuation of less than 5% is caused by intra-pair spacing of the serpentine segment being double versus non-serpentine. With the same intra-pair spacing of the serpentine segment, signal transmission at 10 Gbps or higher-speed grade becomes attenuated at a larger magnitude versus one Gbps or lower-speed grade.

The plots of Scd21 for microstrip and stripline are shown in Figure 7. A smaller absolute magnitude of Scd21 in dB indicates more easily differential is converted to common mode, which is encountered by channel with larger intra-pair spacing in the serpentine segments. This weakens the immunity of the channel against common mode noise or crosstalk.

Summary

In PCBs with multi-gigabit signal transmission of 10 Gbps or beyond, the length of the entire serpentine portion shall be kept below 1 inch for differential transmission channel with a total 5 inches in length (i.e., not more than 20% of the total trace length). Meanwhile, the intra-pair gap of serpentine segment shall be less than 2x the non-serpentine segment intra-pair gap to minimize the impedance mismatch and channel loss. This ensures that the attenuation does not exceed 5% of the signal at receiving end without serpentine routing, to allow more head room for channel loss contributed by other factors (e.g., dielectric loss, copper surface roughness, etc.). Besides that, due to the weakened immunity of the serpentine segments against common mode noise or crosstalk, serpentine routing shall be implemented further away (i.e., a distance of at least 5x the transmission channel trace width) from the noise source (e.g., switch mode voltage regulator ICs, clock or any high toggle rate signals). **DESIGN007**

References

1. *High-Speed Interface Layout Guidelines, Embedded Processor Applications,* July 2017.

2. *Considerations for PCB Layout and Impedance Matching Design in Optical Modules* by Daniel Long, February 2011.

3. Keysight ADS guide.

Chang Fei Yee is a hardware engineer with Keysight Technologies. His responsibilities include embedded system hardware development, and signal and power integrity analysis.

Recent Highlights from Design007

1 AltiumLive 2018 a Mecca for PCB Designers ▶

The event took place in San Diego, California at the Lowes Coronado Bay Resort. Located right on the water, the venue was perfect. The attendees were provided excellent meals throughout the entire event and the views were spectacular.

2 Tim's Takeaways: Contract Positions–Go the Extra Mile ▶

For newbies just entering the industry or experienced designers who have always worked for a corporation, the transition to contractor can be a culture shock. The allure of working from home and setting your own hours can quickly be replaced by the realities of chasing jobs. However, there are some wonderful aspects of working as a contractor.

3 Artificial Intelligence: The Future of EDA? ▶

Artificial intelligence has been making inroads into a variety of industries in the past decade or so, from automobiles to medical devices. Naturally, EDA tool companies are taking a look at AI. I recently interviewed Paul Musto, director of marketing for the Board Systems Division of Mentor, about Mentor's plans for integrating AI into EDA tools, and why we may be at the very beginning of understanding the pros and cons of this new technology.

4 Mark Thompson of Prototron Circuits Publishes Book on Producing the Perfect Data Package ▶

Mark Thompson, engineering support and CID + at Prototron Circuits, sees thousands of data packages each year. Dan Beaulieu recently sat down with Thompson to find out more about his new book and discuss the quest for the perfect data package.

5 PCB West 2018 Draws a Crowd of Designers and Technologists ▶

The I-Connect007 team attended UP Media Group's PCB West 2018 Conference and Exhibition in September. I have been attending this event for many years, and every year the show is better than the year before. This year was no exception.

6 Transitioning from FR-4 to High-Frequency Materials, Revisited ▶

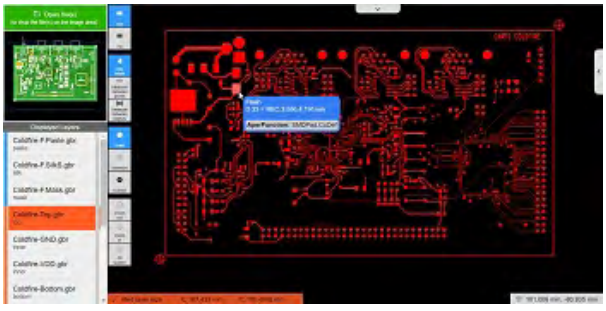
The bottom line is that FR-4 materials have been around a long time, and they work well within the range they are formulated to work. The same can be said for high-frequency circuit materials, which are also thought of as low-loss materials. However, there is a definite gray area that can muddy the waters when a designer is weighing a possible decision to switch from FR-4 to low-loss materials.

7 Samtec Releases Over 100,000 New Models on SnapEDA ▶

With this new collaboration, designers can now easily discover, download, and design with over 100,000 ready-to-use Samtec connector models, helping accelerate the design process. The new models include USB, card edge, board-to-board, headers, and RF coaxial connectors.

8 Version 2.8 of Ucamco's Free Reference Gerber Viewer Now Available ▶

"For version 2.8 of the Reference Gerber Viewer our focus was ease of use and especially ease of learning. Plenty of users of the viewer need it only from time to time, and for them it is of paramount importance that it is very intuitive," said Peter Vermeulen, lead developer of the Reference Gerber Viewer.



9 Zuken to Hold Fall Webinar Series ▶

Zuken's Fall Webinar Series will run from September 2018 through March 2019. The company will be covering a wide range of topics from Silicon Expert to E3.series MCAD co-design.

10 Mentor Xpedition and PADS Professional Win ISO 26262 Functional Safety Compliance ▶

Mentor's Xpedition and PADS Professional printed circuit board design (PCB) design flows, including the Valor NPI and HyperLynx family of products, have each achieved ISO 26262 functional safety compliance.

Career Opportunities

Pssst! Are You Looking for Someone?

Place your notice in our Help Wanted section.

For just $500, your 200 word, full-column—or, for $250, your 100 word, half-column—ad will appear in the Help Wanted section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs and suppliers.

Potential candidates can click on your ad and submit a résumé directly to the email address you've provided. If you wish to continue beyond the first month, the price is the same per month. No contract required. We even include your logo in the ad, which is great branding!

To get your ad into the next issue, contact:
Barb Hockaday at barb@iconnect007.com or +1.916.608.0660 (-7 GMT)

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GOOD FOR THE INDUSTRY

smt007 pcb007 pcb design007

Career Opportunities

PCB DFM Engineer

Apple products are as alluring on the inside as they are on the outside. Inside our products are some of the world's most challenging consumer PCB assembly and flex designs. Imagine yourself as a select member of the team that brings these assemblies from concept to high-volume manufacturing.

Key Qualifications

- At least 5 years of experience with printed circuits, including hands-on process engineering experience
- Creativity and curiosity about materials science and electronics packaging at all levels
- Deep knowledge of industry specifications, especially IPC and JEDEC specifications
- Understanding of the relationship between manufacturing processes and printed circuit defect conditions, especially latent defects
- Ability to travel overseas for up to 25 percent of your time

Primary Responsibilities

- Maintenance of PCB design guidelines for all Apple products as well as the technology road map and acceptability specifications
- Establishment and maintenance of the supplier site/material/technology qualification matrix
- Direct responsibility for all PCB-related quality issues and excursions
- Providing mentorship to product designers on available PCB technologies and materials

Education

BS or higher in Materials Science or Mechanical, Chemical, or Electrical Engineering

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Senior Manager, Flex/PCBA DFM

On this team, you'll be responsible for new product development, sustaining products and failure analysis while leading and mentoring design, process, and quality engineers and managers. You'll collaborate cross-functionally with Product Design, Electrical Engineering, strategic suppliers, and contract manufacturers to ensure the manufacturability of Apple products and maintain Apple's high standards for quality.

Key Qualifications

- At least 10 years of experience, with 5+ years of experience as a senior manager or director
- Experience managing other managers is preferable
- Experience in design and manufacturing, preferably in the electronics fabrication and assembly industry
- Deep technical knowledge complemented by a good sense of how engineering decisions impact business concerns
- Excellent communication skills, from extemporaneous discussion to synthesis of detailed technical reports and distillation to executive-level presentation

Primary Responsibilities

- Development of several design engineers and first-level managers
- Primary escalation point to resolve blocking issues related to design release, design spec compliance, or production process problems
- Engagement with vendor senior management to set expectations and to communicate feedback
- Highlighting all project risks to executive management and identifying, evaluating, and recommending the best path to resolution

Education

BS or higher in Materials Science or Mechanical, Chemical, Electrical, or Industrial Engineering

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Career Opportunities

FREEDOM CAD SERVICES

Sr. PCB Designer – Allegro

Freedom CAD is a premier PCB design service bureau with a talented team of 30+ dedicated designers providing complex layouts for our enviable list of high-tech customers. Tired of the commute? This is a work-from-home, full-time position with an opportunity for overtime at time and a half.

Key Qualifications

- EXPERT knowledge of Allegro 16.6/17.2
- Passionate about your PCB design career
- Skilled at HDI technology
- Extensive experience with high-speed digital, RF and flex and rigid-flex designs
- Experienced with signal integrity design constraints encompassing differential pairs, impedance control, high speed, EMI, and ESD
- Experience using SKILL script automation such as dalTools
- Excellent team player that can lead projects and mentor others
- Self-motivated, with ability to work from home with minimal supervision
- Strong communication, interpersonal, analytical, and problem solving skills
- Other design tool knowledge is considered a plus (Altium, PADS, Xpedition)

Primary Responsibilities

- Design project leader
- Lead highly complex layouts while ensuring quality, efficiency and manufacturability
- Handle multiple tasks and provide work leadership to other designers through the distribution, coordination, and management of the assigned work load
- Ability to create from engineering inputs: board mechanical profiles, board fabrication stack-ups, detailed board fabrication drawings and packages, assembly drawings, assembly notes, etc.

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American Standard Circuits
Creative Innovations In Flex, Digital & Microwave Circuits

CAM Operator

American Standard Circuits is seeking a CAM Operator for its Phoenix, Ariz., office. Qualified applicants will need experience in using Valor/Genesis (GenFlex) CAD/CAM software with printed circuit board process knowledge to edit electronic data in support of customer and production needs.

Job Requirements:

- At least 5 years' experience in PCB manufacturing
- Process DRC / DFMs and distinguish valid design and manufacturing concerns.
- Modify customer supplied data files and interface with customers and engineers
- Responsible for releasing manufacturing tooling to the production floor
- Prepare NC tooling for machine drilling, routing, imaging, soldermask, silkscreen
- Netlist test, optical inspection
- Work with Production on needed changes
- Suggestions on continual improvements for engineering and processing.
- Be able to read write and communicate in English
- Must understand prints specifications
- Must be US Citizen or permanent resident (ITAR)
- High School Graduate or equivalent

Join our Team!

Founded in 1988, American Standard Circuits is a leading manufacturer of advanced circuit board solutions worldwide. Our ongoing commitment to leading-edge higher-level interconnect technology, cost-effective manufacturing and unparalleled customer service has put us at the forefront of advanced technology circuit board fabrication.

We manufacture quality rigid, metal-backed and flex printed circuit boards on various types of substrates for many applications.

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Career Opportunities

ELECTROLUBE
THE SOLUTIONS PEOPLE

We Are Recruiting!

A fantastic opportunity has arisen within Electrolube, a progressive global electro-chemicals manufacturer. This prestigious new role is for a sales development manager with a strong technical sales background (electro-chemicals industry desirable) and great commercial awareness. The key focus of this role is to increase profitable sales of the Electrolube brand within the Midwest area of the United States; this is to be achieved via a strategic program of major account development and progression of new accounts/projects. Monitoring of competitor activity and recognition of new opportunities are also integral to this challenging role. Full product training to be provided.

The successful candidate will benefit from a generous package and report directly to the U.S. general manager.

Applicants should apply with their CV to
melanie.latham@hkw.co.uk
(agencies welcome)

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Ucamco
Former Barco ETS

International Field Service Engineer located in ITALY

The successful candidate will:

- Install and service our plotters and direct imaging machines at customer sites Europe-wide
- Carry out maintenance in the field
- Frequent travel: 4 to 5 days a week, 3 to 4 weeks a month
- Assist product manager

We are looking for a team player who is:

- Strongly customer-oriented and experienced in on-site support
- Accustomed to travel, and willing to travel frequently
- Motivated, independent and enterprising
- Technically-minded with training/background in electromechanics/electronics
- Experienced with software (setup, configuration, and usage of Windows-based CAM front-end software and Linux-based RIP software)
- Fluent in Italian and English (German and/or French is a plus)
- An analytical thinker
- Capable of problem solving

The right candidate will be a valued member of a friendly, team-oriented, growing international company that is a leader in its field, dedicated to excellence in all it does. Dynamic and fun, the company offers a great working atmosphere, and this new position is forward-looking and open, with plenty of opportunities for enterprising individuals whose results could be rewarded with prospects for progression in technical development.

Apply to Anja Ingels after clicking below.

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Career Opportunities

MacDermid Enthone
ELECTRONICS SOLUTIONS

Product Group Field Manager
Waterbury, CT

Do you have what it takes? MacDermid Enthone Electronics Solutions is a leading supplier of specialty chemicals, providing application-specific solutions and unsurpassed technical support.

The position of the Product Group Field Manager will be responsible for creating and driving a strategic plan for the regional product line, including the following:

- Possess a thorough understanding of the overall PCB business, and specifics in wet processing areas
- Play an integral part in developing a commercial and technical customer strategy
- Create and deliver customer facing presentations
- Provide technical training for field staff
- Create and execute a product rationalization program
- Develop new product roll-out packages

Hiring Profile

- Bachelor's degree or 5 years' job-related experience
- Strong understanding of chemistry and chemical interaction within PCB manufacturing
- Excellent written and oral communication skills
- Strong track record of navigating technically through complex organizations
- Willingness to travel

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GO Gardien

Role: Vice President Gardien Taiwan
TAOYUAN COUNTY, TAIWAN

Gardien Taiwan is a service provider of circuit board (PCB) quality solutions, including electrical testing, AOI optical inspection, engineering (CAM), fixture making, repair and rework. Gardien Taiwan operates service centers in Taoyuan and employs about 100 employees and is currently seeking a vice president to manage and oversee the entity.

Candidate Profile:

- Proficiency in Chinese and English (written and spoken)
- Excellent communication and organization skills
- Experience in change management
- PCB background appreciated, but not mandatory
- Management experience in internationally operating companies
- Savvy in standard office software (Word, Excel and Power Point)

If this sounds like you, please click here to send us an email with your attached CV.

About Gardien Group - Gardien is the world's largest international provider of independent testing and QA solutions to the PCB industry with a global footprint across 24 service centres in five countries and we cater to a whole range of customers, from small family owned PCB shops to large international fabricators. Gardien's quality solutions and process standards are trusted by leading high-tech manufacturers and important industries including aerospace, defense, and medical technology.

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Career Opportunities

ZENTECH

Zentech Manufacturing: Hiring Multiple Positions

Are you looking to excel in your career and grow professionally in a thriving business? Zentech, established in Baltimore, Maryland, in 1998, has proven to be one of the premier electronics contract manufacturers in the U.S.

Zentech is rapidly growing and seeking to add Manufacturing Engineers, Program Managers, and Sr. Test Technicians. Offering an excellent benefit package including health/dental insurance and an employer-matched 401k program, Zentech holds the ultimate set of certifications relating to the manufacture of mission-critical printed circuit card assemblies, including: ISO:9001, AS9100, DD2345, and ISO 13485.

Zentech is an IPC Trusted Source QML and ITAR registered. U.S. citizens only need apply.

Please email resume below.

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Manncorp™

Sales Associate - Mexico

Manncorp, a leader in the electronics assembly industry for over 50 years, is looking for an additional sales associate to cover all of Mexico and to be part of a collaborative, tight-knit team. We offer on-the-job training and years of industry experience in order to set up our sales associate for success. This individual will be a key part of the sales cycle and be heavily involved with the customers and the sales manager.

Job responsibilities:

- Acquire new customers by reaching out to leads
- Ascertain customer's purchase needs
- Assist in resolving customer complaints and queries
- Meet deadlines and financial goal minimums
- Make recommendations to the customer
- Maintain documentation of customer communication, contact and account updates

Job requirements:

- Located in Mexico
- Knowledge of pick-and-place and electronics assembly in general
- 3+ years of sales experience
- Customer service skills
- Positive attitude
- Self-starter with ability to work with little supervision
- Phone, email, and chat communication skills
- Persuasion, negotiation, and closing skills

We offer:

- Competitive salary
- Generous commission structure

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Career Opportunities

Mentor®
A Siemens Business

PCB Manufacturing, Marketing Engineer

Use your knowledge of PCB assembly and process engineering to promote Mentor's Valor digital manufacturing solutions via industry articles, industry events, blogs, and relevant social networking sites. The Valor division is seeking a seasoned professional who has operated within the PCB manufacturing industry to be a leading voice in advocating our solutions through a variety of marketing platforms including digital, media, trade show, conferences, and forums.

The successful candidate is expected to have solid experience within the PCB assembly industry and the ability to represent the Valor solutions with authority and credibility. A solid background in PCB Process Engineering or Quality management to leverage in day-to-day activities is preferred. The candidate should be a good "storyteller" who can develop relatable content in an interesting and compelling manner, and who is comfortable in presenting in public as well as engaging in on-line forums; should have solid experience with professional social platforms such as LinkedIn.

Success will be measured quantitatively in terms of number of interactions, increase in digital engagements, measurement of sentiment, article placements, presentations delivered. Qualitatively, success will be measured by feedback from colleagues and relevant industry players.

This is an excellent opportunity for an industry professional who has a passion for marketing and public presentation.

Location flexible: Israel, UK or US

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BLACKFOX
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This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

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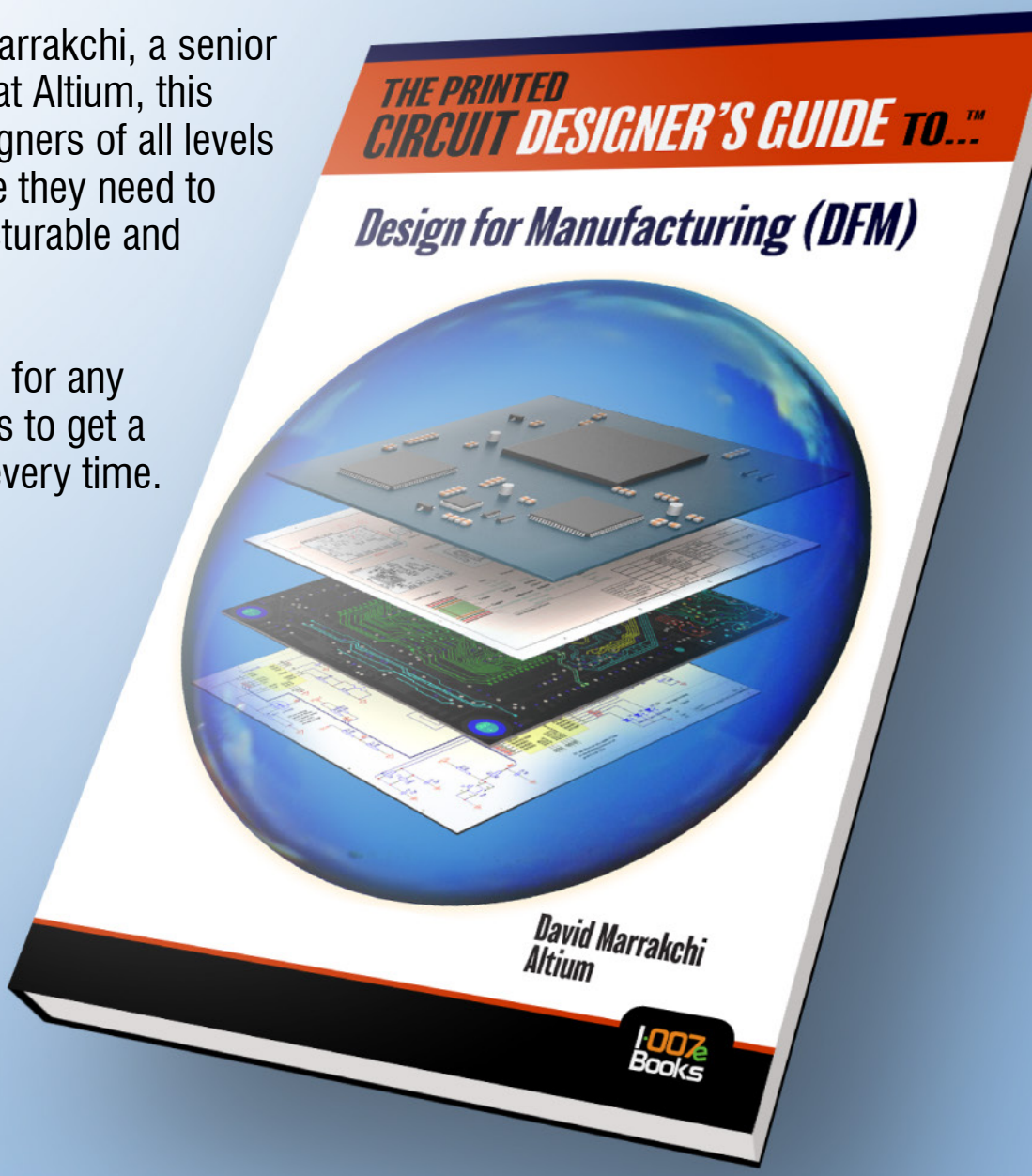
“A guided tour through the entire DFM process.”

Kelly Dack
CID+, CIT, EPTAC Corporation

Written by David Marrakchi, a senior technical engineer at Altium, this book provides designers of all levels the DFM knowledge they need to produce a manufacturable and functional board.

This is a must-read for any designer who wants to get a good board back, every time.



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International Wafer-Level Packaging Conference Exhibition ▶
October 23–24, 2018
San Jose, California, USA

IMPACT 2018 ▶
October 24–26, 2018
Taipei, Taiwan

Medical Design & Manufacturing (MD&M) Minneapolis ▶
October 31–November 1, 2018
Minneapolis, Minnesota, USA

IPC Southeast Asia High Reliability Conferences 2018 ▶
November 1, 2018
Penang, Malaysia

PCB Carolina ▶
November 7, 2018
Raleigh, North Carolina, USA

IPC/SMTA High-Reliability Cleaning and Conformal Coating Conference ▶
November 13–15, 2018
Schaumburg, Illinois, USA

electronica 2018 ▶
November 13–16, 2018
Munich, Germany

International Printed Circuit & APEX South China Fair ▶
December 5–7, 2018
Shenzhen, China

DesignCon 2019 ▶
January 29–31, 2019
Santa Clara, California, USA

IPC APEX EXPO 2019 ▶
January 26–31, 2019
San Diego, California, USA

Additional Event Calendars

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