THE pcb design MAGAZINE

October 2014

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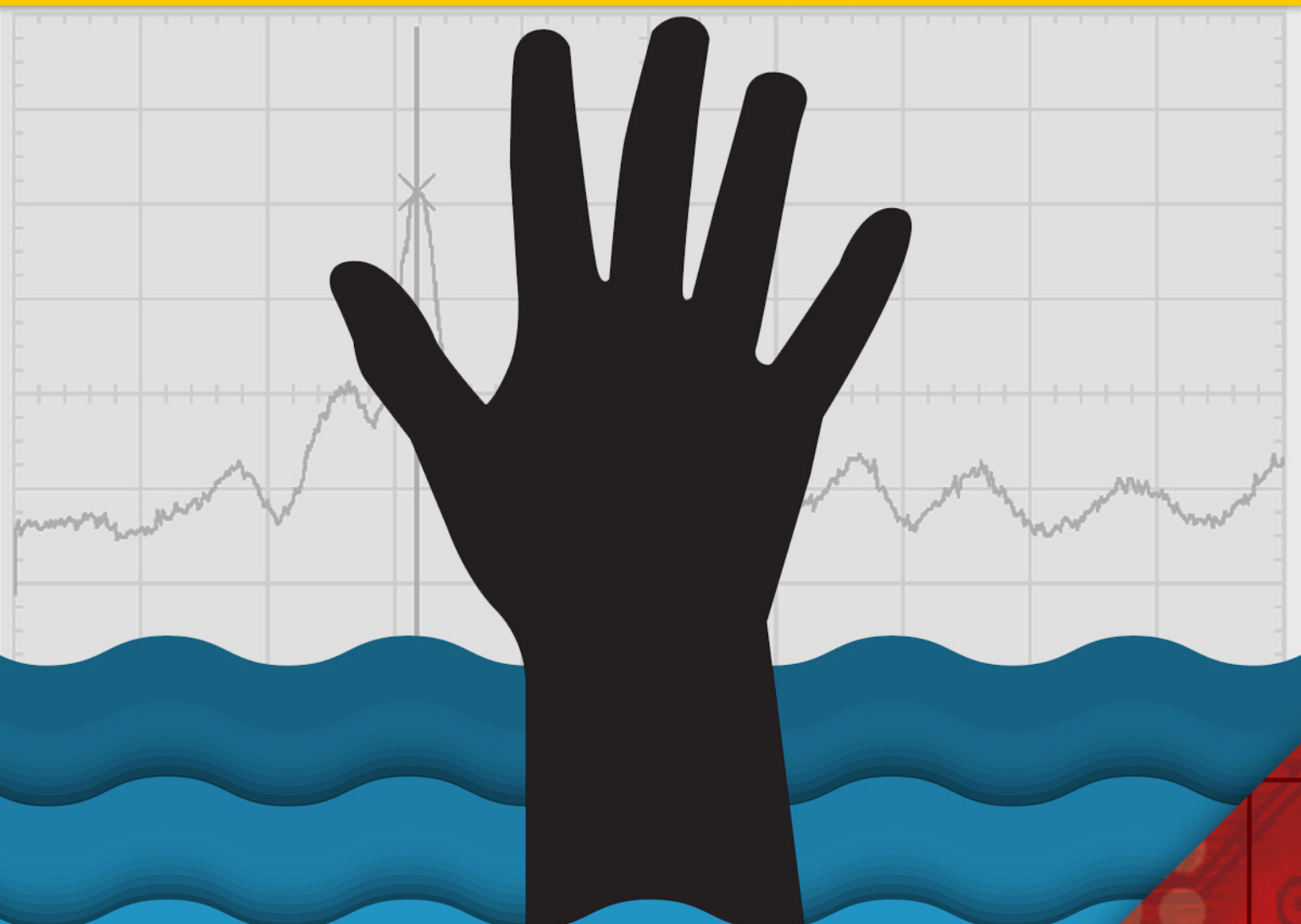
Signal Integrity, Part 1 of 3
by Barry Olney p.24

ALSO:

Thermal Characterization of LEDs: Enabling the Upcoming Lighting Revolution
by Dr. John Parry p.34

SIGNAL INTEGRITY



Sink or Swim at 28 Gbps

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THE pcb design MAGAZINE™
October 2014

This Issue: SIGNAL INTEGRITY

FEATURED CONTENT

Gone are the days when signal integrity was just a problem for the EE; if you don't already have signal integrity problems, you certainly will. In this issue, Yuriy Shlepnev and Barry Olney offer some of the latest SI tips, tricks and techniques for achieving signal integrity. We'll also feature columns by Charles Pfeil, John Coonrod, Tim Haag, Bob Tarzwell and Dan Beaulieu, and an article on Thermal Characterization of LEDs by John Parry of Mentor Graphics.

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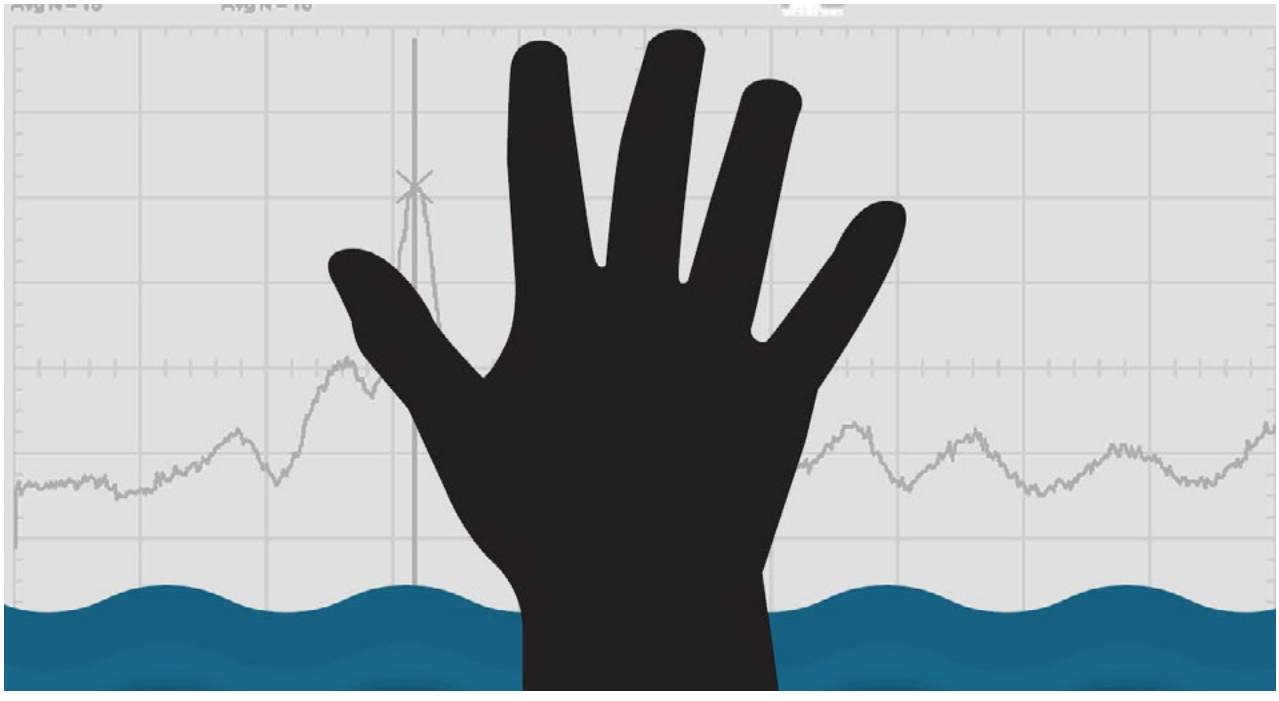

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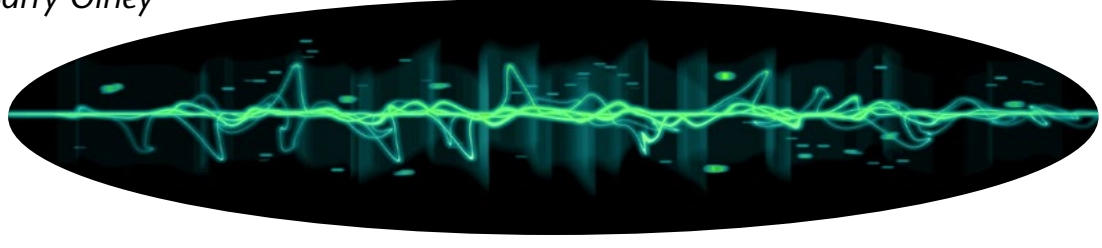

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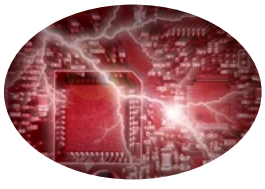

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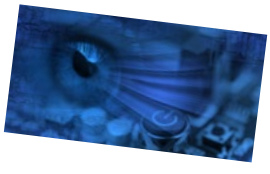

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So You Want to Write an Article!

by Andy Shaughnessy
I-CONNECT007

As a journalist and editor, I can't imagine a better beat to cover than PCB design and EDA. This is the perfect career for me. I come armed with an English degree. I studied Chaucer and Shakespeare for years to prepare myself for through-holes and fanout routing.

"I bear a charmed life," as Macbeth put it. But it's people like you who write the fantastic articles and columns that make our publications great. We'd be nowhere without these wonderful writers who sacrifice their nights and weekends putting their thoughts on paper.

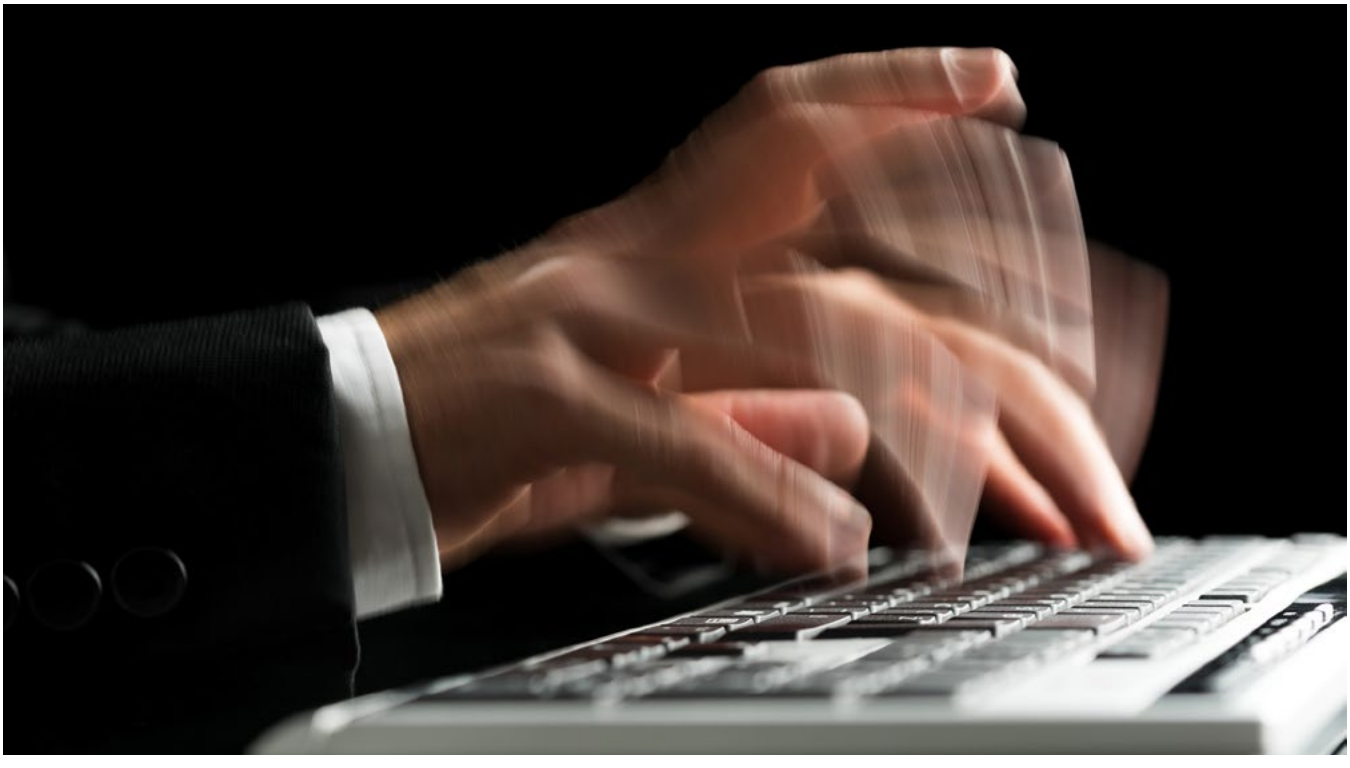
That said, this month I'm going to offer a few tips for anyone considering writing articles or contributing press releases to this magazine, or any B2B pub, for that matter.

Spell Check is Your Friend

We try to leave your copy as untouched as possible. We want your particular tone to shine through. But we also want all of our magazines to adhere to the same style. We follow the Associated Press style for the most part, but AP doesn't cover certain terms, such as microvia vs micro via vs micro-via. (We've settled on microvia, since that's how most of the industry spells it.)

Our writers keep us on our toes. Some of our contributors capitalize words for no reason, such as High-Density Interconnect. That's not a proper name, so it doesn't need to be capped. Other writers only capitalize every Noun, as if we were speaking high German. And beware the writer who has—recently—discovered the dash; the same holds true for the semicolon. It could be great stuff; then again, it might be trouble.

And some articles have obviously never been run through spell check. I use spell check, and so should you. It won't catch your use of "threw" instead of "through," but it will catch the biggest snafus, and it highlights sentences that are unclearly worded.



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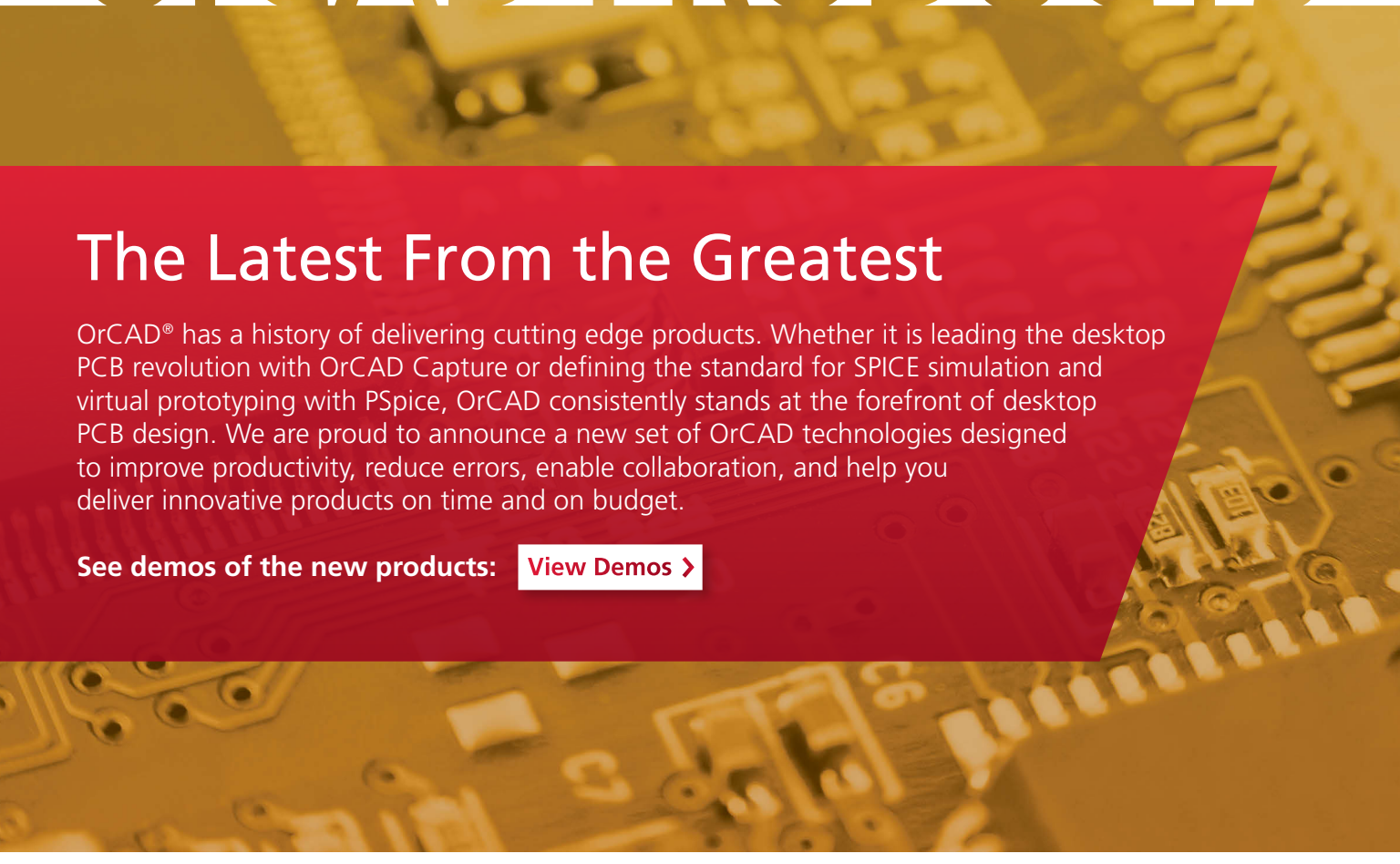

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SO YOU WANT TO WRITE AN ARTICLE! *continues*

Have a Plan Before You Begin

If you're brave enough to submit an article, congratulations. We salute you! We won't get very far without good, solid content.

Before you begin, read some similar articles in the magazine you're submitting to, and develop a good understanding about the mag's audience. I've gotten articles from PR managers who have obviously never read my magazine. Our audience doesn't design ICs, but I still get articles about how to use the latest synthesis compiler to great advantage.

Sketch out a basic outline before you start writing your article. Take a few minutes to decide what you're trying to say. Why are you saying it? Is it important to a PCB designer, in our case? What will the reader learn?

Avoid Marketing Copy

It may sound counterintuitive, but it's true: You're more likely to generate leads for your company if you keep marketing copy out of your article. If you find yourself mentioning your company's "industry-leading software that easily and simply allows designers to simulate the most complex high-speed designs," you've become a marketing guy (or girl).

> ***Marketing buried in an article makes readers angry, especially designers, because they're being marketed to constantly anyway. They expect our technical articles to be free of marketing spiels. They'll send me hate mail and they'll be mad at you and your company, and they won't forward your article to their friends.***

This is for your benefit, and mine. Marketing buried in an article makes readers angry, especially designers, because they're being marketed to constantly anyway. They expect our technical articles to be free of marketing spiels. They'll send me hate mail and they'll be mad at you and your company, and they won't forward your article to their friends.

I'm going to edit out all the marketing copy, though we do allow one mention of a company or tool as an example in the article. But you're much better off focusing on telling a story about laying out the board, performing EMC measurement, or describing the return of outsourced designs from Asia, and keeping the marketing out.

When in doubt, remember: Cover the process, not the tools or services.

We Love Case Studies, But...

Case studies offer some of the best content around. A good case study explains how a company or department solved a major technical problem that was costing them time and money. But I doubt we've run more than a handful in the past five years. Why?

Too often, the case study is just a big ad for a software tool or board shop. An EDA company or board shops asks a customer to write a case study, and it arrives in my inbox. The article reads great, for a while. Then, towards the end, when the future of the republic hangs in the balance, the customer buys the newest rev of an EDA tool, or sends his design to Fabricator XYZ, and their problems disappear into the vapor. All that's missing is a farmer shouting, "Hallelujah! Call the bank, Ma! We don't have to sell the farm after all!"

No, a case study is about much more than making the right tool purchase or picking the right board shop, though that may be one small part of the story. In a case study, readers want the dirty details. They want to hear about the process itself and all the attendant problems.

What were some of the problems you had before making this transition? What were some of the challenges to implementing this new process? What mistakes did you make? (That's a big plus.) Did you form different teams and divide the work? How did you assign members to the teams? How often did you meet to compare notes?

I'd love to run more case studies, so keep them in mind.

Precise, But Concise

As the Bard said, "Brevity is the soul of wit." This means saying all that you need to say, and in as few words possible.

Keep it concise and precise. Say what you need to say, and stop writing. Here are a few slightly exaggerated composites of sentences I've seen.

- The challenges PCB designers and engineers face are often challenging to PCB designers and engineers.
- Smaller North American printed circuit board fabricators and medium-sized North American printed circuit board fabricators can often learn from larger North American printed circuit board fabricators.
- The industry's problems can be very, very problematic.
- Your department will never have a proper process in place unless you create a process.

These sound silly, don't they? But I see this kind of thing every so often. If you're in doubt, read your complete draft out loud. Or have your spouse read it; many of our contributors utilize their spouses for copy editing. If your wife is like my exes, she won't mind telling you that you've made a mistake or two.

The "So What?" Test

Once you're finished writing, the "So what?" test comes into play. Think about it: if a designer reads your article, is he likely to say, "So what? Every designer knows that."

Or will a designer say, "Wow, I didn't know that. This guy is quite intelligent, and he really keeps his thumb on the pulse of the industry. I'll read his stuff every time. I'll consider his company the next time I need new software, fabrication, or design services, or whatever his company offers."

Obviously, you can't write about a technological breakthrough in every article. But you don't have to. The good thing about designers is that you all have a different take on every subject.

In our case, we love columns, first-person screeds that allow (require, actually) the writer to share his personal feelings on the topic. Putting yourself into the story gets other designers interested. There's an old saying in journalism: People like reading about other people. Talk about how you overcame a certain hurdle. Explain how you had a problem fanning out from a monster BGA, but you won the day by doing this, this, and this. Readers like a good story about trials and tribulations. Give it to them.

Press Release 101

We post dozens of news stories each day, most of which arrive as press releases. If you're sending a press release to the media, don't forget to include times, dates, prices, and other relevant information. I still get PRs lacking these items.

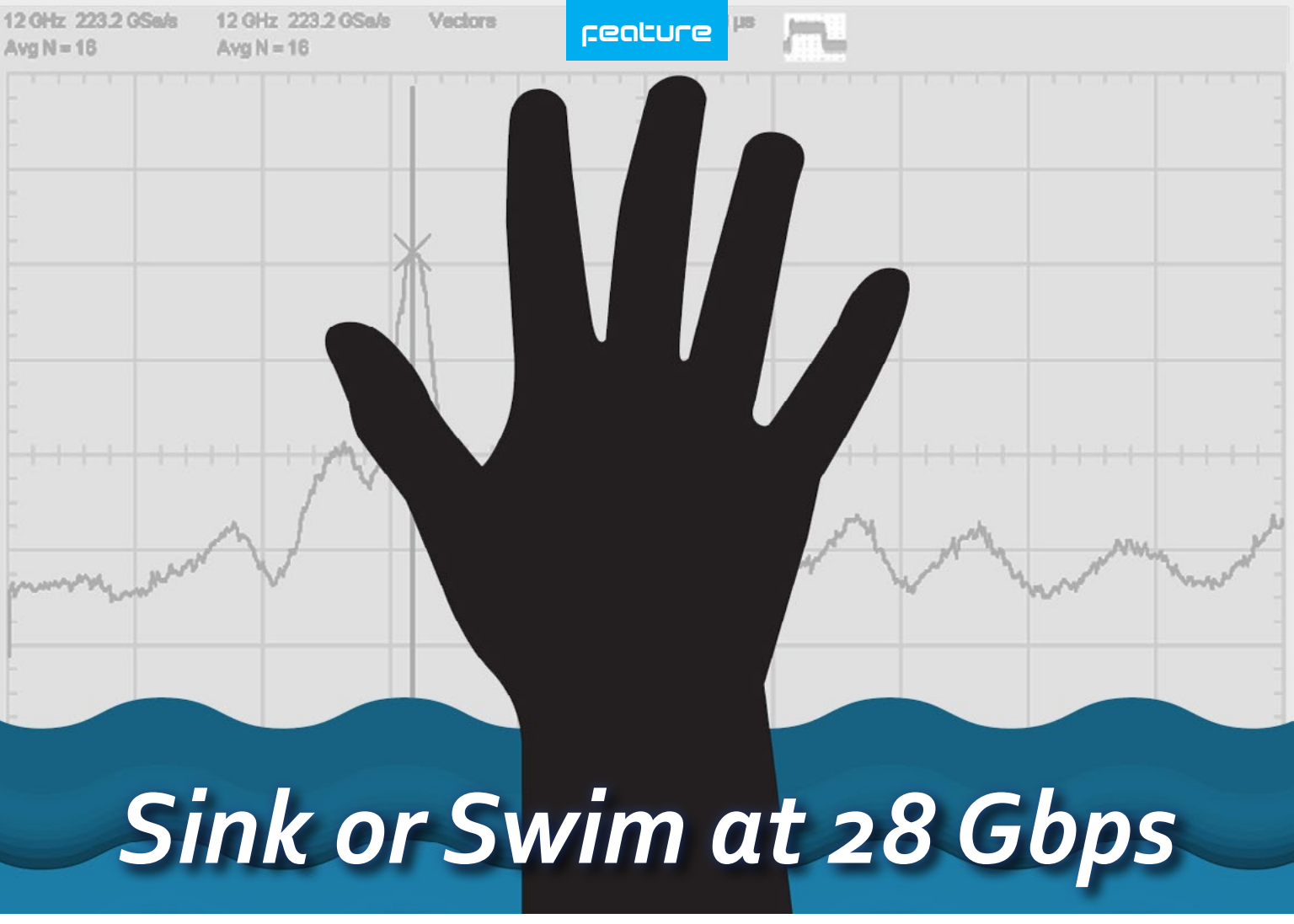
Remember: Send press releases whenever you do anything, and I mean anything. Some of the larger EDA companies send out a PR if they hire a new janitor, and that's fine. I'd rather have too many press releases to choose from than too few.

Released a new product? Hired a new designer, EE, or sales manager? That's a PR. And think of it this way: You didn't just hire a new designer. No, your company is in a growth period, and the constant stream of new customers has made it imperative that you expand your staff. That new product is the first of many as you lead the industry into the future, etc.

For a good PR, give a summary of the news in the first paragraph. This should be followed by a quote from the CEO or CTO about how great this news is for you and your customers. (As I said, people love people, and press releases with quotes get more hits than those without quotes.) Finally, the last few paragraphs break down the details of the new tool or new hire. Don't forget an "About the Company" tagline at the end, including a company URL.

I hope this helps those of you considering writing for us. We'd love to have you on board. If you have any questions, give me a shout. See you next month! **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 15 years. He can be reached by clicking here.



Sink or Swim at 28 Gbps

by Yuriy Shlepnev
SIMBERIAN INC.

Abstract

How do you know that your signal integrity software is qualified for the analysis of interconnects with signals running at 28–32 Gbps? The software vendor told you so? How does the vendor know? Most of the time, it is a "sink or swim" situation for the SI software user. One way to figure it out is to use a validation platform, such as Wild River Technology's CMP-28/32 Channel Modeling Platform, which provides interconnect structures specifically designed to benchmark the signal integrity software at these data rates. Just run the post-layout analysis of interconnects on the validation platform and compare with the pre-qualified measurements taken by an expert up to 50 GHz. The validation process may be that simple in general, but some peculiarities are discussed in this article.

Introduction

Design of PCB and packaging interconnects for data links running at 28–32 Gbps bitrates and beyond is a challenging problem, to say the least. It requires accurate electromagnetic analysis over extremely broad frequency bandwidth from DC to 40–50 GHz. What complicates it further is the absence of the broadband frequency-continuous dielectric and conductor roughness models. In addition, the final board is not usually manufactured as designed due to uncontrolled variations and manipulations by the board manufacturers to "dial in the impedance."

It is also extremely difficult to make high-quality measurements up to 50 GHz. So is it possible to design and manufacture interconnects and have acceptable analysis-to-measurement correlation up to 40–50 GHz systematically? To answer, four necessary elements for design success were formulated [1]. One of the elements is systematic benchmarking of manufacturing, measurement, and the software. Systematic in

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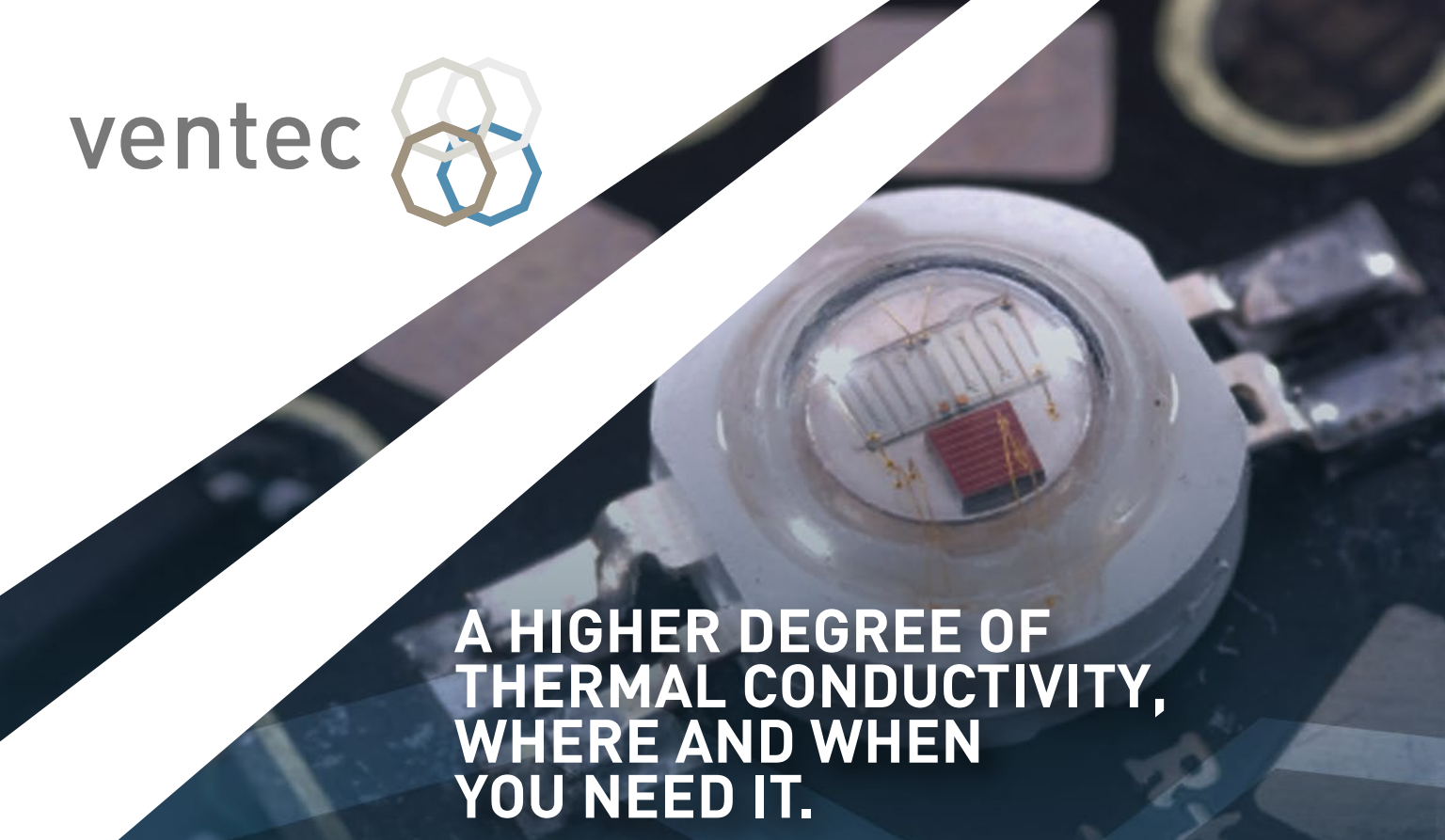

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VT-4A2	2.2W/m.K.	✔			
VT-4B1	1.0W/m.K.	✔	✔	✔	✔
VT-4B3	3.0W/m.K.	✔	✔	✔	✔
VT-4B5	4.2W/m.K.	✔	✔	✔	✔
VT-4B7	6.5W/m.K.	✔	✔	✔	✔

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this context means analysis-to-measurement correlation is observed, not just for one or two structures (test coupons for instance), but rather for a broad range of typical interconnects: single-ended and differential, stripline and microstrip, simple planar and with the vertical transitions or vias, etc.

Such comparison should be done consistently both in frequency (magnitude and phase of S-parameters) and time (TDR and eye diagram) domains. In other words, the systematic validation or benchmarking is needed to make sure that the board is manufactured as designed, measurements are taken properly and, finally, that the interconnect analysis software provides acceptable accuracy. It is a whale of a project, if you do it yourself from scratch. Though, the process can be facilitated if you start with a readily available validation platform such as CMP-28/32 from Wild River Technology [2]. The platform was designed to illustrate and facilitate systematic analysis-to-measurement validation process at 28–32 Gbps and to demonstrate that interconnects for 28–32 Gbps can be predictably designed. Use of such a platform saves time and lowers the risks by benchmarking against known and already measured and simulated structures. The CMP-28 platform [2] and Simbeor electromagnetic signal integrity software [3] are used here to illustrate signal integrity software validation process for 28 Gbps interconnects. The validation process can be divided into three steps:

1. Measure S-parameters with VNA up to 50 GHz and qualify them with formal quality metrics and, optionally, compare with S-parameters measured by an expert.

2. Identify or confirm broadband dielectric and conductor roughness models.

3. Simulate all test structures with the identified material models and verified board design adjustments and compare with the measured data in frequency and time domains.

> ***The CMP-28/32 platform contains multiple single-ended and differential line segments, suitable for identification or confirmation of material models, and also serve as the simplest validation structures. It also contains practical stripline and microstrip link paths with vias and crosstalk.***

Validation platform

A validation platform is a very important tool for signal integrity software benchmarking or formal pre-qualification. Accuracy and limitations of the software can be easily identified with the analysis to measurement comparisons on a typical set of interconnect structures. A validation platform can be either developed in-house or purchased from a vendor. One of the industry-first validation platforms was the physical layer reference design board (PLRD-1) from Teraspeed Consulting Group [4]. Use of the PLRD-1 revealed the need and enabled development of the industry-first broadband dielectric and conductor roughness models in Simbeor software. Another example of validation platform is the CMP-28/32 channel modeling platform from Wild River Technology [2]. Both CMP-28 and 32 versions contain 27 microstrip and stripline interconnect structures. All structures are equipped with either 2.92 mm (CMP-28) or 2.4 mm (CMP-32) connectors to facilitate accurate measurements with a VNA. The CMP-28/32 platform is shown in Figure 1 and will be used here to demonstrate the systematic approach to the analysis to measurement correlation.

The CMP-28/32 platform contains multiple single-ended and differential line segments, suitable for identification or confirmation of material models, and also serve as the simplest validation structures. It also contains practical stripline and microstrip link paths with vias and crosstalk. In addition, it has a set of resonant structures to validate analysis of t-lines with different widths and do validation for highly reflective interconnects [2, 5].

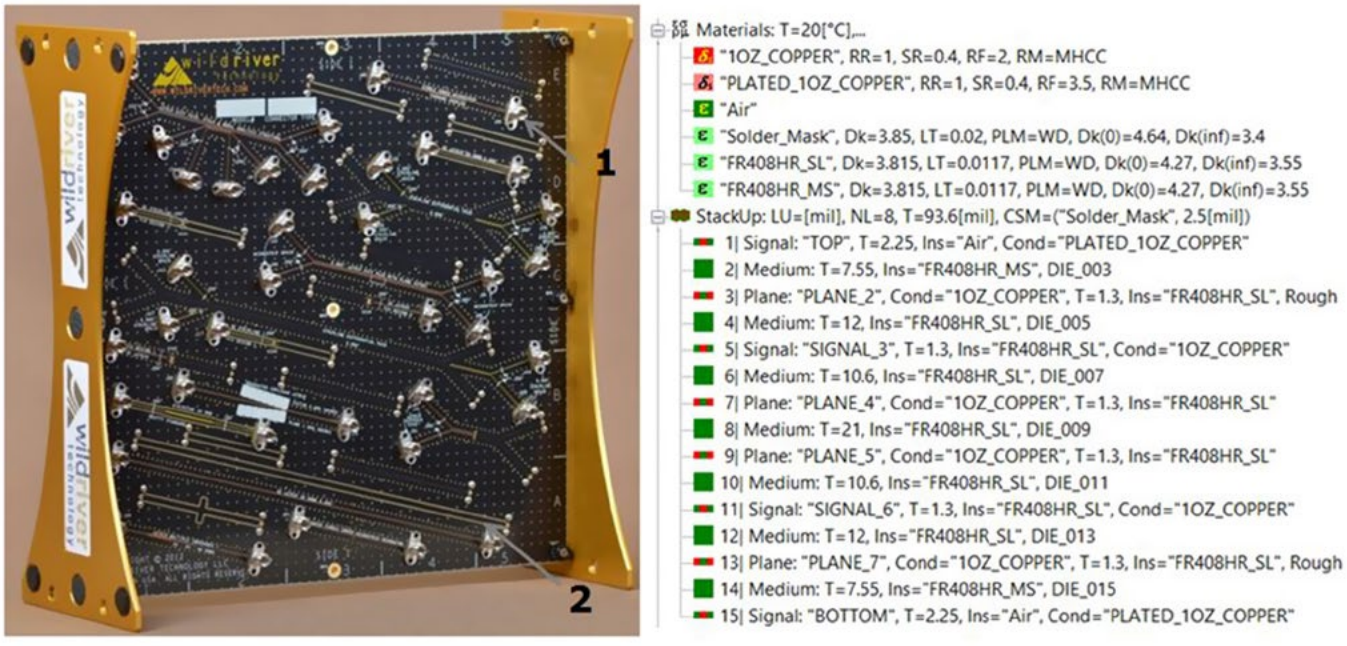

Figure 1: CMP-28/32 channel modeling platform with 27 structures to benchmark software with stack-up and broadband dielectric and conductor roughness models identified in Simbeor software [5].

Step 1: S-parameters measurement and pre-qualification

The first step in the systematic validation process is to make S-parameter measurements with VNA up to 50 GHz for 28–32 Gbps data rates and pre-qualify them for further analysis. For the reference, the CMP-28/32 kit includes S-parameter in Touchstone format measured for all structures by an expert with SOLT calibration up to the SMA connector. We will start with the example of formal pre-qualification of these measured data. The process is described in details in [1, 6]. We start with preliminary estimation of the passivity, reciprocity and causality metrics computed for discrete and bandwidth limited datasets. All metrics conveniently range from 0 (bad) to 100 (excellent) and further subdivided into bad, questionable, acceptable and good intervals as described in [6]. If all metrics fall into acceptable (blue) or good (green) intervals, we proceed and estimate the final quality metrics with the rational approximation or rational compact model. Models measured with high quality allow rational approximation with high accuracy—the root mean square error of such approximation can be used to construct the final quality metric [1, 6]. The end result of the measured S-parameters quality evaluation in Simbeor software is shown in Figure 2. All models measured by the expert pass the final quality test (Quality column).

Note that the frequency-continuous approximation of the discrete Touchstone models with the rational compact models is 100% causal by definition, because of the passivity is ensured by the software from DC to infinite frequency in this process. Such models are usable not only for the original Touchstone model quality evaluation, but also for further validation in time domain—fast and accurate computations of TDR/TDT and eye diagrams.

Step 2: Broadband material model identification

After S-parameters are measured and pre-qualified, the next step is to identify broadband dielectric and conductor roughness models. The model identification with generalized modal S-parameters (or GMS-parameters) is the simplest and most accurate way to do it [7-9]. It requires S-parameters measured for two line segments with different length. Line of any type with any impedance can be used. It also does not require modelling of the connectors and launches. The

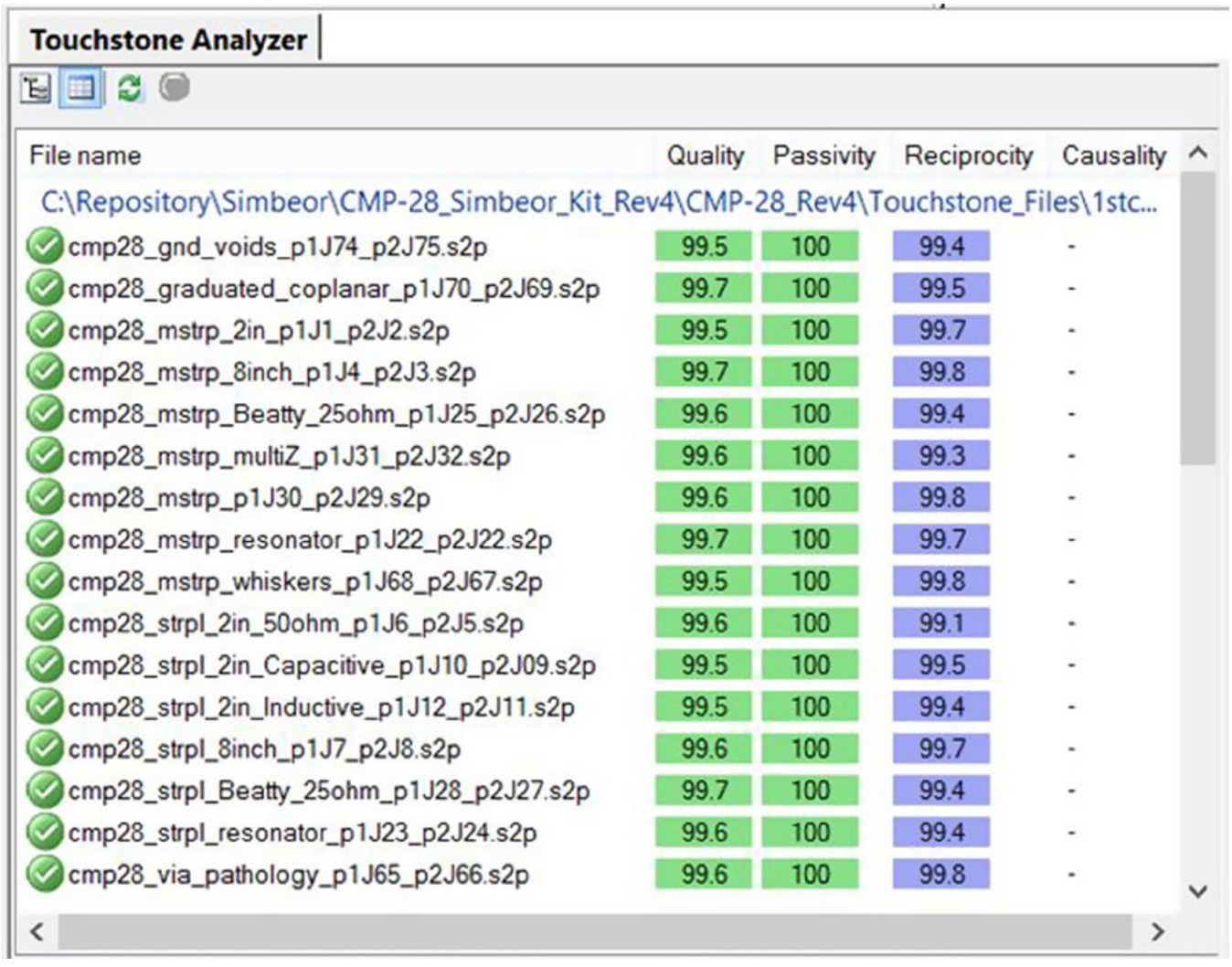

Figure 2: Example of formal quality evaluation in Simbeor software for a subset of S-parameters measured for CMP-28 platform.

CMP-28/32 platform contains 2- and 8-inch segments of single-ended stripline and microstrip traces and 2- and 6-inch segments of differential stripline and microstrip traces that can be used to extract or confirm dielectric and conductor roughness models.

We start with the single-ended stripline and first extract reflectionless GMS-parameters for 6-inch segment from the measured data shown in Figure 3 (red and blue lines with stars). The useful range of the GMS-parameters is about 30 GHz for the insertion loss and 40 GHz for phase delay (restricted by the manufacturing variations). Next we build a model of a 6-inch stripline segment with quasi-static field solver and first define dielectric model as the wideband Debye (AKA Djordjevic-Sarkar) [7] with dielectric constant Dk=3.66 and loss tangent LT=0.0117 as specified for Isola FR408HR material at 1 GHz.

To match the measured and modeled phase delay as shown in Figure 3, the Dk in the model needed adjustment from 3.66 to 3.815. This adjustment can be explained by the anisotropy of the composite dielectric. To match measured and modeled generalized modal insertion loss, we have two choices—increase the loss tangent or model conductor roughness. We choose to simulate conductor roughness with the simplest Modified Hammerstad model [7], defined

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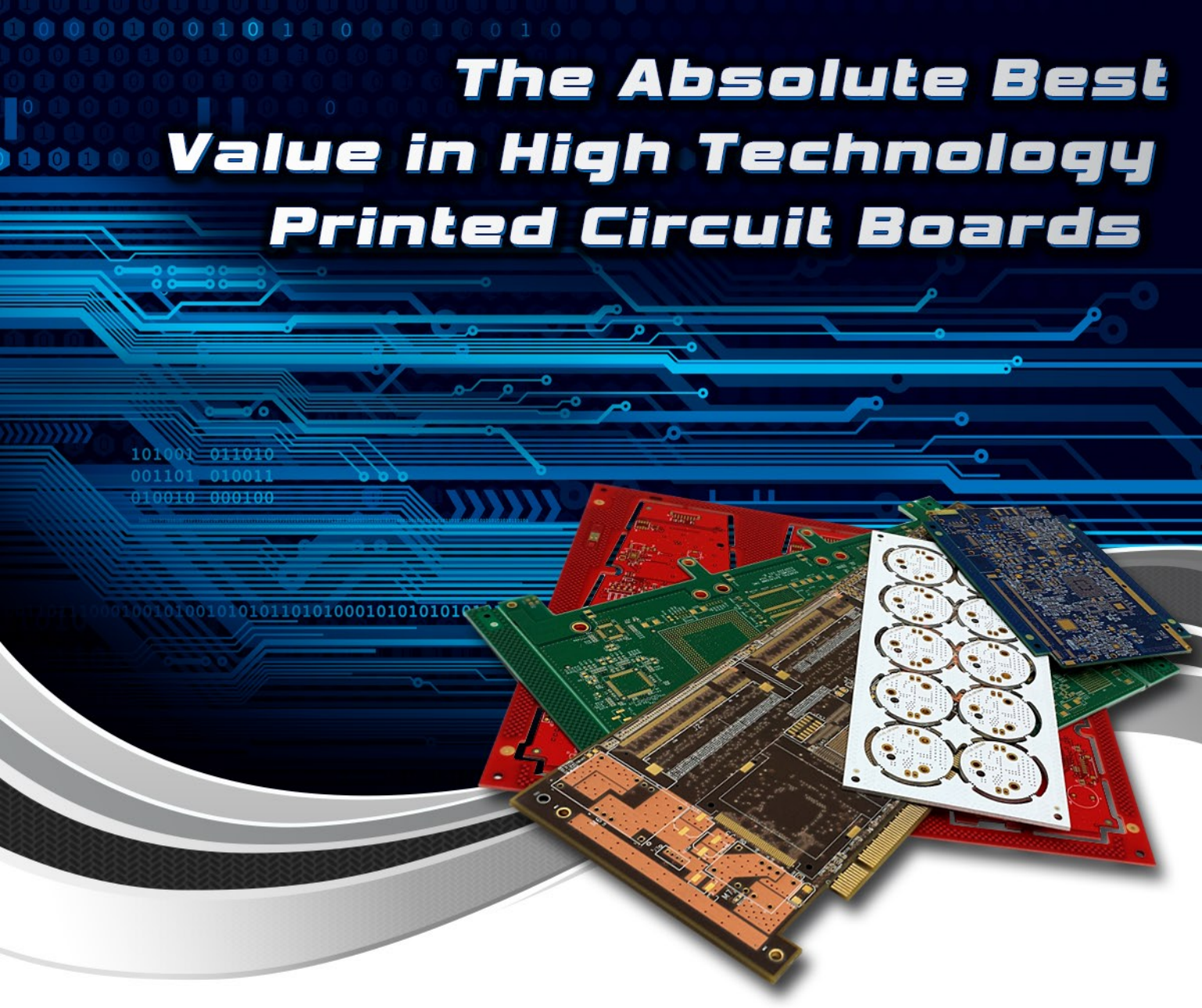

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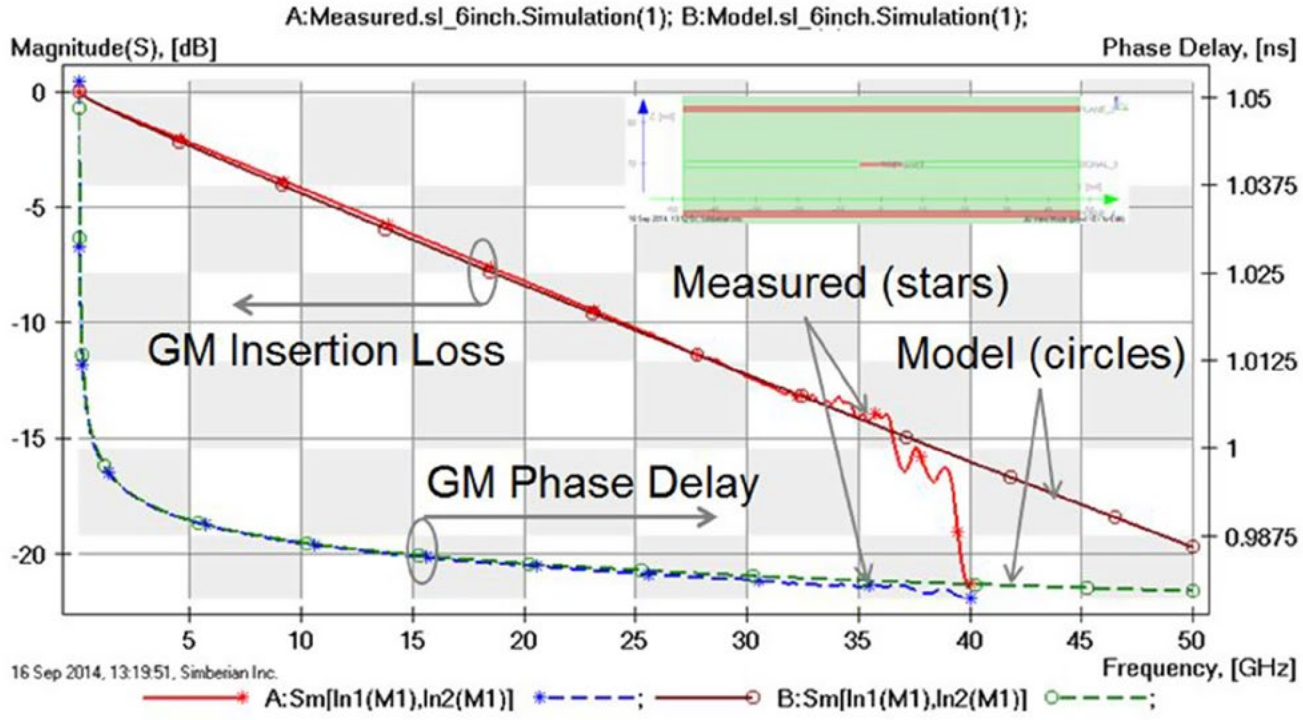

Figure 3: GMS parameters computed from S-parameters measured for 2- and 8-inch stripline segments (red and blue lines) and modeled for 6-inch stripline segment (brown and green lines) with wideband Debye dielectric model with Dk=3.815, LT=0.0117 @ 1 GHz, and Modified Hammerstad conductor roughness model with SR=0.4 um, RF=2.

by two surface roughness (SR) and roughness factor (RF) parameters. It is applied to the conductor surface impedance in the model. SR=0.4 um and RF=2 produced perfect good for the generalized modal (GM) insertion loss as shown in Figure 3.

FR408HR model identified with the stripline should also work for the microstrip line. It can be validated with the GMS-parameters computed from the measured S-parameters of 2 and 8 inch microstrip line segments and shown in Figure 4. The 6-inch segment model is constructed with the electromagnetic solver to capture the high-frequency dispersion seen as the upward trend in the phase delay in Figure 4. In addition we define solder mask model as the wideband Debye with the values taken from the manufacturer specification: Dk=3.85 and LT=0.02 at 1 GHz. Good match of the phase delay can be observed in Figure 4. To match measured and modeled GM insertion loss, the conductor roughness parameters for the microstrip line needed adjustment of the roughness factor from 2 to 3.5. That concludes the material model identification. The process is automated in Simbeor software and typically takes 5–10 minutes.

As an optional, but recommended step, GMS-parameters extracted from S-parameters measured for 2- and 6-inch differential links can be further used to confirm (or further adjust) the models extracted with the single-ended lines as demonstrated in [5].

Note that the identified dielectric and conductor roughness models are simple frequency-continuous expressions [7].The models are not just tables of Dk and LT frequency points and do not end where the measured data end. The extracted models are expected to be sufficiently accurate from DC up to 40 GHz and well above that frequency—the validation step will confirm it.

Step 3: Analysis-to-measurement validation

After the S-parameters are measured and pre-qualified and broadband material models

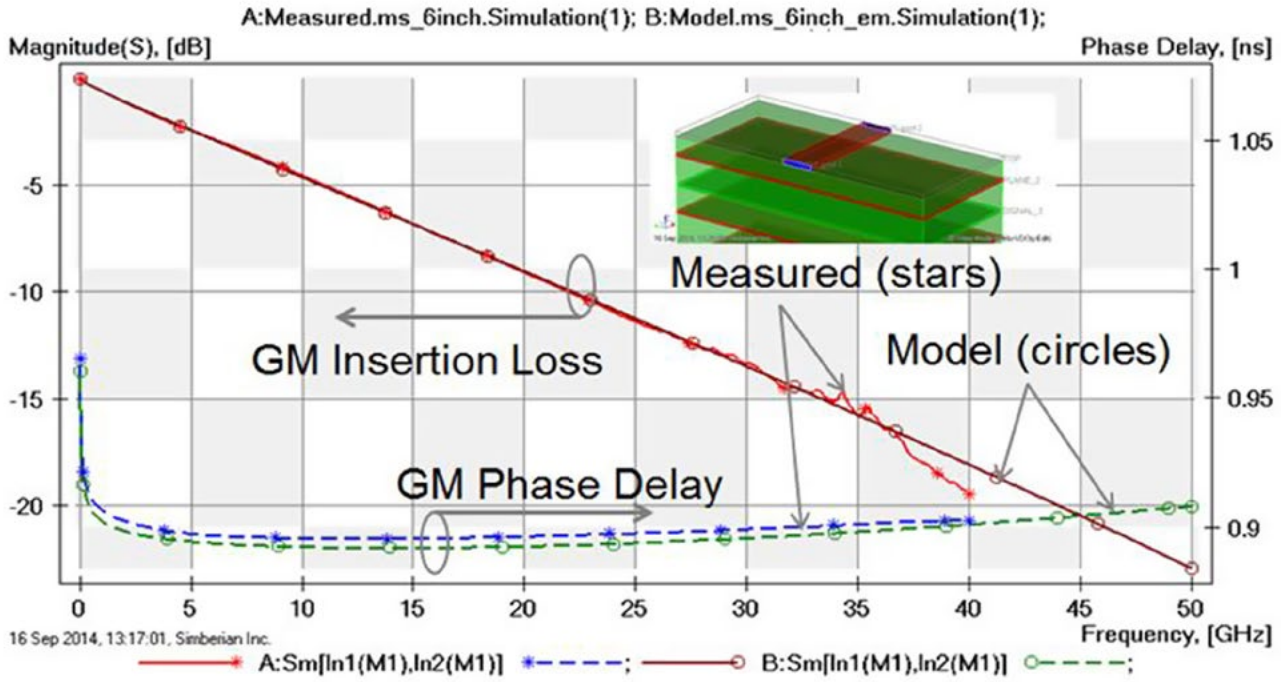

Figure 4: GMS parameters computed from S-parameters measured for 2- and 8-inch microstrip line segments (red and blue lines) and modeled for 6-inch microstrip line segment (brown and green lines) with the same FR408HR model as for the stripline and wideband Debye model for solder mask with Dk=3.85, LT=0.02 @ 1 GHz and Modified Hammerstad conductor surface roughness model with SR=0.4 um, RF=3.5.

are identified, the final step is to run the post-layout analysis on all 27 structures on the validation platform and compare magnitude and phase of S-parameters, TDR and eye diagrams for 28 Gbps signals. Note, that before proceeding with the post-layout analysis and even before the material model identification step, all stackup and trace width adjustments made by the PCB manufacturer must be discovered. If no information is available, the board has to be cross-sectioned to proceed further. PCBs are rarely manufactured as they appear in your favorite layout tool, but a post-layout analysis tool usually takes geometry directly from the board design files. Changes in stackup, trace width and shape, and via back-drilling have to be verified and applied to the interconnect geometry consistently before running any analysis. Believe it or not, even the most accurate electromagnetic solver will produce garbage results without proper geometry description. Note that these manufacturing variations introduce additional uncertainties, and they usually cause discrepancies at frequencies above 20–30 GHz and so far cannot be properly accounted for.

The validation can be done in two ways: for just the PCB interconnect part with de-embedded connectors, or for complete link paths with the connectors and optionally adapters (exactly as measured in step 1). De-embedding is the additional step that can be problematic and error-prone. From the earlier validation experience [4] we have learned that the de-embedding of PCB structures with TRL procedure produces acceptable results only for highly reflective structures such as resonators or highly reflective vias. The highly reflective structures can be used to validate the software, but they are not typical for the actual interconnects with the minimized reflection. TRL de-embedding produces large errors in the reflection for the typical low-reflective structures. It makes it difficult or even practically impossible to use TDR for the valida-

tion. This is due to large manufacturing and dielectric properties variations in the test fixtures typical for PCB realm.

Thus, we proceed with the second option: validation for the complete link path. All measurements for the step 1 were done with the 2.92 mm SMA connectors and 2.92 to 2.4 coaxial adapters; no models were available for both. To overcome this obstacle, the model of the connector with the adapter was simply synthesized from S-parameters measured for two connectors and two adapters connected symmetrically back-to-back. We used cascaded connection of four coaxial sections to model adapter and connector and then matched both magnitude and phase of the reflection and transmission of the measured S-parameters and the circuit model of the back-to-back structure [5]. In addition, models for all launches (PCB part) were built with the 3D electromagnetic solver as a part of the post-layout electromagnetic decompositional analysis in Simbeor. That eliminated the error-prone de-embedding step.

Technically, comparison of the magnitudes and phases of S-parameters is sufficient to either make a decision on the accuracy or spot a problem. However, comparison in time domain is usually also needed and may reveal additional

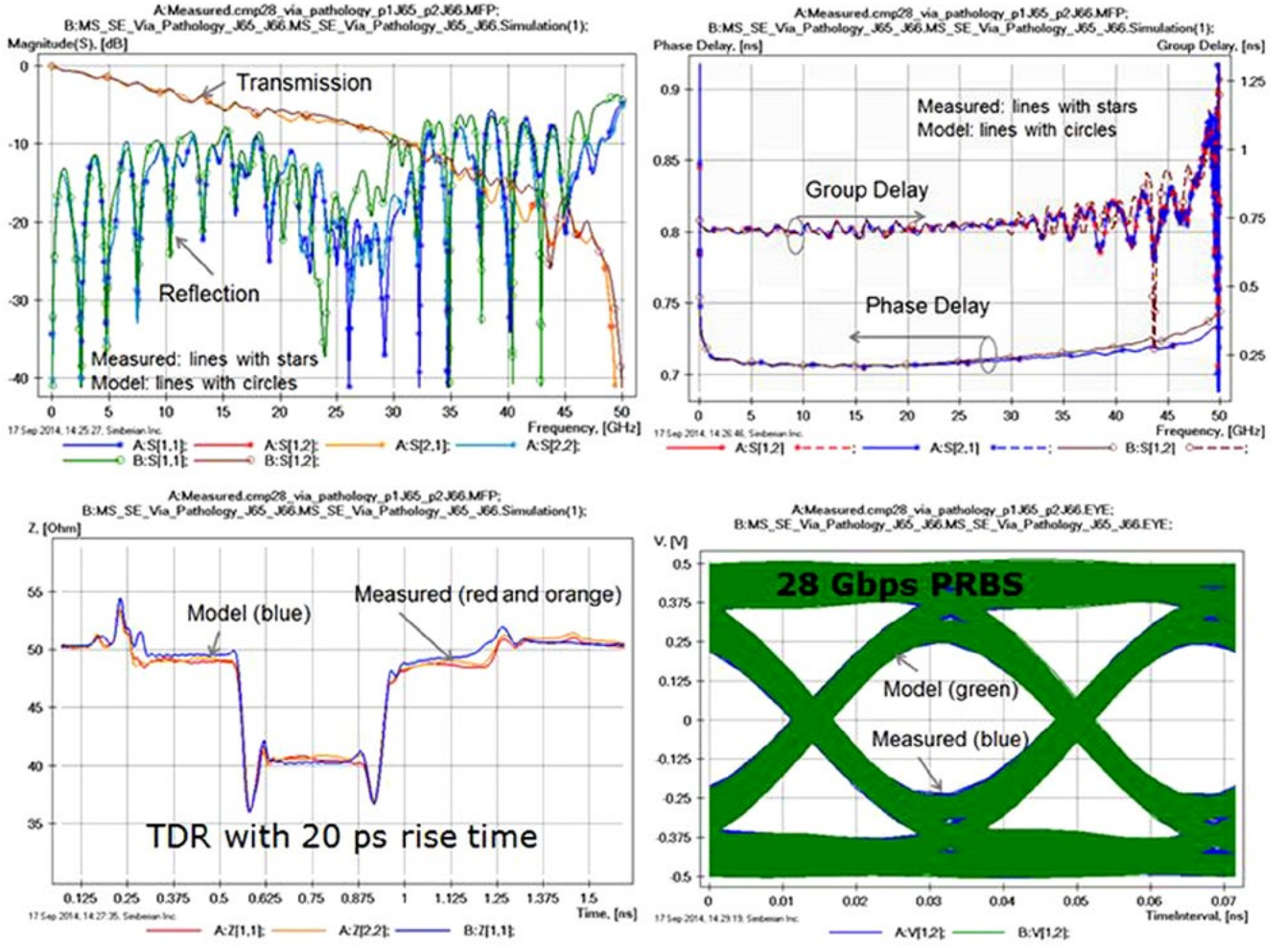

Figure 5: Model-to-measurement validation results for microstrip link with two capacitive vias (Figure 1, structure 1): Magnitudes of the transmission and reflection parameters (top left); group and phase delays of the transmission (top right), TDRs computed with 20 ps rise time Gaussian step (bottom left); eye diagrams for 28 Gbps PRBS signal (bottom right, on top of each other).

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problems. Comparison with TDR/TDT response that is measured directly with TDR scope requires modeling with the step function with the shape and spectrum matching to one used in the experiment. Similar situation is with the eye diagrams. Use of the ideal ramp step functions or PRBS with ideal trapezoidal shaped pulses may obfuscate and distort the results. Alternatively, measured and modeled S-parameters should be used to do all time domain computations with exactly the same stimuli matching the bandwidth of the model.

This can be done in two ways: either with convolution with the impulse response computed directly from discrete S-parameters with IFFT, or with the rational approximation and fast recursive convolution as it is done here. The rational approximation is frequency-continuous and naturally extends S-parameters to DC and to infinite frequencies. It is also causal by definition if passivity is ensured. The accuracy of the time domain analysis in this case is defined only by the accuracy of the rational approximation. In other words, the accuracy is always under control, unlike in case of analysis with IFFT where interpolation and extrapolation introduce uncontrolled errors. In addition, the recursive convolution is exact for piecewise linear signals and

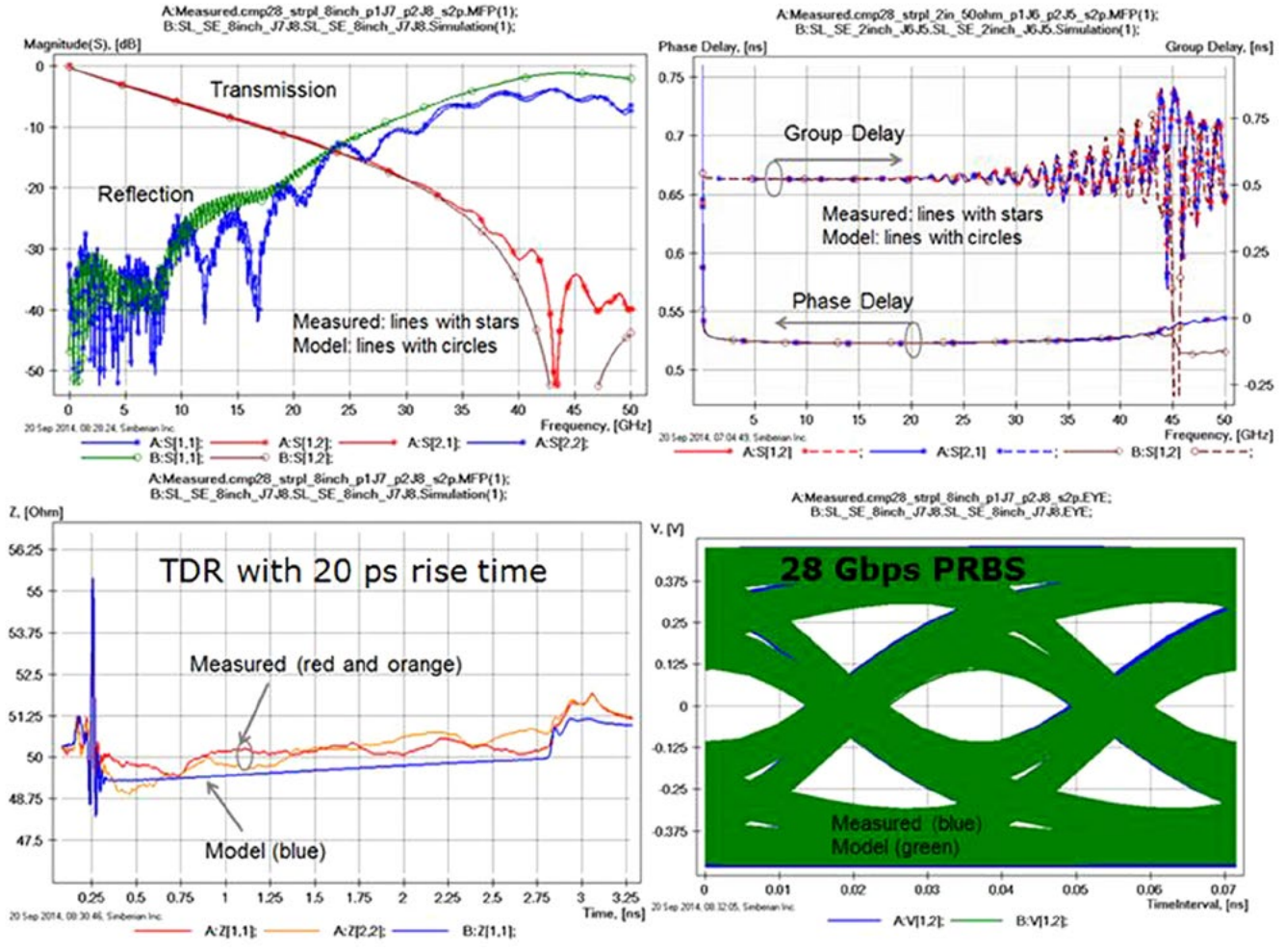

Figure 6: Model-to-measurement validation results for 8-inch stripline link (Figure 1, structure 2): Magnitudes of the transmission and reflection parameters (top left); group and phase delays of the transmission (top right), TDRs computed with 20 ps rise time Gaussian step (bottom left); eye diagrams for 28 Gbps PRBS signal (bottom right, on top of each other, literally).

much faster than the direct convolution. Thus, we will naturally use rational approximation for all time-domain computations here.

After all modeling decisions on what to compare and how to compare are made, we run the post-layout analysis for all 27 structures on the CMP-28 platform and compare the magnitudes of S-parameters, phase and group delays (and optionally phases), TDR computed with Gaussian step with 20 ps 10–90% rise time and eye diagrams computed with PRBS signal with 25 ps rise and fall time generated with LFSR with order 32. Two examples of the validation are shown in Figure 5 and Figure 6.

Results for microstrip line link with two capacitive vias (Figure 1, structure 1) are shown in Figure 5. It contains connectors with adapters on both ends, microstrip launches with through-hole vias, two segments of microstrip line with about 50 ohm impedance, two vias and one segment of wide microstrip line in the middle. The link is not optimal by design and represents highly reflective structure. We can conclude that the correlation is very good in this case and all discrepancies may be explained by the manufacturing and material properties variations.

Results of validation for a relatively low-reflective structure are shown in Figure 6. It is a simple 8-inch segment of single-ended stripline with launches, connectors and adapters on both ends (Figure 1, structure 2). The launches in this case are back-drilled with the goal to have less than 10-mil via stubs. Though, the manufacturer specified that the stubs may have +- 5 mil variation. 10-mil stubs were used in the model. Considering this and other types of variations, the correlation is acceptable. See all details of the analysis and analysis-to-measurement correlation for all 27 structures on CMP-28 platform in Reference [5] .

Conclusion

A systematic process of the analysis-to-measurement validation up to 50 GHz is introduced here. The process is illustrated in this article with the CMP-28/32 validation platform and Simbeor software. Note that the validation problems can fall into three categories: manufacturing, measurement, and analysis, and only measurement quality and the interconnect analysis parts are covered here. Following the procedure, you can easily qualify or reveal problems in your signal integrity software of choice. Just try to do the analysis of all 27 test structures on CMP-28/32 validation platform and swim at 28 Gbps and beyond.

Do not forget to compare the productivity and cost of the tools. Finally, is your software qualified for the analysis of PCB interconnects running at 50 Gbps? The question is rhetorical so far. **PCBDESIGN**

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Signal Integrity, Part 1 of 3

by Barry Olney
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As system performance increases, the PCB designer's challenges become more complex. The impact of lower core voltages, high frequencies and faster edge rates has forced us into the high-speed digital domain. But in reality, these issues can be overcome by experience and good design techniques. If you don't currently have the experience, then listen-up. This three-part series on signal integrity will cover the following topics:

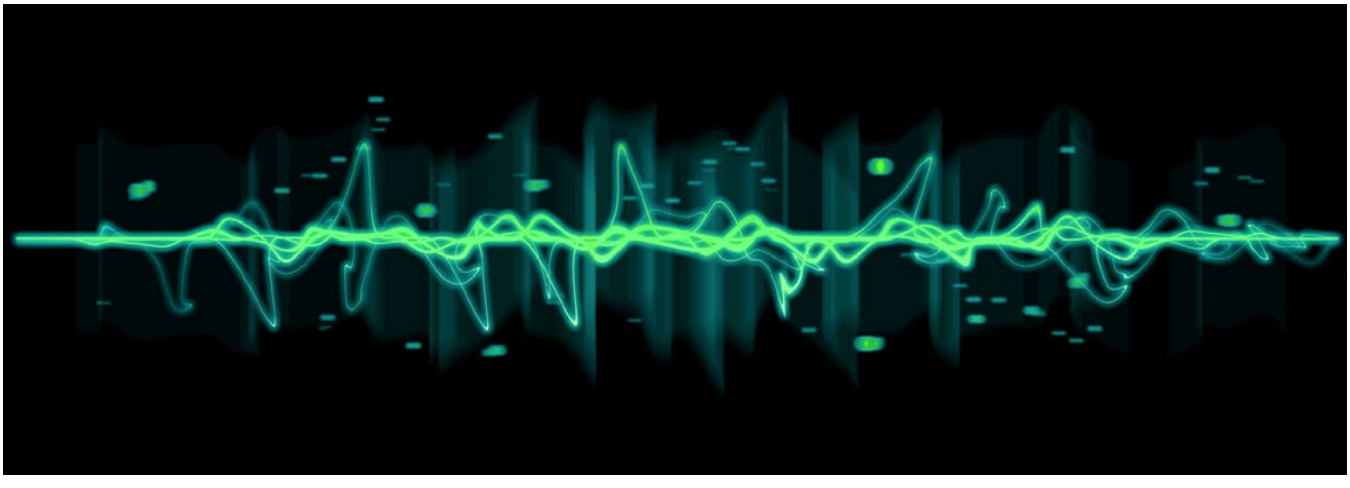
1. How advanced IC fabrication techniques have created havoc with signal quality and radiated emissions.
2. The effects of crosstalk, timing and skew on signal integrity.
3. Where most designers go wrong with signal integrity and how to avoid the common pitfalls.

Technology is moving fast and much has changed over the past 25 years that I have been involved in high-speed multilayer PCB design. Particularly, advances in lithography enable IC manufacturers to ship smaller and smaller dies on chips. In 1987, we thought that 0.5 micron technology was the ultimate, but today 22 nm technology is common.

Also, power consumption in FPGAs has become a primary factor for FPGA selection. Whether the concern is absolute power consumption, usable performance, battery life, thermal challenges, or reliability, power consumption is at the center of it all. In order to reduce power consumption, IC manufacturers have moved to lower core voltages and higher operating frequencies, which of course mean faster edge rates. However, faster edge rates mean reflections and signal quality problems. So even when the package has not changed and your clock speed has not changed, a problem may exist for legacy designs. The enhancements in driver edge rates have a significant impact on signal quality, timing, crosstalk, and EMC.

Figure 1 illustrates the change in edge rates over the years, from 10ns back in 1985 to less than 1ns in 2010. The faster edge rate for the same frequency and same length trace creates ringing in the un-terminated transmission line. This also has a direct impact on radiated emissions. Figure 2 shows the massive increase in emissions from the slowest to fastest rise time. When dealing with 1ns rise times, the emissions can easily exceed the FCC/CISPR Class B limits for an un-terminated transmission line.

At high frequencies, a trace on a PCB acts



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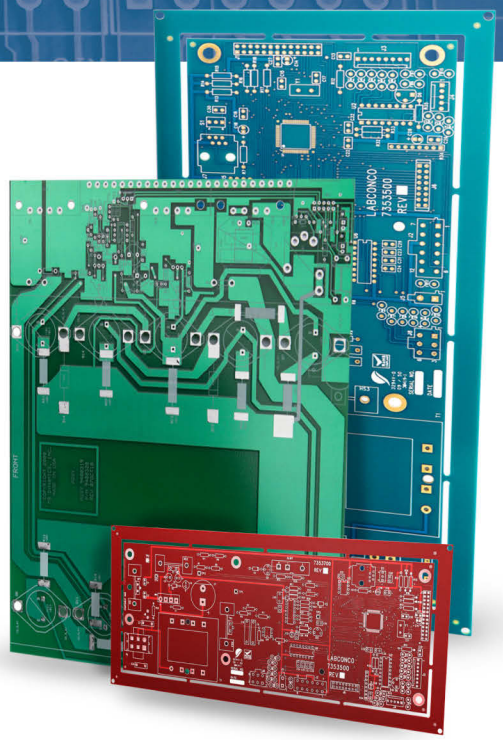

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SIGNAL INTEGRITY, PART 1 OF 3 *continues*

as a monopole or loop antenna. Unfortunately, the high-frequency components of the fundamental radiate more readily because their shorter wavelengths are comparable to trace lengths (particularly stubs), which act as antennas. Consequently, although the amplitude of the harmonic frequency components decrease as the frequency increase, the radiated frequency varies depending on the antennas/traces characteristics.

Computer-based products tend to radiate on the odd harmonics. High emissions are generally detected at the 3rd, 5th and sometimes the 7th harmonic of the fundamental clock frequency. If this also occurs where the AC impedance of the power distribution network is high, then the radiation is even higher. So at what speed should there be concern about wave propagation rather than just the current in conductors?

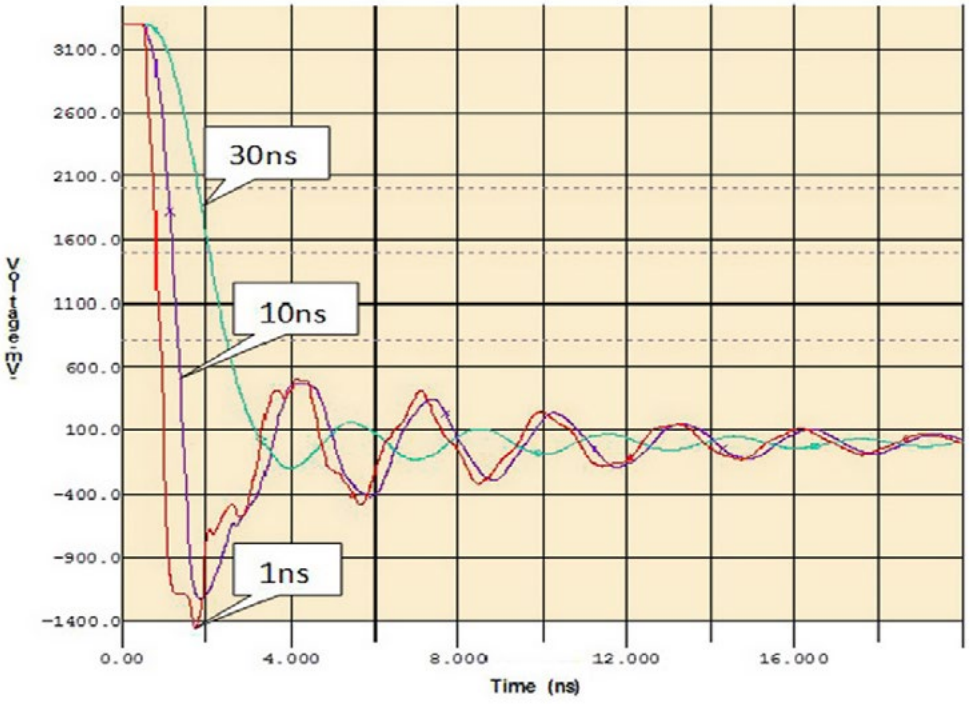

Figure 1: Edge rate changes over the past 25 years.

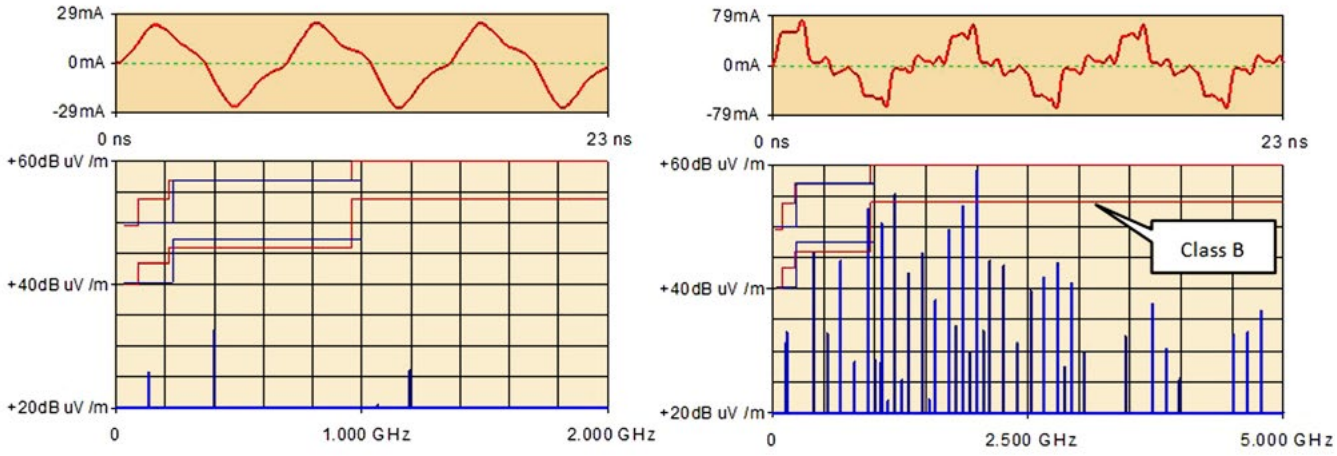

Figure 2: Radiated emissions from the 10ns edge rate (left) and 1ns (right).

Rule of thumb: Transmission line effects become an important design consideration when the trace length approaches 1/6 of the wavelength of the signal being transported. If the system clock frequency is 300 MHz, then the wavelength in FR-4 is about 0.5 m.

Impedance is the key factor that controls the stability of a design—it is the core issue of the signal integrity methodology. At low frequencies, a PCB trace is almost an ideal circuit with little resistance, and without capacitance or inductance. Current follows the path of least resistance. But at high frequencies, alternating current circuit characteristics dominate causing impedance, inductance and capacitance to become prevalent. Current then follows the path of least inductance. The impedance of an ideal lossless transmission line is related to the capacitance and inductance:

But this is very simplistic and the impedance should be simulated by a field solver (Figure 3) to obtain accurate values of impedance for each signal layer of the substrate. The impedance of the trace is extremely important, as any mismatch along the transmission path will result in a reduction in quality of the signal and possible radiation of noise. For perfect transfer of energy, the impedance at the source must equal the impedance at the load. However, this is not naturally the case and terminations are generally required at fast edge rates to limit ringing.

The configuration of the PCB stackup depends on many factors. But whatever the requirements, one should ensure that the following rules are followed in order to avoid a possible debacle:

- All signal layers should be adjacent to and closely coupled to an uninterrupted reference plane, creating a clear return path and eliminating broadside crosstalk.
- There is good planar capacitance to reduce AC impedance at high frequencies.
- High-speed signals should be routed between the planes to reduce radiation.
- The substrate should be symmetrical with an even number of layers. This prevents the PCB from warping during fabrication and reflow.
- The stackup should accommodate a number of different technologies.
- Cost (the most important design parameter) should also be addressed.

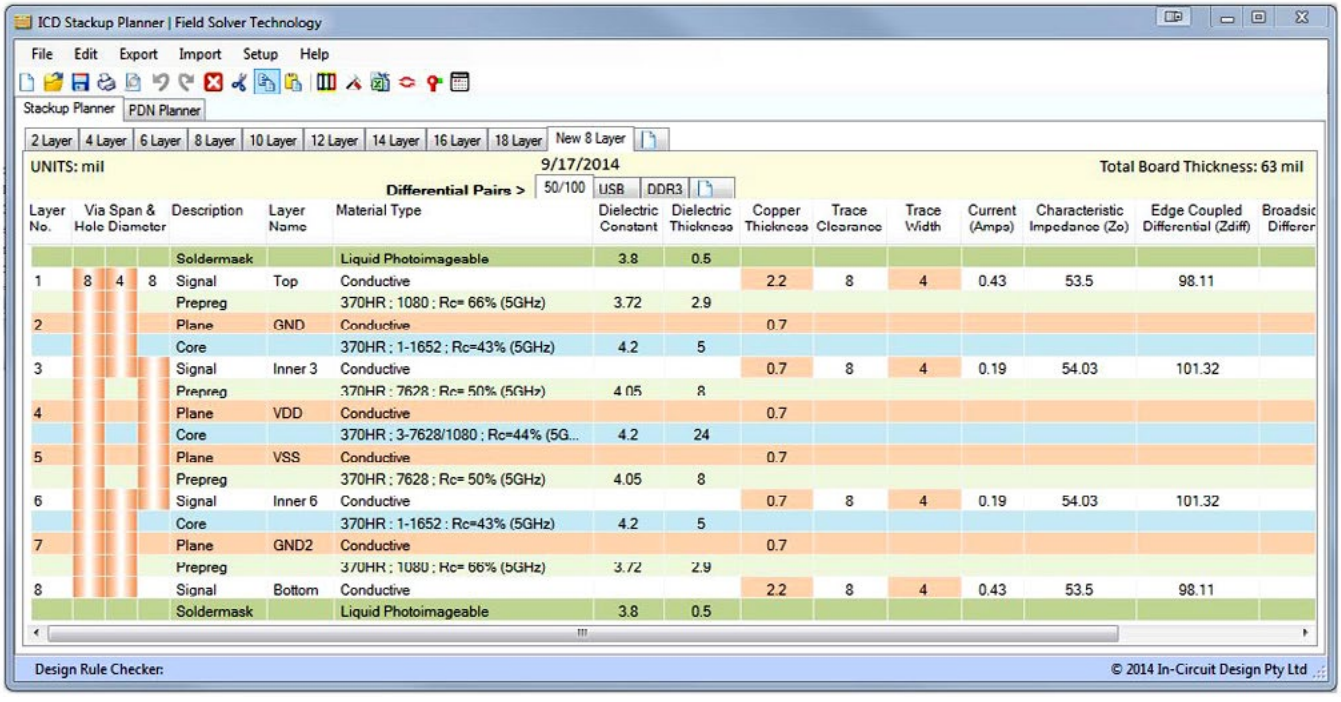

Figure 3: Impedance simulated by a 2D BEM field solver in the ICD Stackup Planner.

SIGNAL INTEGRITY, PART 1 OF 3 *continues*

As signal rise times increase, consideration should be given to the propagation time and reflections of a routed trace. If the propagation time and reflection from source to load are longer than the edge transition time, an electrically long trace will exist. If the transmission line is short, reflections still occur but will be overwhelmed by the rising or falling edge and may not pose a problem. But even if the trace is short, termination may still be required if the load is capacitive or highly inductive to prevent ringing. Note that series terminators are the most effective for high-speed design.

For a driver signal with a 1ns rise time, since the speed of a signal in FR-4 is approximately 6in/ns (150mm/ns), then an un-terminated trace can only be 6 x 1/6 = 1.0 inches (25mm) before reflections occur and termination is required.

Rule of Thumb: All drivers, whose trace length (in inches) is equal to or greater than the rise time (in ns), must have provision for termination.

In order to terminate a transmission line, one first needs to know the impedance of the driver and the transmission line. So how do we find this information? First of all an accurate field solver, such as the ICD Stackup Planner is required to determine the impedance of the PCB traces. Then, the source impedance must be extracted from the IBIS model. Subtracting the source impedance from the trace characteristic impedance gives the required series terminator value. Further details on how to find the source impedance in the IBIS model can be found in a previous column Beyond Design: Impedance Matching: Terminations.

Differential pairs are frequently used in high-speed design to provide noise immunity on serial interconnects. A differential pair is two complementary transmission lines that transfer equal and opposite signals down their length. These lengths should be kept equal and they should be coupled evenly along the signals length where possible. Symmetry is the key to successfully deploying differential signals in high-speed designs. Maintaining the equal and opposite amplitude and timing relationship is the principle concept.

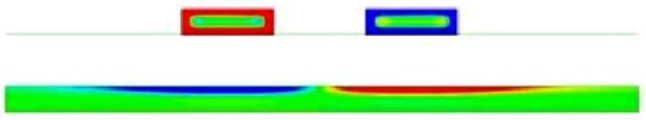

Figure 4: Return current of a microstrip differential pair. (courtesy of Ansoft)

Many people believe that since the two halves of the pair carry equal and opposite signals, that good ground connection is not required as the return current flows in the opposite signal. However, the return current actually flows in the reference plane below each trace. Figure 4, illustrates the return current of a microstrip pair flowing directly below each trace—just as is the case for a single ended transmission line. The only reason the pair of traces need to be coupled, is to reject common external noise.

If a differential pair can be routed closely coupled along the entire length, then consider using tight coupling. Otherwise, if the pair need to separate around an obstacle (a via for instance) then coupling the pair by twice the trace width is more effective. The reason being that a tightly coupled pair will increase impedance by 25% if separated while a more loosely couple pair will only vary by about 4% impedance. This provides more stable impedance along the trace length.

The rule of thumb: Gap = 2x trace width.

Next month's column will continue to discuss signal integrity, in particular the effects of crosstalk, timing and skew on signal integrity so stay tuned.

Points to Remember

- Advances in lithography enables IC manufacturers to ship smaller and smaller dies on chips.
- In order to reduce power consumption, IC manufacturers have moved to lower core voltages and higher operating frequencies, which of course mean faster edge rates.
- Faster edge rates mean reflections and signal quality problems.

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• The faster edge rate, for the same frequency and same length trace, creates ringing in the un-terminated transmission line. This also has a direct impact on radiated emissions.

• Transmission line effects become an important design consideration when the trace length approaches 1/6 of the wave-length of the signal being transported.

• Impedance is the key factor that controls the stability of a design—it is the core issue of the signal integrity methodology.

• Any mismatch in impedance along the transmission path, will result in a reduction in quality of the signal and possibly radiation of noise.

• Series terminations are generally required at fast edge rates to limit ringing.

• All drivers, whose trace length (in inches) is equal to or greater than the rise time (in ns), must have provision for termination.

• Differential pair return current actually flows in the reference plane below each trace not in the opposite signal. **PCBDESIGN**

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The ICD Stackup and PDN Planner is distributed globally Altium.

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.

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PCB007 News Highlights

IPC: Slump in PCB Sales and Orders is Typical for July

"July is typically a slow month for the PCB industry and this year is no exception," said Sharon Starr, IPC's director of market research. "The PCB book-to-bill ratio has been hovering around 1.00 since February, which explains the flat year-to-date sales growth we are seeing," she added.

Molex Dongguan China Earns FDA Registration

Molex Incorporated announced that the Molex Dongguan, China facility is now registered with the U.S. FDA as a compliant manufacturer of Class I medical devices. Part of an ongoing process improvement plan by the Molex printed circuit products group, registration confirms the Dongguan China site's adherence with FDA inspections, tracking, and traceability criteria.

Global PCB Market to Increase to $74.3B in 2018

IndustryARC forecasts the global PCB manufacturing market to increase its market size from around $62.3 billion in 2013 to around $74.31 billion in 2018, growing at a CAGR of 3.6%.

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The executed technology license agreement between the two companies provides Murrietta the right to manufacture PCBs using eSurface's patented technology, receive implementation and marketing support from eSurface, and to be acknowledged as an eSurface authorized facility.

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i3 Electronics Inc. has signed a multi-year agreement with an industry leading high-performance Computing firm for the supply of high-performance electronic assemblies. i3 will manufacture the PCBs and provide assembly, integration, and test services.

Precision Circuits West Unveils Line of Aluminum PCBs

These aluminum PCBs (also called metal core PCBs) are five to ten times as thermally conductive as conventional epoxy-glass, at one-tenth of the thickness resulting in thermal transfer far more efficient than a conventional rigid PCB.

Intercept Strengthens Canadian Representation with Kaltron

"Kaltron is delighted to offer Intercept's PCB, Hybrid IC, and RF software solutions to our customers in Canada. They complement very well our existing portfolio of design services, components, and modules," said Tom Martin, president of Kaltron.

Multitest Leads the Way in 0.3 mm-pitch PCBs

Multitest can manufacture PCBs with 40+ layers at 0.35 mm in a single lamination process without the use of laser drilled, "stacked," blind vias.

Ibiden Receives Multilayer PCB Manufacturing Tech Patent

The patent is mainly for a method of manufacturing a multi-layer printed wiring board including forming a core substrate, forming a first interlayer insulation layer over the core substrate, and forming a first filled via in the first interlayer insulation layer.

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Thermal Characterization of LEDs: Enabling the Upcoming Lighting Revolution

by Dr. John Parry
MENTOR GRAPHICS

According to a June 2012 report from the Climate Group, many commercially available, outdoor light-emitting diode (LED) products offer high-quality light, durability, and significant electricity savings in the range of 50–70%. More European cities are adopting LED streetlights because LEDs can save energy costs, while exceeding local lighting standards. They last 50,000 to 100,000 hours, change little in color, and have a failure rate of around 1%, compared, for example, to up to 10% for ceramic metal halide fixtures over a similar time period. LED streetlights are a gateway technology—when LED designers solve the current problems of reducing cost and thermal challenges, they'll be paving the way for wider adoption and the energy-saving potential of LEDs.

Thermal management is one of the more complex areas of LED system design. And until a few years ago, the methods and technology to scientifically characterize the thermal behavior of the component, as well as its systems and subsystems, were not available. Instead, most engineers calculate their thermal needs from data sheets published by component manufacturers. Understandably, having data available to engineers on the specific thermal mechanics of LED-based devices within the system in which they are being used could be a huge step forward for future lighting designs.

This article describes a method that combines hardware measurement (a thermal transient tester), and computational fluid dynamics (CFD) software to provide high measurement throughput, which enables systems integrators to verify a vendor's thermal resistance data during design and to test incoming commercial off-the-shelf parts before they are introduced into production. This data can be used during the design and product development phase to accurately capture the thermal response of an LED lighting system.

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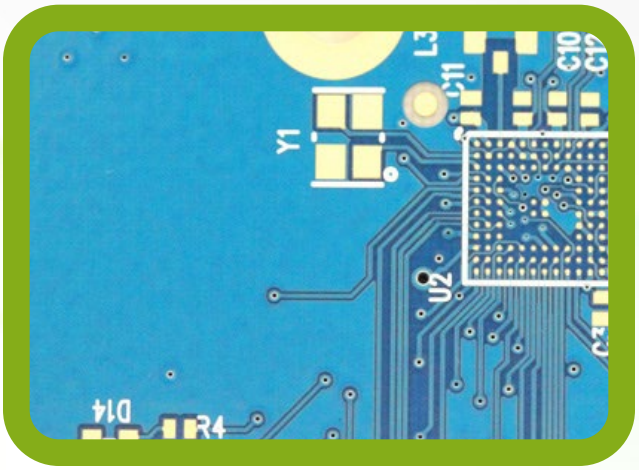

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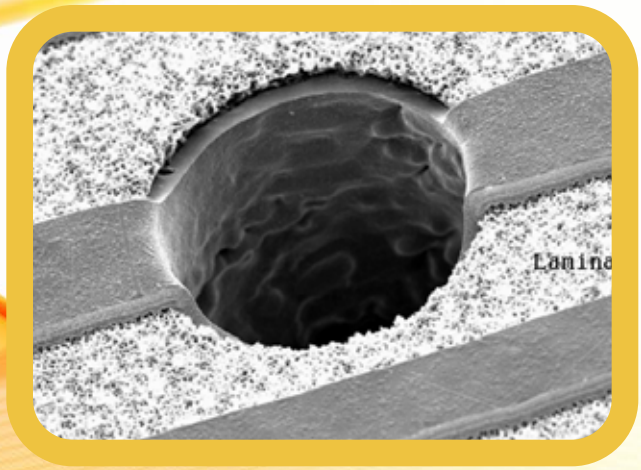

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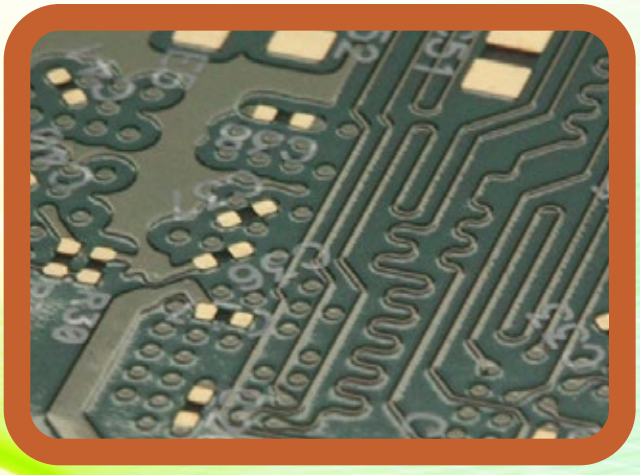

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Comprehensive LED Characterization

The first step is to measure the LEDs that are generally suitable for the lighting application and to evaluate them by thermal and radiometric characterization. The LED must be measured as it transitions from a hot to cold state of operation to be able to thermally characterize it using the electrical test method. The results of such measurements are LED package thermal metrics and descriptive functions that will help design engineers understand the structure. The proper thermal design of the cooling solution can be created when the latest JEDEC LED thermal testing standards[1, 2] are used in this approach to identify the real thermal resistance and the real thermal impedance of the package. Also, not only the radiant power is measured and used in the thermal resistance-impedance calculations, but the temperature dependence of other light output properties such as luminous flux or color coordinates can also be measured. This way the best suitable LED can be selected from the various LED vendors for the design of a particular lighting application.

These testing standards were used in the development of LED-specific testing and measurement systems to provide comprehensive LED characterization, including thermal transient measurements and measuring almost all light output properties of LEDs. Figure 1 shows an example of an LED junction temperature transient measured on a cold plate—as the JESD 51-51 and JESD 51-52 standards recommend.

The measured junction temperature transient is turned into thermal impedance if it is divided by the applied heating power. In the case of LEDs, this is the supplied electrical power (forward voltage ´ forward current) less the emitted optical power, also known as total radiant flux. The LED under test must be characterized optically to account for this. If the emitted optical power is not considered, the resulting thermal resistance will be smaller than reality,

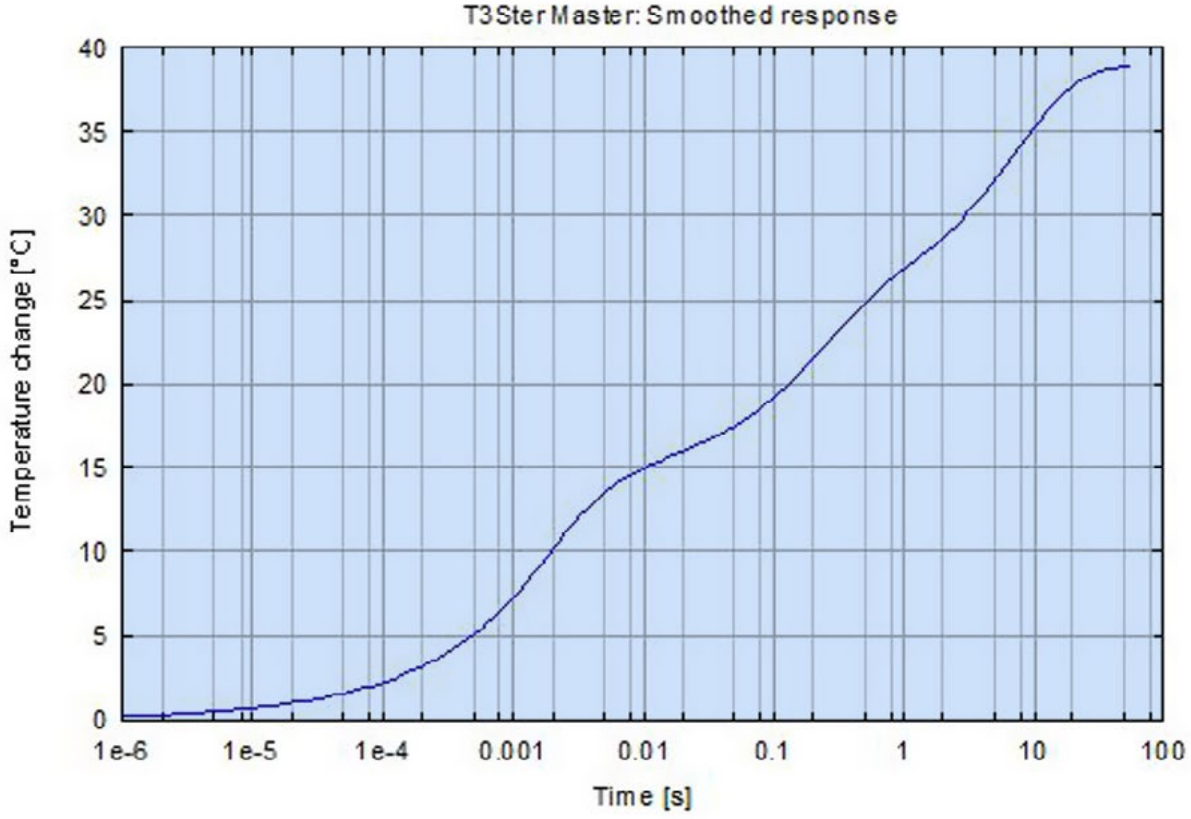

Figure 1: Example of measured junction temperature transient of a device.

misleading the designers of the cooling solution. Measurement of the light output properties in combination with thermal tests as suggested, for example, by the JEDEC JESD 51-52 standard provides useful information about their temperature dependence (Figure 2). Figure 3 shows how the chromaticity of the measured LED changes with forward current and temperature.

The data processing software of the measurement system, T3Ster, derives structure functions from the transient measurement, which are then converted into models that are accurate in the case of packages that possess one-dimensional heat-flow path such as power LED packages[3]. Such models can be created as "side products" when the R_{thJC} junction-to-case thermal resistance of the package under test is identified according to the latest JEDEC transient measurement standard (JESD 51-14), based on the so-called transient dual interface method[3].

New Model for Simulating LED Thermal Resistance and Capacitance

This transient tester data can be used to more accurately simulate LED thermal characteristics by 3D CFD software, such as FloEFD, through an LED model, the so-called JEDEC 2R thermal resistor model in an extended format. For the 2R model, the necessary information can be found easily in the datasheets. In case of LEDs, the junction-to-bottom resistor of the 2R model is relevant; it is more or less equal to the R_{thJC} junction-to-case thermal resistance of the package.

For the junction-to-top resistance of the 2R model, the junction-to-lens thermal resistance would be needed. This is usually not provided and it hardly can be correctly tested, and usually a sufficiently large value obtained from CFD simulations is provided. The way the standard 2R model is extended in the CFD software is that the junction-to-bottom part of the model is represented an RC model, which allows tran-

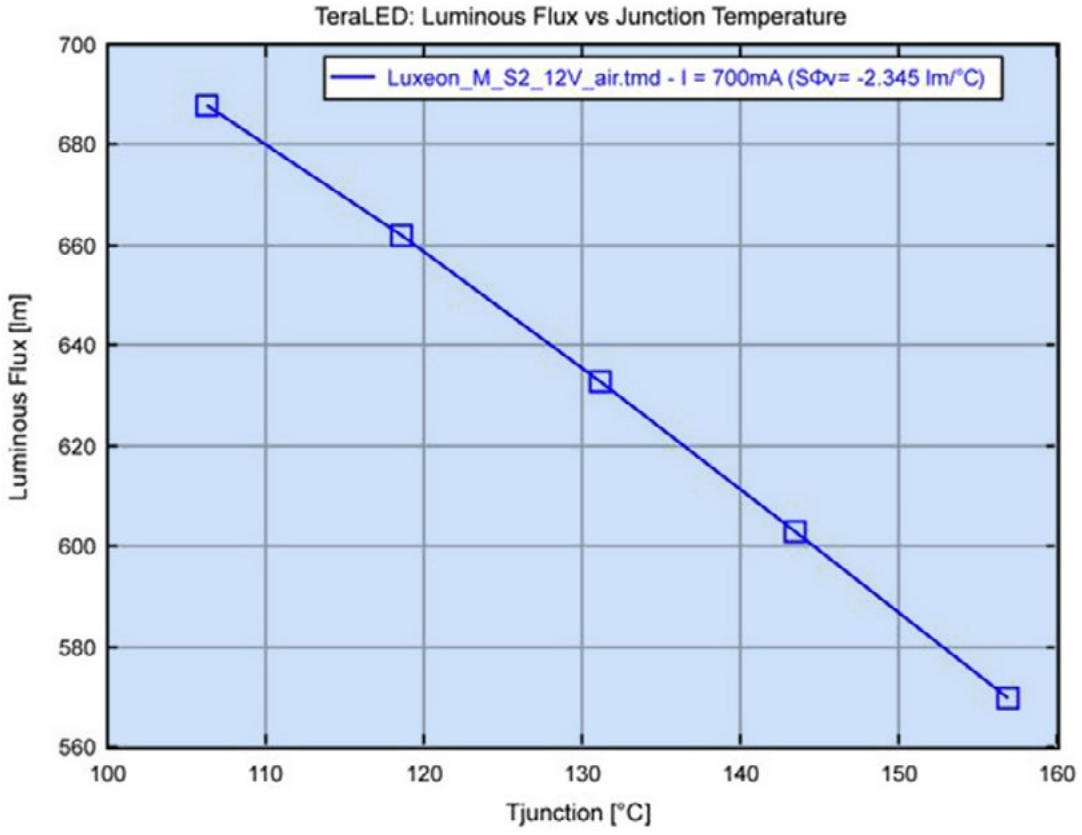

Figure 2: Example of luminous flux vs. junction temperature at different current settings.

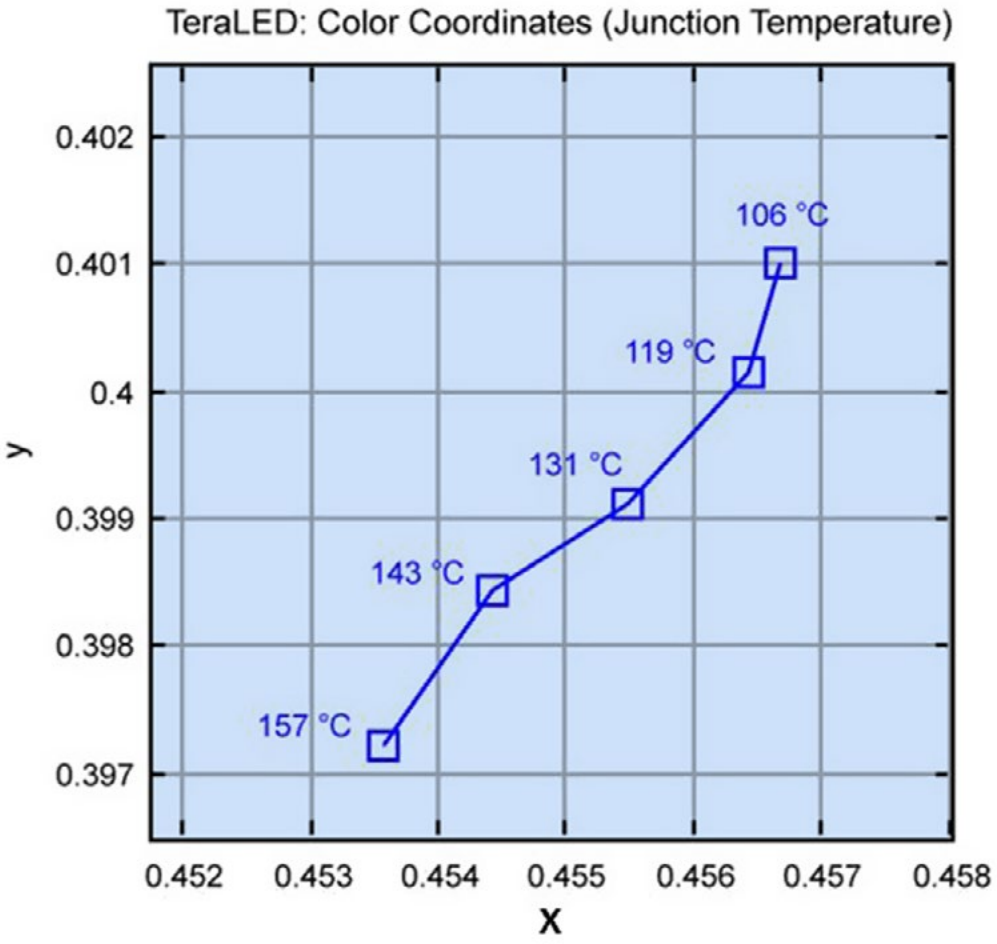

Figure 3: Example of a chromaticity diagram for an LED generated by the TeraLED measurement system.

sient simulations because the thermal capacitance is also included in the model. However, the more detailed RC model requires more data of the LED, which often cannot be found in datasheets. In this case, the CFD tool makes it easier with an interface to the thermal characterization system.

A file can be exported out of the thermal transient tester's post-processing software that can be read by the CFD simulation tool with all the necessary data for the RC model in form of a Cauer-type ladder model. This file contains not just single thermal resistance and capacitance from junction to bottom (R_{jb} and C_{jb}) values of the LEDs as a bulk value representing a single thermal time constant for the package, but represents the heat-flow path structure in details appropriate for accurate transient simulation using CFD analysis. For the proper prediction of the LED's hot lumens (luminous flux at operating junction temperature), an LED model in CFD also contains simple models for the radiant flux and luminous flux for constant drive currents of the LED. These models use the measured junction temperature sensitivity of these light output properties. Including the temperature sensitivity of these parameters is important to account for the complex, multi-domain operation of LEDs. Figure 4 shows results from the LED Compact Model in FloEFD provided for a given forward current using thermal data from thermal transient measurements by the T3Ster system.

Based on measured results from a validation experiment[4] to test this approach, it was clear that a simple reliance on datasheet values is insufficient when trying to determine the thermal performance of an LED system. Other meth-

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ods provided information that there was a thermal issue with the LED packages under test; however, only the JESD 51-51 compliant transient test method provided a hint about the location of the problem. As well as being useful for failure analysis, this method can be used to derive an appropriate compact LED model which, when inserted into a simulation tool, can provide better predictions of LED operation. LED system designers will be able to rely on real measured component data, allowing them to make better judgments on their thermal designs. This capability will allow wider adoption and reduced costs with the energy-saving potential of LEDs. **PCBDESIGN**

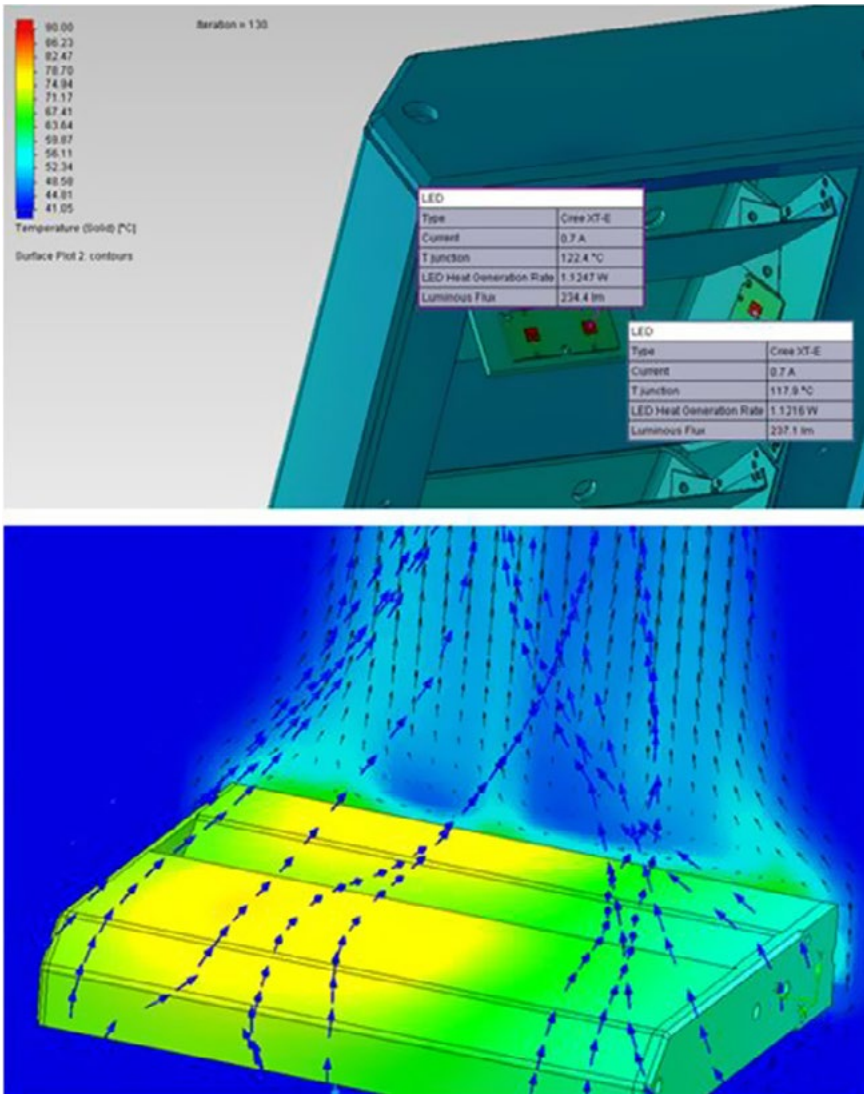

Figure 4: An example of the calculation done in the CFD simulation software using the LED Compact Model of the luminous flux, at operating junction temperature for the LEDs in a luminaire. (Image courtesy of OptimalOptik Ltd. and Budapest University of Technology and Economics, Budapest, Hungary.)

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4. B. Marovic, "Efficient and Accurate Thermal Simulation by Combining Thermal and Radiometric Characterized LEDs with Computational Fluid Dynamics," International Symposium on Automotive Lighting, Sept. 2013, Darmstadt, Germany.

Dr. John Parry is electronics industry manager for the mechanical analysis division of Mentor Graphics. He serves on the JEDEC Thermal Standards Committee and on various conference committees and was General Chair of the SEMI-THERM 21 conference.

This is Sketch Routing, Part 2: Quality

by Charles Pfeil
MENTOR GRAPHICS

This is the second of three articles that discusses the core elements of effective PCB routing (control, quality, and performance). I recommend reading my last column on taking control, because it gives some background information that will help when reading this column.

PCB designers care about route quality and it is not just a matter of being artistic. Route quality is objective and subjective—both are essential to successful routing.

Objective Quality

Objective quality can be defined as fulfilling the fabrication and signal integrity requirements as defined. The intent of route quality for fabrication is to enable high board yields, high reliability and low cost. It is important to understand the critical elements required by the fabricator, then set up and follow the physical constraints that will satisfy the desired objectives. Interactive and automatic routing must follow these physical rules, otherwise the time spent preparing any moderately complex design for fabrication will be excessive.

Signal integrity requirements are more complex. The timing, impedance management, and noise control requirements can be expressed through constraints. However, sometimes it is necessary to compromise in order to build a board that meets the fabrication goals. There is a tendency to over-constrain for signal integrity purposes. The thinking is if the constraints are very conservative, the design should perform as desired. Unfortunately, over-constraining for signal integrity purposes can lead to lower yields, poorer reliability and higher fabrication cost. The right balance between the fabrication and signal integrity requirements must be discovered and applied.

The routing environment needs to provide the ability to constrain, route, tune, and analyze both single-ended and differential signals in a manner that satisfies these objective quality aspects of design. If you're manually routing a

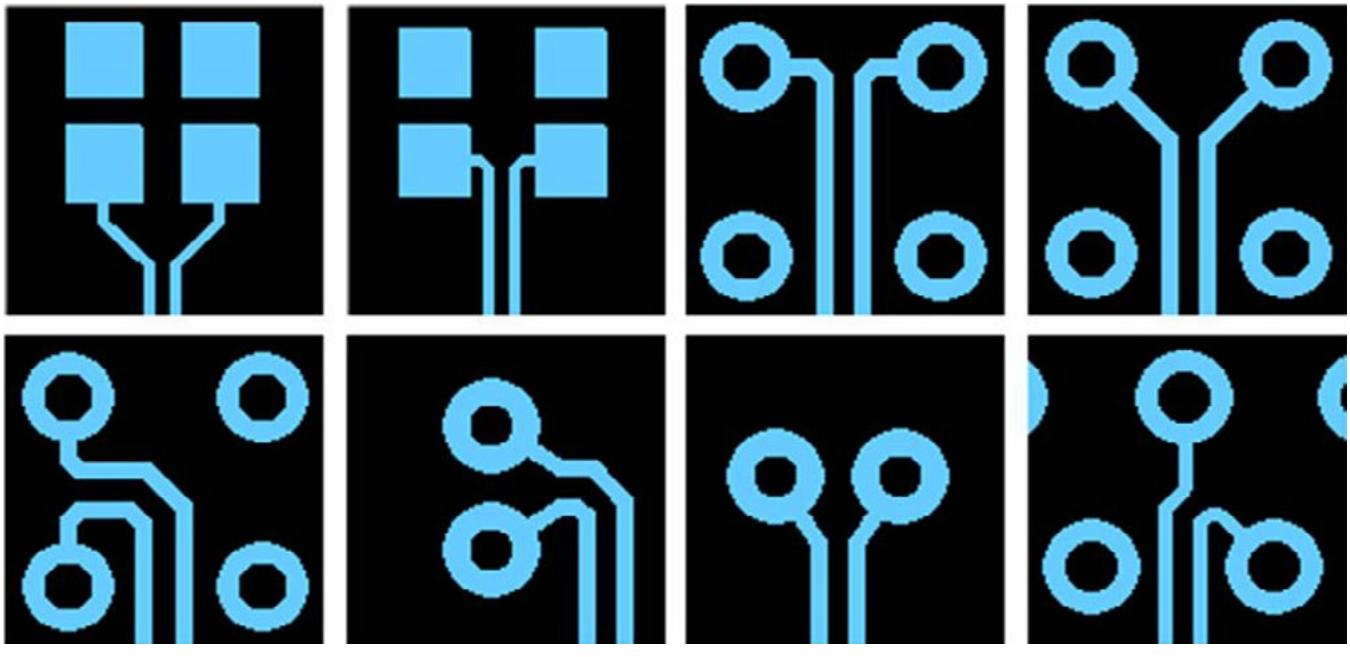

Figure 1: Objective quality for differential pair pad entry.

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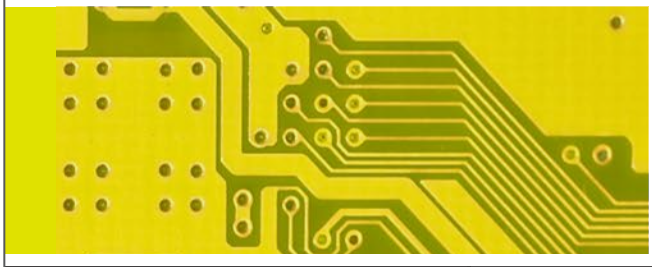

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THIS IS SKETCH ROUTING, PART 2: QUALITY *continues*

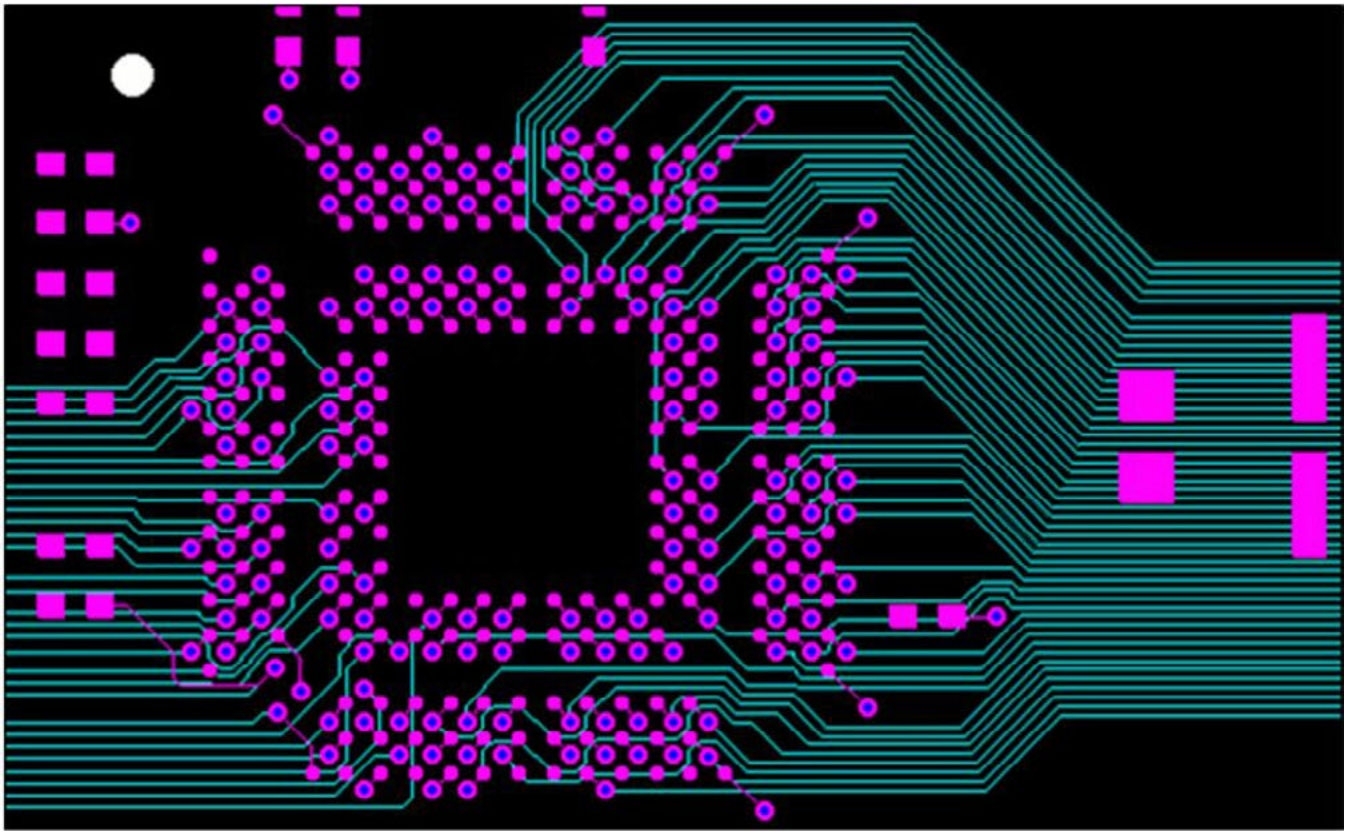


Figure 2: Subjective quality = efficient routing.

design and the constraints are set up properly, fulfilling the objective quality metrics will be accomplished—the only problem is that it may take a long time. Tuning the nets in matched sets or tuning for phase matching is clearly a painstaking process if it all has to be done manually. The most effective routing environment for objective quality is to have high levels of automation under the control of the designer.

Subjective Quality

Subjective quality is not so easily defined or accomplished. We have all heard that designers spend time trying to make the routing look pretty or look like art. I suggest that it is actually something else. It is a matter of efficiency. Designers want to route efficiently, meaning the traces are direct without excessive meandering, vias used only when absolutely necessary, no extra jogs without purpose, and the traces spaced evenly. Efficient routing is a primary method for attaining the objective quality. It is not a coincidence that efficient routing often appears artistic because we tend to associate symmetry, balance, and repeated patterns with what know as graphical art.

Mentor Graphics conducts the Technology Leadership Awards program each year, with customers submitting designs to be judged. Awards are given out in each technology segment and an overall winner is celebrated. I was a judge in the last event, and along with the other judges, we found it is sometimes hard to determine if a design is truly simple, or if it is really complex, yet routed so well that it only looks simple. If routing a design in the most efficient manner results in the design looking simple, we can call it art but I prefer to look at it as routing excellence. This is my definition of subjective quality. I believe that providing this kind of quality is fundamental and is required for any automated routing methods to be widely adopted by designers.

Any designer who has been manually routing PCBs for years also understands that most of us display a bit of obsessiveness in our routing methods, especially when it comes to even spac-

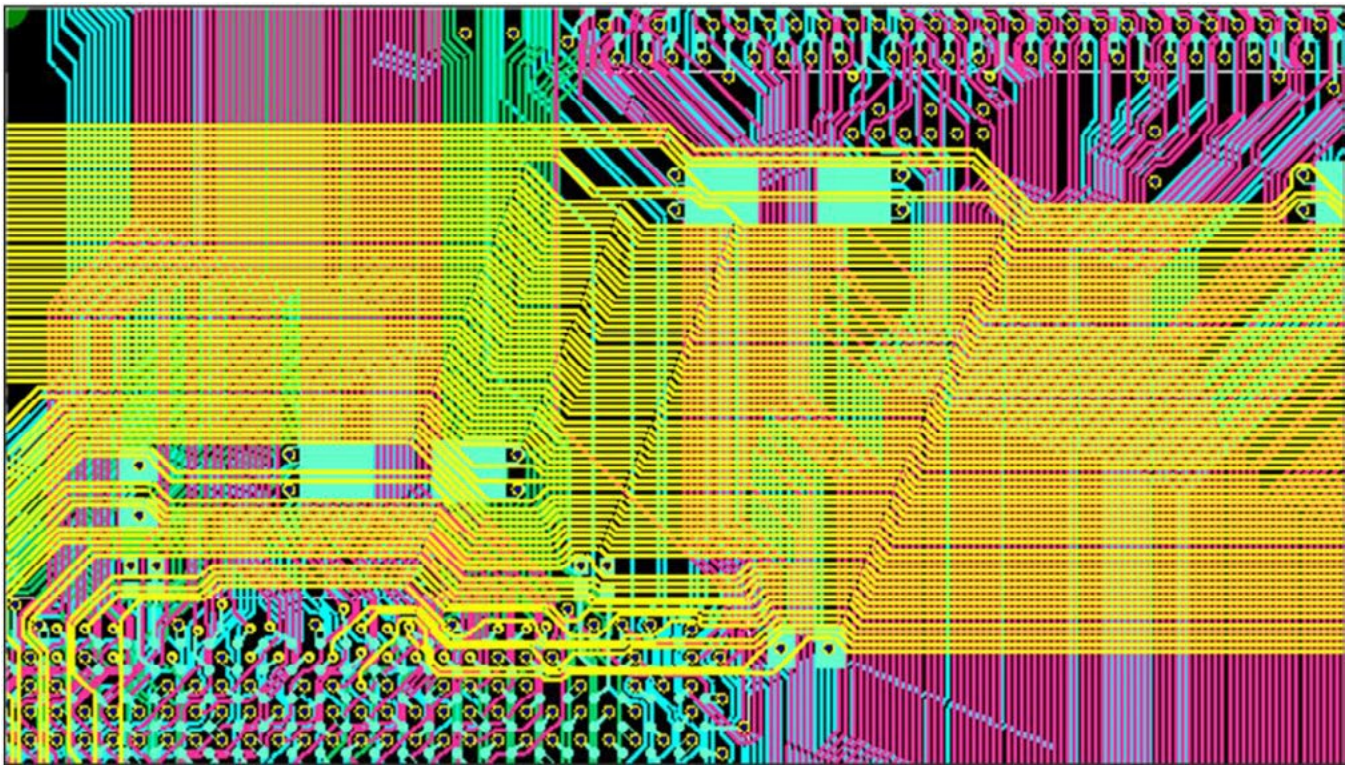


Figure 3: Sketch router quality that matches manual routing.

ing, pad entry and eliminating extra trace segments. In reality, the time spent making these adjustments is comparatively insignificant in the context of routing the entire design. Each designer has a slightly different idea about what conditions warrant these additional adjustments. It is our expectation that the sketch routing environment will provide 99% of the desired quality and if that isn't good enough, we should feel free to continue with those OCD tendencies.

Video Examples

Board routing is something that can be expressed much better in a video example than describing with text. Here is a short video that looks at PCB layout quality in terms of both objective quality and the subjective quality, culminating in efficient routing.

Summary

Sketch routing environments with interactive routing tools like plow and the sketch router, along with the powerful tuning capabilities, are all focused on providing both objective and subjective quality results. During the development of the sketch routing environment, considerable effort has been applied to ensure that the routing results have both the objective and subjective quality as seen with manual routing. Again, this enables the designer to get the desired results in a much faster time because of the attention to quality during the interactive process.

The next article in this series describing sketch routing address routing performance. Don't miss it. **PCBDESIGN**

Charles Pfeil is an engineering director in the Systems Design Division at Mentor Graphics. He was the original product architect for Expedition PCB and an inventor of XtremePCB. Pfeil has been in the PCB industry for more than 40 years as a designer, owner of a service bureau, and as a marketing and engineering manager at Racal-Redac, ASI, Cadence, PADS, and VeriBest. To contact Pfeil, click here.

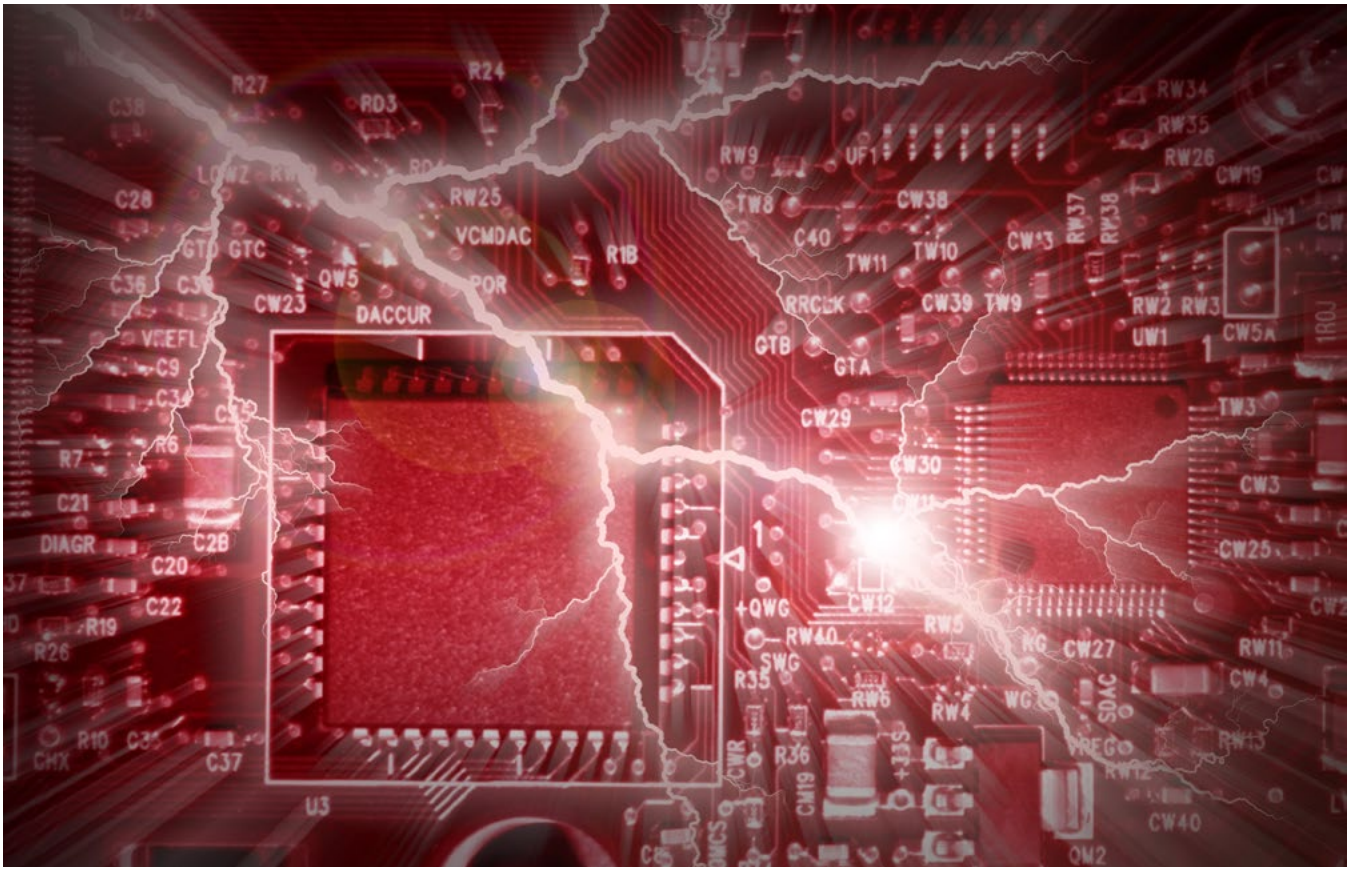
Chilling Out with Conductive Adhesives

by John Coonrod
ROGERS CORPORATION

Conductive adhesives have been around for many years. Some are electrically conductive, others are thermally conductive, and some have both properties. Additionally, the conductive adhesives can be a pressure-sensitive adhesive (PSA) or a thermoset adhesive. To narrow the scope of this month's column, only thermoset thermally and electrically conductive adhesive (TECA) will be discussed.

TECA is often used for heat sink attachment of PCB assemblies when thermal management is a concern. In the RF industry, power amplifiers often generate a lot of heat, and the PCB supporting the power amp is generally attached to a large metal heat sink. The attachment between the PCB and the heat sink is usually done by mechanical attachment with screws, sweat soldering or TECA. Each attachment method has its own set of capabilities and limits.

The mechanical attachment may have air gaps between the circuit and the heat sink, and if these are in critical areas they can make a less efficient heat flow path from the PCB to the heat sink. A less efficient heat flow path can cause the PCB assembly to have a higher temperature than desired and sweat soldering can have similar issues due to voiding. Air gaps are not an issue with TECA when parts are properly bonded using vendor supplied parameters. The drawback to TECA, compared to the other two technologies, is that TECA is usually not as thermally conductive as a metal-to-metal contact. And for RF applications, the heat sink is often used as the system ground and the electrical



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Bare circuit	1.869	3.218	4.479	5.651	1.941	3.355	4.697	5.941	0.072	0.137	0.218	0.29
Circuit laminated to Heat Sink	1.898	3.177	4.464	5.617	1.937	3.315	4.726	5.863	0.039	0.138	0.262	0.246

Figure 1: Test results for TECA films with 50 ohm microstrip transmission line circuits.

connection between the PCB, so the heat sink has to be very good for most RF applications.

The obvious critical material properties for TECA are thermal conductivity and electrical conductivity, but there are other concerns. As general statements, a TECA material with thermal conductivity of 3 W/m·K or more is considered good, and electrical conductivity with a volume resistance value of 0.0005 ohm·cm or less is considered good. Regarding other properties, TECA with good bond strength to different metals and robustness to lead-free solder reflow may be important.

Having TECA bond well to different metals is beneficial for bonding to heat sinks made with different metals and/or the different final plated finishes on a PCB, which will be bonded to the heat sink with the TECA. There have been TECA materials in the PCB industry which were not robust with lead-free soldering; they were still useful for heat sink attachment, but had special processing considerations.

Lastly, electrical performance will be more challenging for RF applications. The electrical conductivity of TECA will be important for DC or low-frequency applications, but is even more critical for RF applications. With RF applications, the ground plane of the PCB must be extremely well connected to the ground of the system, which can be through the heat sink. In these cases, at high frequencies, small anomalies in the grounding between the PCB and the heat sink can cause an increase in system noise and insertion loss. These small electrical anomalies may not be detected at lower frequencies or DC, but they can be very problematic for high-frequency systems. When using TECA in this manner, the surface treatment of the bond surfaces should be considered. A gold surface will provide the best electrical bond interface.

Another concern for TECA used in high-frequency applications is the possible variance of the ground return path due to the conductivity changing with a change in temperature. TECA uses conductive fillers to make the electrical connection through the volume of the material. When TECA is heated, it will expand and the fillers may move farther apart, causing less connection or less conductivity. This generally changes little with electrical conductivity, but with high-frequency applications it can be detectable. Knowing how much the electrical conductivity will change for TECA, a change in temperature should be understood for RF applications.

Laminate providers now offer TECA films. Rogers Corporation's COOLSPAN TECA Film has been tested for all of the concerns mentioned in this column. It is robust for lead-free soldering and bonds well to any metal evaluated thus far. High-frequency testing has been conducted using 50 ohm microstrip transmission line circuits and across a range of microwave frequencies. The table in Figure 1 shows a summary of these circuits, and it can be seen that there is no significant difference for insertion loss from room temperature to 65°C across the range of frequencies tested.

There are several options to attach heat sinks to PCBs, and TECA materials are being used more often. Even though the other options are usually higher in thermal conductive because they use metal or direct metal-to-metal interface, TECA is generally more consistent for heat flow path, relatively easy to apply, and comparable to the RF electrical performance of other options. **PCBDESIGN**

John Coonrod is a market development engineer for Rogers Corporation, Advanced Circuit Materials Division. To read past columns, or to reach Coonrod, click here.

IBM Seeking the Next Generation of Technologists

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Matt Kelly of IBM explains his company's strategy for attracting more young technologists. Kelly believes that getting engineering students involved in their local SMTA chapters can go a long way toward making them feel more confident and less nervous among the older, more experienced engineers.

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New Mechanism of Photoconduction for Next-gen Devices

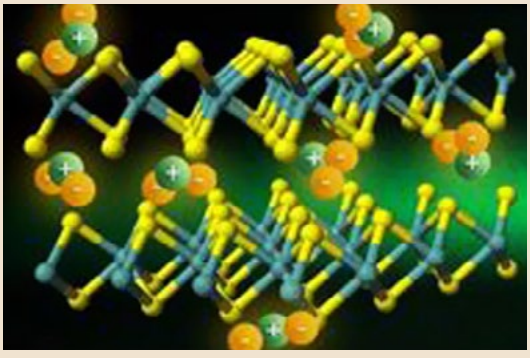
Shining light on a semiconductor will make it more conductive. But now researchers have discovered that in a special semiconductor, light can have the opposite effect, making the material less conductive instead.

The phenomenon was discovered in an exotic two-dimensional semiconductor — a single layer of molybdenum disulfide (MoS_2) just three atoms thick. The finding is reported in a paper inPhysical Review Letters by MIT postdoc Joshua Lui; Nuh Gedik, the Lawrence C. and Sarah W. Biedenharn Career Development Associate Professor of Physics; and six others at MIT, Harvard University, and in Taiwan.

When a semiconductor is illuminated by light, its conductivity tends to increase. This is because light absorption generates pairs of loose electrons and holes—places in a material with "missing" electrons—that facilitate the flow of electrical current through the material.

The MIT team, however, observed the opposite behavior in a two-dimensional semiconductor. In single-layer MoS_2, trions have the same net charge as an electron, but a mass roughly three times that of an electron.

Instead of increasing the population of free charges, the illumination actually converts the original free electrons into heavier trions with the same charge density. This is the reason for the reduction of conductivity of single-layer MoS_2 under illumination.



So far, the team has only studied the effect in MoS_2, which belongs to a family of new two-dimensional semiconductors. "There are other types of two-dimensional materials with [similarly] strong trionic effect." Lui says. "They are likely to exhibit the same photoconduction phenomenon."

Mil/Aero007 News Highlights

Microtek Earns DLA Laboratory Suitability Status

The company's Linthicum Heights, Maryland facility has received Laboratory Suitability Status approval from the DoD DLA for MIL-I-46058, MIL-PRF-55110, MIL-PRF-31032, and MIL-PRF-50884. With this approval, the lab can now perform all applicable Group A, Group B, Group C conformance and reliability testing as well as full qualification testing for these specifications.

Invotec Gets Support for "Sharing in Growth" Program

The company is delighted to announce it has been approved by the government-backed Sharing in Growth (SiG) program. SiG is designed to enhance the competitive capabilities of selected companies within the UK aerospace supply chain, helping them to tackle barriers to growth, boost exports, and create more than 5,000 jobs within the UK's high-value manufacturing sector.

Amitron Named Truck-Lite's "2014 Supplier of the Year"

Truck-Lite Co. LLC has recognized Amitron Corporation by awarding their "2014 Supplier of the Year" to the Illinois PCB manufacturer. In a letter to Amitron, Truck-Lite's Vice President of Worldwide Purchasing Martin Schroeder stated that the award was for Amitron's "exceptional performance in the last 12 months in the areas of quality, delivery, technology and commercial competitiveness."

All Flex Achieves Re-cert to AS9100C, ISO 9001:2008

All Flex, a manufacturer of flexible printed circuits and heaters, announces re-certification to AS9100C and ISO 9001:2008.

Capital Electro-Circuits Reaffirms Commitment to Quality

Capital Electro-Circuits Inc in Gaithersburg, Maryland, is pleased to announce the successful completion of its ISO 9001:2008 re-certification. President Bharat Sitapara said, "This is a continuation of our ongoing commitment to maintain our excellent quality and to improve our quality wherever it is needed."

i3 Nets Contract to Supply Substrates for Military Use

i3 Electronics Inc. has announced that an industry leading aerospace and defense firm has awarded the company an order for the supply of advanced substrates for a military application. The order will run through the remainder of 2014.

Cicor Sees Positive 1H Amid Challenges in AMS Division

The Advanced Microelectronics & Substrates (AMS) Division experienced a difficult start into 2014, which resulted in a decline in sales due to the still challenging market environment in the Eurozone's aerospace, defense, and nuclear energy sectors, as well as the loss of sales in relation to the manufacture of an end-of-life product.

Military Radar Market to See CAGR of 2.9% 2013–2019

Driven by continuous growing threats from both the internal and external sources, global market for military radar was valued at US $6,900 million in 2012 and is expected to reach US $8,440 million by 2019, growing at a CAGR of 2.9% during the forecast period from 2013–2019.

Aerospace Industry's Sensor Market at $2.44B in 2020

New analysis from Frost & Sullivan, "Analysis of Sensor Market in the Global Aerospace Industry," finds that the market earned revenues of $1.24 billion in 2013 and estimates this to reach $2.44 billion in 2020.

U.S. GDP to Grow 3% by 2016; Defense Spending Rises

UCLA Anderson Forecast's third quarterly report of 2014 indicates that the real Gross Domestic Product for the United States will grow at approximately 3% over the next two years, following a decline of 2.1% in the first quarter of this year and a rebound of 4.2% growth in the second.

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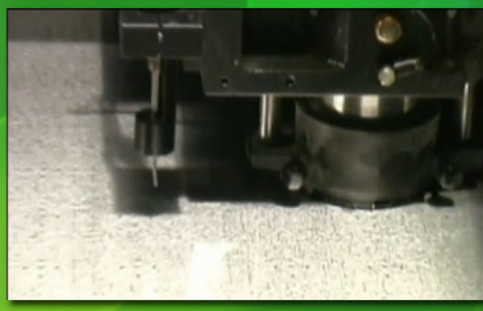

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Tarzwell's First—and Last—Lean Meeting

by Bob Tarzwell with Dan Beaulieu

Dan Beaulieu: While we were working with one or our clients a few years back, the firm decided to get involved in the whole Lean manufacturing thing. They were a big enough company that they were able to hire the real guys: the ones who had gone to Japan to work with Toyota and then had written a book about it. They later sold their ideas to a number of large companies including the one we were working with. Now they were here and in our face! We were told that as part of our gig, we were going to have to play nice with these guys.

Out of all my guys, Bob Tarzwell was the first of my team to attend one of these Lean meetings. This was possibly the worst guy we could have sent, but I knew that and our contact at the client's office knew it too, so they could play their games and we could play ours.

I'll let Bob tell you all what happened, in his own inimitable way.

Bob Tarzwell: First, the "Lean lady" asked everyone what they did and how long it took them to do it. Then there was someone who, for some reason that I could not figure out, brought up the fact that the shelves were in the wrong place and that if they were in the right place it would increase the efficiency of the department. So, acting as proactively as they could, they took all of us to stare at those shelves and then held a brainstorming session on what we should do. Have you ever seen a decision tree? A fish scale pattern thingy? (Figure 1.) Well, they started working on one of those for those shelves. Actually, I have to say that moving the shelves was a pretty good idea, and they should have just done it instead of talking about it for hours.

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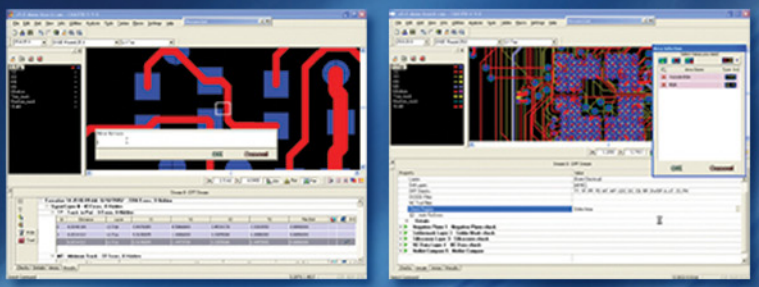

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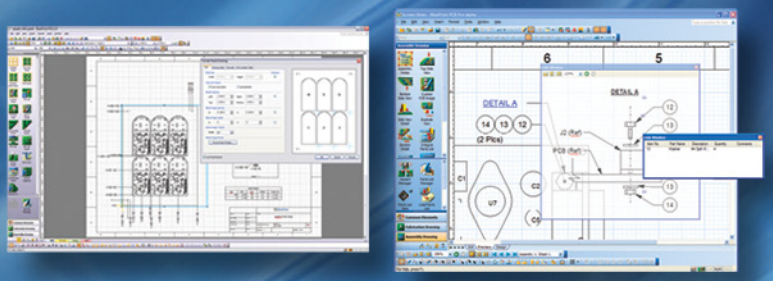

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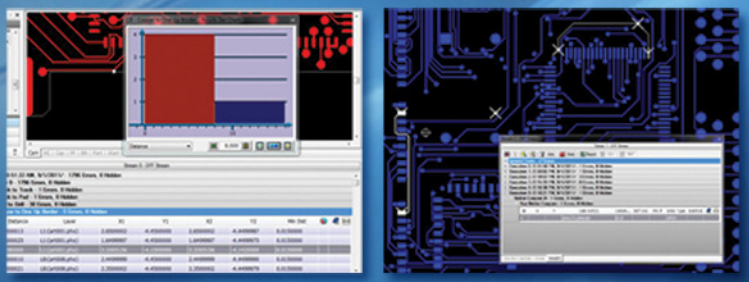

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TARZWELL'S FIRST—AND LAST—LEAN MEETING *continues*

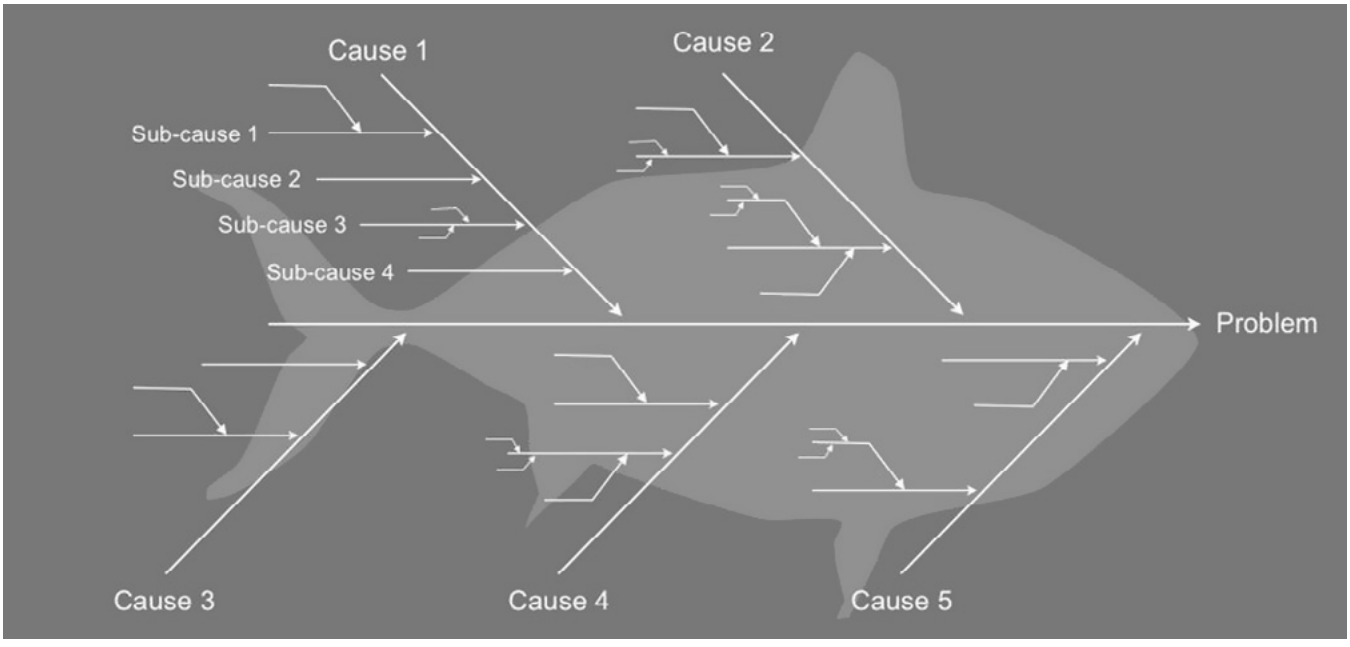


Figure 1: An example of an Ishikawa fish diagram designed to help break down the causes of problems. In this case, it may have caused Tarzwell to have a breakdown.

But there was only one problem with moving the shelves: A fire extinguisher hung exactly where we wanted to move them. Now, that brought everything to a stop.

First, there was a big discussion about where fire extinguishers were supposed to go, how they were supposed to be hung, how high they were supposed to be hung, and how near the door frame they were supposed to be.

They sent someone out to find an OSHA rule booklet and then they started looking at that. It was such a waste of time. I wanted to kill somebody—either myself or maybe the facilitator.

These people were discussing this with all of the seriousness in the world. They were acting like this was one hell of a real problem and that we should spend the right amount of time and do this right.

After about 20 minutes on this subject, the Lean lady sent someone back to get her big pad of paper from the easel in the conference room and bring it into the quality department. That's when she started talking about this "decision fish" thing again. She asked for suggestions and then wrote everything down on the fish scales. One side had the pros and the other the cons. Man, it was horrible.

After 45 minutes of this, I had had enough. I grabbed the fire extinguisher, brought it over to where it should be, held it up, marked the spot with my pen, and told them that this was where they needed to put it.

Then I walked out of the room. I was done. I thought, if you ask me to go in there again, I'm going home. I've lost enough brain cells for one day.

I am done. I have retired from this Lean bullshit for the rest of my life.

Inventing the Super Board

Bob Tarzwell: One of my best inventions took four years. During a routine thermal reliability study, one panel stood out as virtually indestructible over 3,000 thermal cycles, compared to the other four, which all showed normal 200–400 cycles-to-failure. For some reason, this one panel, which for all known reasons should be the same as the other four panels, passed the toughest thermal stress tests with flying colors when its accompanying three panels were normal.

I studied the panels, cross-sectioned them, looked, pondered and kept it secret. I carried those panels with me for years. I kept experi-

menting with them and continued pondering about it. Then one day I saw the difference. It was as clear as mud! It was so simple I missed it, like missing the forest for the trees. The one great panel was made with a mistake and the operator tried to fix it, hiding a problem that he created.

In reality, he unknowingly created a super board! I re-created the difference with a new test panel and got the same results—another super board! Wow. I could not make these vias crack.

Via cracking is one of the single biggest problems in our business, and I found a simple, easy trick to solve it. Soon, the idea was sold, and it is now on the market.

Not all inventors are normal; I have been told that many times. I don't get along well with big stiff companies. I don't wear suits; I don't fit the normal engineer mold. I invent way-out ideas; I think in outer space. I would have fit in fine in a "skunk works" R&D department decades ago.

So what's the simple trick to making a super board, and why would I tell you now? Because the fact is, it's so simple that most people won't even believe it. That's how I know my secret is safe, because you probably won't even attempt it.

Not all inventors are normal; I have been told that many times. I don't get along well with big stiff companies. I don't wear suits; I don't fit the normal engineer mold. I invent way-out ideas; I think in outer space. I would have fit in fine in a "skunk works" R&D department decades ago.

Here it is: The big/little secret is a physics attribute called Young's modulus. In short, Young's modulus is a measure of how hard a material expands with heat, or how hard it pushes as you heat it. We all talk about CTE, and, in fact, far too many articles work CTE to death. Yet none mention Young's modulus, its silent partner.

Here's an easy way to understand how important Young's modulus is. Let's do a simple experiment: Take a hunk of FR-4, tighten it in a vice, heat it up, and nothing will happen. But take a hunk of steel, tighten it in a vice, heat it up and watch it break the vice. FR-4 only expands in the Z-axis with 3 million pounds per square inch (21 GPa) of force when being heated, but steel expands at 30 million pounds (200 GPa) of force, pushing (or resisting) 10x harder than FR-4 as it expands. Copper pushes with 17 million pounds per square inch (17GPa), nearly six times more than FR-4.

When the FR-4 board is expanding in the Z-axis, it's got just enough expanding force to rip apart the thin copper in the hole; even though copper is six times stronger, it's also thin, so it stretches and cracks. If the copper is thin enough, less than about 1 mil, it will cause cracking with thermal cycles. The expanding FR-4 in the Z-axis will cause the top of the copper via pad to tilt up as the FR-4 tries to expand faster than the copper, with the copper wall resisting. When we put 1.8 mils of copper in the hole, it stops a lot of the upward movement of the copper hole wall and therefore reduces pad movement and hence the reduced cracking of the copper via.

Note: This 1 mil cliff edge of failure we stand perched upon also just happens to be right dead in the middle of where we plate our holes.

If the board shop happens to put a bit more copper in the holes, you'll have a PCB that will survive more thermal cycles. But if they are a little skinny in the plating, your PCB will fail earlier. This is how close to the cliff edge we have been standing for the 50 years I have been in PCB manufacturing. So who decided that 1 mil of copper in the hole was a standard back in the beginning? No one said, "Hmm. How much copper do we put in the holes to give the circuit a long life?" We just plated what we could back in the '60s; there were no tests to see how much copper will survive thermal cycles. It just happened, and it continues today.

A simple, little change like starting with thinner base copper and then adding 2 mils of dry film and plate-up close to the top of the dry

TARZWELL'S FIRST—AND LAST—LEAN MEETING *continues*

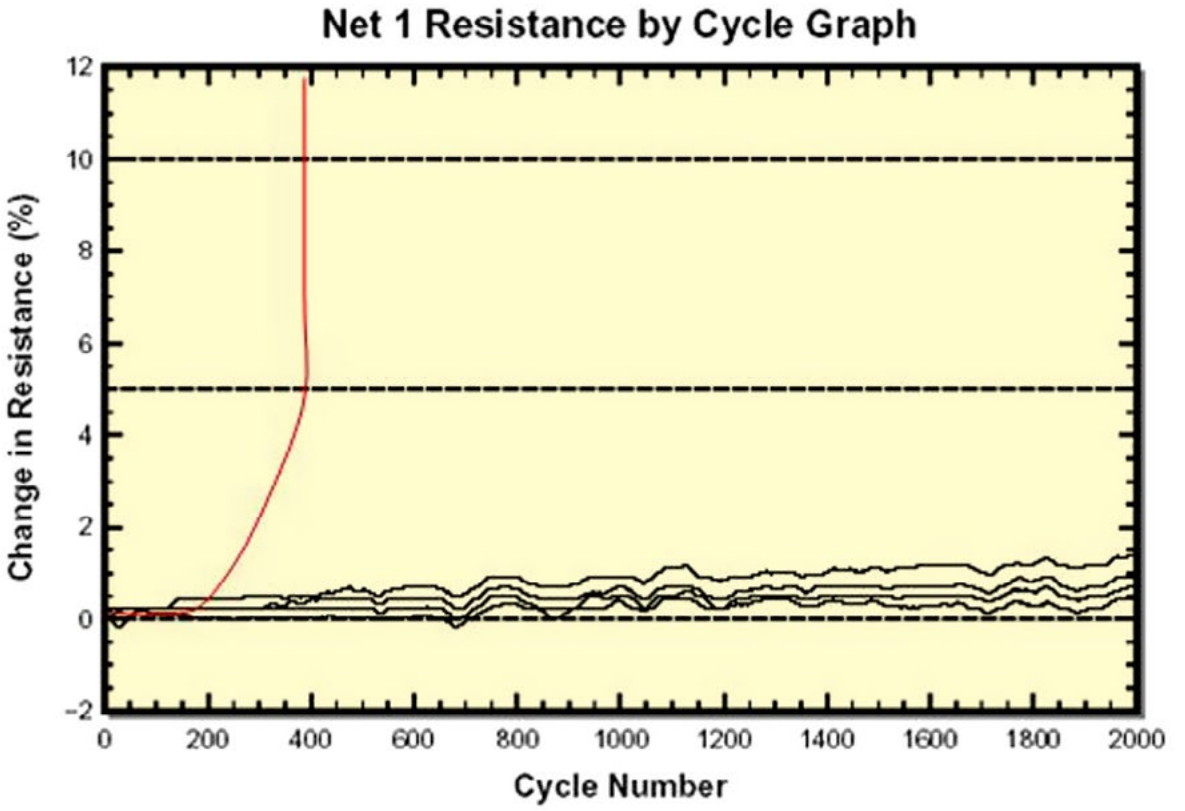


Figure 2: Red line is a normal 1 oz. copper-plated board; the black lines are 2 oz. copper-plated boards.

film will result in a very tough, high-reliability thermal cycle PCB. The 2 mil dry film can take the extra copper plating and still give a sharp edge. With the thinner base copper, you etch less and get finer lines and higher yields for free.

The super board I mentioned had 1.8 mils of plated copper in the holes. The operator was trying to compensate for an error: One panel out of four had been wrongly laminated with thin base copper of only 5 microns, not the half-ounce copper called for in the build sheet.

The plating operator must have measured the copper thickness, and to make it look like a normal board, he plated more copper to compensate for the thin base copper that was accidentally laminated on. He did not tell anyone and off the panels went for thermal testing.

Later, I got a call from our test operator.

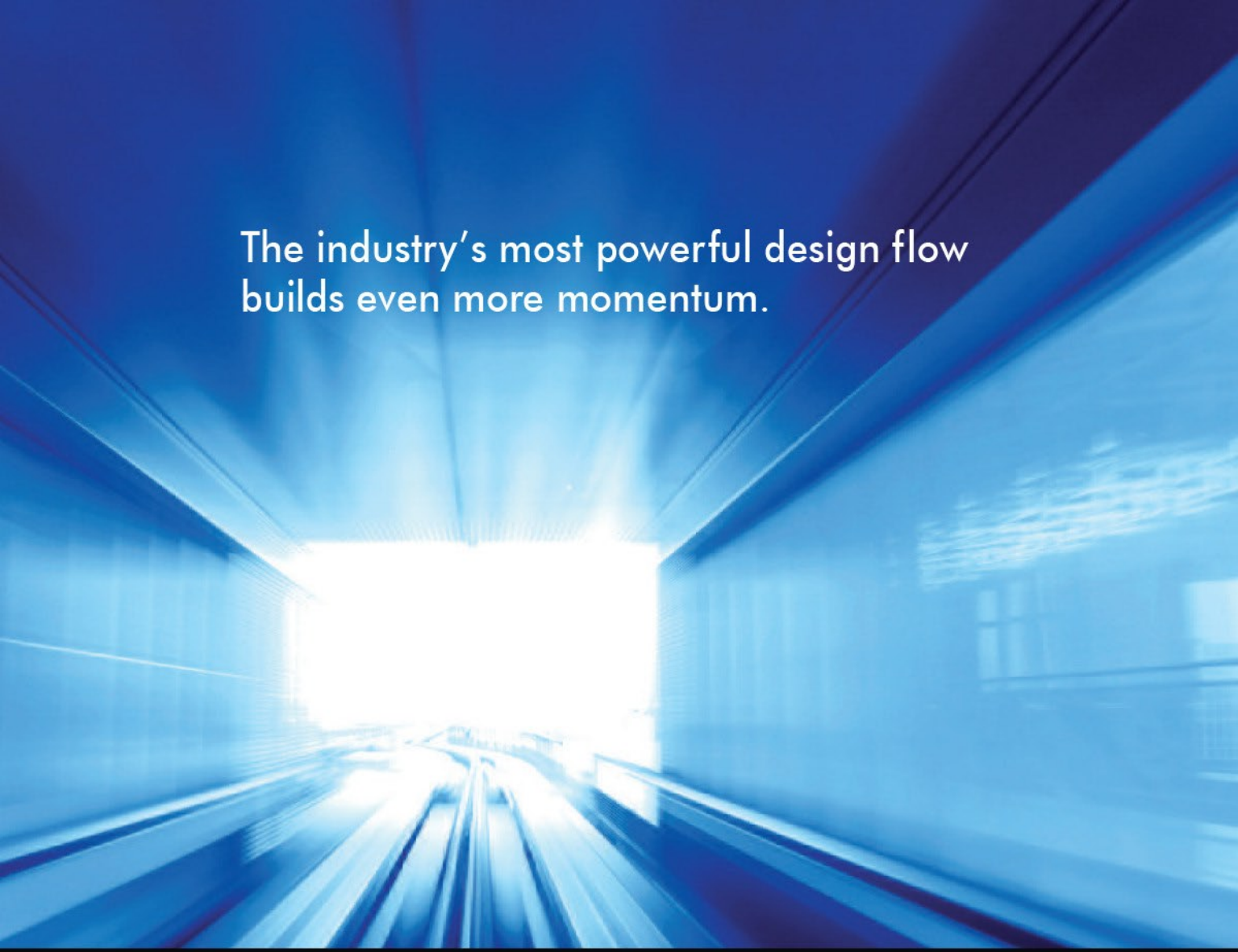
"Can I take this set off the tester? It's been on for three weeks and it's not even close to failure, and I need the machine."

So, the big secret is this: If you want your PCB to survive more thermal cycles, just add more copper to the plating in the holes or microvias. It's as simple as that.

See you next month. **PCBDESIGN**

Bob Tarzwell is a PCB consultant who has spent 50 years in the PCB industry, inventing technology and building almost every type of PCB. He is the co-owner of DB Publishing, publisher of the *PCB 101 and Quality 101* handbooks. For more information, visit www.dmrpcb.com.

Dan Beaulieu is a well-known industry consultant and co-owner of DB Publishing. His column *It's Only Common Sense* appears Monday mornings in the I-Connect 007 Daily Newsletter. He can be reached at danbbeaulieu@aol.com.



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Blink and You Will Miss It

by Tim Haag
INTERCEPT TECHNOLOGY

The year was 1987. I was married, owned my own home, and our first child was a year old. Life was great—better than I could have ever imagined. And then it happened: I got laid off. This was the company that I had planned on being employed with forever, and yet they showed me the door. I was devastated. My career as a circuit board designer, which had just started, was now in serious jeopardy.

Was I going to lose my house? Could I support my wife and child? Was this an indication that I couldn't cut it in my chosen profession? I was 27 years old, and it was one of the lowest points that I had ever experienced.

I knew one thing for sure though; I did not want to work as a contract board designer. I didn't want to go from job to job, I didn't want to give up on the perks that I had enjoyed at my previous company, and I didn't want to pay for my own benefits. I wanted the security that I had become accustomed to and I wanted my future to continue as I had planned it out. To be honest, though, I was scared of what was around the next corner. But since full-time jobs for junior designers were not in abundance, I was forced to widen my search for work. Eventually, I would end up full-time at a service bureau, which is where, for the next seven years, my career as a board designer really took off. But before I got that job I spent three months as a contract board designer—exactly what I said that I would never do.

Isn't it funny how that tends to happen a lot in life? The scenarios that worry us, the ones that we try our best to avoid, are often what we end up facing. Friedrich Nietzsche said, "That which does not kill us makes us stronger." Well, that adage certainly proved to be true in my situation. If I hadn't been ripped from my secure position and forced to contract for a short season, who knows how my future would have eventually unfolded. And if it hadn't been for that brief season of hardship, would I have had the strength and flexibility to succeed later on? I wonder how often it happens that the season of challenge that we are confronted with in

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BLINK AND YOU WILL MISS IT *continues*

the moment is exactly what we need to help us grow. It can be really easy to miss the big picture of moments in our lives because we are so tightly focused on the problem that is right in front of us..

Some years back I was teaching a CAD class in Ontario, Canada, and decided that I should visit Niagara Falls. I had never seen the falls before and since I didn't know if I would return to the area again, I decided to go for it. It was a two-hour drive from my hotel and I arrived in the early evening. As I was driving into the area of the falls, I could tell that I had arrived by the mist in the air and the amount activity that was going on, but I couldn't see the falls yet. Then, as I got within viewing range, I wasn't able to actually look at the falls because I had to concentrate on driving in order to avoid running over the dozens of pedestrians who were crossing in front of me without paying attention. I found a place to park across from the visitor center, which happened to be blocking my view of the falls, and crossed the street to go inside. While looking at the information, I noticed that the visitor center had advertised a special on viewing the falls from behind the falls. This sounded very intriguing; I paid the price of admission and entered the building. The key here is that I am now inside the visitor center at Niagara Falls, and I still have not actually seen the falls.

As I remember it, you descend some stairs, then take an elevator down, then descend some more stairs to finally find yourself in a tunnel that braches out in two directions. One tunnel led to the viewing platform and the other to see the advertised "falls behind the falls." Since that is what I had come down to look at, I took the branch that led me to the area where you could see the falls from behind the falls. After walking to the end of the tunnel so see this amazing thing, it turned out to be a big…disappointment. I had been hearing about Niagara Falls all my life and was eagerly looking forward to this incredible marvel, and yet my first official look at the falls was something about the size of a shower door with falling water behind it. As I stood there looking at this "shower," the thought that was running through my mind was, "This is it? All this way for one of the greatest spectacles of nature known to the world, and this is it?"

Figure 1: One view of Niagara Falls.

So what had happened? Niagara Falls hadn't changed, but my expectation was unfulfilled. If I had been able to see it while driving in, I would have seen the awesomeness of the falls from a distance. If I had paid more attention while walking down the tunnel I would have noticed the mist in the air, the water dripping from the roof of the tunnel, and the thunderous noise of the falls reverberating all around me. And I should have especially noticed how all of us were dressed in those fashionable yellow rain slickers. But no, I only focused on what was in front of me at the moment, a shower-sized window with a view that wasn't at all what I expected.

Later I retraced my steps and took the tunnel to the viewing platform and there was the view that I expected; Niagara Falls in all of its strength, power and glory.

This served as a great lesson to me: Just because what we see in front of us at the moment isn't what we expect, it doesn't mean that what is beyond it will be a disappointment. Sometimes we just need the patience and perseverance to succeed where we are currently before we will have the strength and skills to move on to the next step.

When I took that contractor job that I tried so hard to avoid, I had no idea that I was helping to lay the skills that I would later rely on

Figure 2: A better view of the falls.

in for my future career. In that short contract, I worked with a team of software engineers that were enhancing a little in-house CAD tool that they had developed for their own specialized boards. I would never have dreamed that 14 years later I would leverage that experience while working for a CAD company where I would be helping customers to excel at their jobs using our advanced applications.

I also had no idea that the simple little tape-up boards that my contract job started me with would one day give me a greater appreciation for the history of our industry and better insight to help users as they transition from older design techniques to more modern ones. And I never would have imagined that that little contract job would flex my design skills, getting them ready for the larger jobs and more advanced technologies that I would later face. Where would I be today if I hadn't been forced to leave what I thought was safe and secure so that I could get out of the box and grow in my skills and abilities?

Many of these kinds of situations cross our paths, and we need to be ready to learn and grow from them when they present themselves. Blink and you might miss what is right in front of you. **PCBDESIGN**

Tim Haag is customer support and training manager for Intercept Technology.

News Highlights from PCBDesign007 this Month

① Zuken Intros CADSTAR Essential PCB Design Suite

Zuken has launched an entry-level schematic and PCB design bundle as part of the CADSTAR family of products. CADSTAR Essential is a complete schematic and PCB design tool suite that allows PCB designers and engineers to download software, learn the basics, and start designing as quickly as possible.

② PCB and MCM's 20% Growth Boosts EDA Industry

"Double-digit increases in PCB/MCM and semiconductor IP led the way to an overall increase in industry revenue for Q2," said Walden C. Rhines, board sponsor for the EDAC MSS and chairman and CEO of Mentor Graphics.

③ Keysight Technologies Introduces DDR Bus Simulator

"Individual simulations are both fast and accurate, allowing designers to run in batch mode and quickly explore the design space," says Colin Warwick, product manager for signal integrity tools at Keysight EEsof EDA. "In addition, we offer DDR Bus Simulator Distributed Computing 8-pack licenses so users can farm out their parameter sweeps to a compute cluster for an even shorter time-to-answer."

④ PCB West Registration Up 6% Year-on-Year

PCB West show registration rose 6% year-over-year, reaching nearly 2,600 registrants and over 90 exhibitors, according to UP Media Group. It was the annual PCB industry trade show's highest registration since 2001. Actual attendance was up 4% from 2013.

5 Pegatron Builds PCB Design Flow; Partners with Zuken

Pegatron is now offering contracted design and manufacturing services to its customers through direct utilization of CR-8000 and CR-5000 data. They will exchange design data with their customers in CR-5000/CR-8000 data format. In addition to circuit board patterns, use of CR-8000 and CR-5000 data enables the direct transfer of design constraints specified by Pegatron customers.

6 Agilent Board Approves Separation of Keysight

Agilent Technologies' board of directors approved the separation of its electronic measurement subsidiary, Keysight Technologies Inc., and declared a special dividend distribution of all outstanding shares of Keysight's common stock to Agilent's shareholders.

7 EDA Industry Recognizes Dr. Lanza with Phil Kaufman Award

Dr. Lucio Lanza, managing director of Lanza techVentures, has been selected by the EDA Consortium and the IEEE Council on EDA as the recipient of the 2014 Phil Kaufman Award for Distinguished Contributions to Electronic Design Automation.

8 IEEE Symposium on Future Tech Opens Registration

Leading futurists, innovators and industry luminaries will convene at the Dolce Hayes Mansion in San Jose, Calif., 21-22 October, to debate with attendees on a 2035 vision for the global interplay of science, technology, society, and economics.

9 PCB Design for Signal Integrity, EMC Course Announced

Omniscient International will be holding a two-day seminar focused on printed circuit board design for signal integrity and EMC compliance. The event, to be held October 21-22 at the Grand Pacific Hotel in Singapore, will feature case studies, exercises, and practical applications.

10 DesignCon 2015 Opens Registration; Marks 20 Years

DesignCon is the largest gathering of chip, board and systems designers in the country. The 2015 event boasts 14 innovative tracks designed to enable designers, software developers and silicon manufacturers to hone their skills and learn from the brightest in the industry.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out *The PCB Design Magazine's* event calendar.

Austin CTEA Expo & Tech Forum
October 14, 2014
Austin, Texas, USA

Long Island SMTA Expo and Technical Forum
October 15, 2014
Islandia, New York, USA

Connecticut Expo & Tech Forum
October 21, 2014
Waterbury, Connecticut, USA

Intermountain (Utah) Expo & Tech Forum
October 23, 2014
Salt Lake City, Utah, USA

Industrial Automation Conference 2014
October 23–24, 2014
London, UK

LA/Orange County Expo & Tech Forum
November 6, 2014
Long Beach, California, USA

International Wafer–Level Packaging Conference
November 11–13, 2014
San Jose, California, USA

TSensors Summit 2014 – San Diego
November 12–13, 2014
La Jolla, California, USA

Wearable Sensors and Electronics 2014
November 12–13, 2014
Santa Clara, California, USA

ELECTRONICA 2014
November 11–14, 2014
Messe Munchen, Germany

Graphene LIVE! 2014
November 19–20, 2014
Santa Clara, California, USA

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