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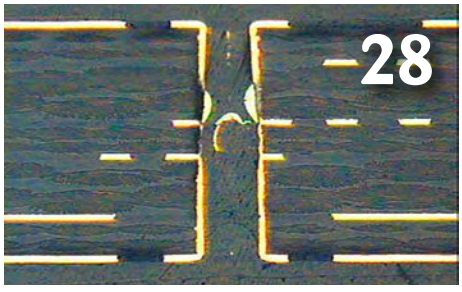

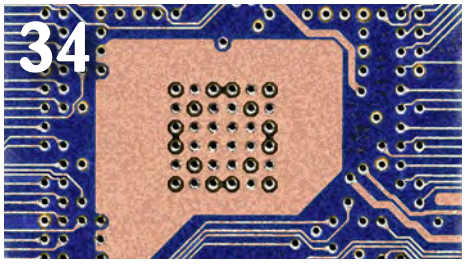

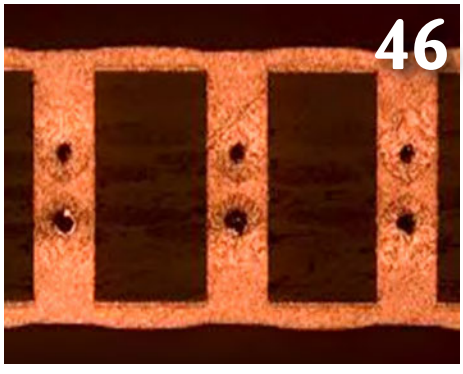

Plating and Surface Finishes

So what is new in plating and surface finishes? This month, our experts weigh in on new processes, the tried-and-true old processes, R&D, and how to go about choosing the right process from among all those available today.

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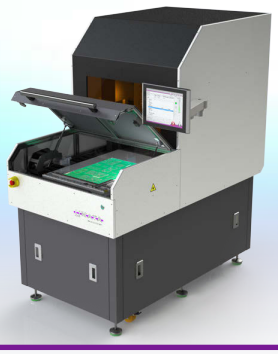

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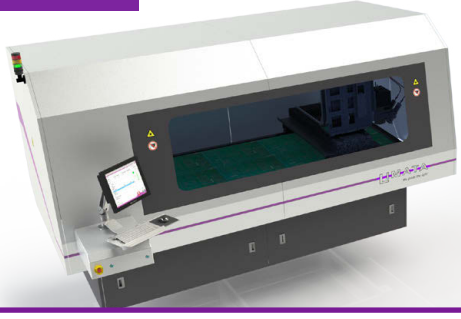

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Everything Old is New Again

by Patty Goldman
I-CONNECT007

Happy New Year to all of you faithful and new readers out there! I hope you are looking forward to 2017 as much as we are here at I-Connect007. We have exciting plans for this year and can't wait to get started, but first we need to talk about this month's topic.

This month's issue is all about plating and surface finishes; long ago, that was pretty much my start in the world of printed circuits—wet processing. So this is kind of my home turf—and not, since I haven't worked in wet processing for some…well, for many years. I've always expected that I could hop right back onto the plating room floor and pick right up where I left off all those years ago. Or could I? Have things changed much? Time to read on and see.

So what is new in plating and surface finishes? Well it's true that there are still the basic processes—cleaners and microetches, copper and nickel and gold electroplating, immersion tin, nickel, silver—all of which have been around for quite a long time. But with the finer features, the far greater reliability concerns, the lead-free solders, the constant need for lower cost and greater efficiency, etc., the spotlight is often on these "old" processes. Plus, there are a few new ones like ENIPIG.

Much research and development has gone into refining additives for electroplating and electroless/immersion baths to improve the plating quality in one way or another, both on surfaces and in through-holes and vias. Following on that is a tremendous amount of testing to prove out said processes and the subsequent assembly-ability of components. In the end, it's all about reliability, reliability, and reliability.

There are a plethora of final finishes to choose from today. How does one decide? Well, that takes us right to the line-up for this month. Regular columnist Tara Dunn of Omni PCB has

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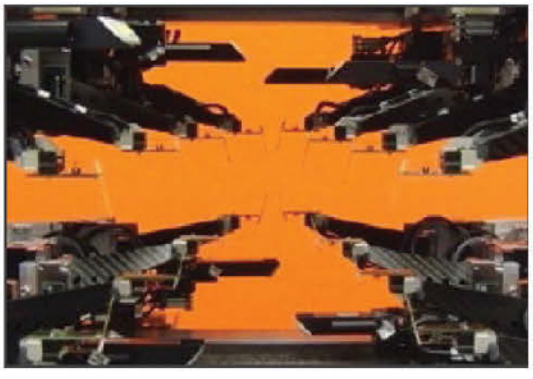

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chosen that very subject so it seems appropriate to start with her column on how to choose a final surface finish.

Following this is a study of immersion gold processes—some of that R&D work I mentioned earlier. Don Gudeczauskas, et al, of Uyemura International, present a fine research paper on a comparative study of three immersion gold processes, looking at both solderability and wire bondability.

Lest anyone think that wet processes have no effect on electrical test, Gardien Services' Todd Kolmodin is here to set the record straight with a look at the challenges that plating and surface finishes present to electrical test.

RBP Chemical Technology's Michael Carano is Mr. Plating himself, and he gives us a detailed look at some of those things you might tend to overlook or perhaps take for granted in your acid copper plating process. Rather than talk about controlling the typical constituents, Mike looks beyond at tank parameters and the surrounding process steps.

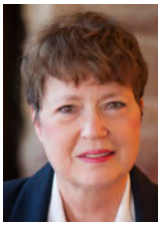
We are fortunate to have another R&D article, this one by Ron Blake, et al, of MacDermid Enthone Electronics Solutions. They get into another relatively new area for copper electroplating, the filling of through-holes with copper.

Next, our own Pete Starkey reports on a MACFEST development project on a "universal surface finish," namely ENIPIG (electroless nickel/immersion palladium/immersion gold). This detailed report—including ample test data—has also been recorded as a webinar and can be viewed by clicking on the link near the end of the article.

In keeping with our policy of having a few general interest items for those chemistry-phobes out there, we have no less than three columnists weighing in on the U.S. presidential election—in vastly different ways. IPC President John Mitchell starts with a discussion on how the Trump presidency and potential policy shifts may affect the electronics industry. He is followed by guest columnist John Hasselmann, IPC's VP of Government Relations, with a discussion on corporate tax policy and possible changes that may come about with the new administration in Washington, DC.

Regular columnist Barry Lee Cohen compares the "fake news" from this past presidential campaign to the potentially false news that can and probably does occur within and about your own company. Barry also provides some concrete advice on how to keep the communication lines open so news and other information can be quickly disseminated—and any false "news" can be immediately combatted.

IPC APEX EXPO 2017 happens next month (see our calendar of events) and what better time to have our magazine focus on new technology—our topic for February. We expect there to be plenty for you to read about. You can subscribe now and have *The PCB Magazine* delivered to your inbox every month, giving you a head start on all things PCB. **PCB**



Patricia Goldman is a 30+ year veteran of the PCB industry, with experience in a variety of areas, including R&D of imaging technologies, wet process engineering, and sales and marketing of PWB chemistry. Active with IPC since 1981, Goldman has chaired numerous committees and served as TAEC chairman, and is also the co-author of numerous technical papers. To contact Goldman, click here.

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Final Surface Finish: *How Do You Choose?*

by Tara Dunn
OMNI PCB

There are so many final surface finish options to choose from today. How do you decide which is best? HASL—both tin-lead and lead-free—immersion tin, immersion silver, ENIG, OSP, and ENIPIG are the primary finishes used in PCB fabrication. Fabricators and assemblers generally work with the majority of these surface finishes to support their customers' requirements. So the question is, with all of these available, how do OEMs select their preferred surface finish?

In the past, the primary function of the surface finish was to protect the copper from oxidation prior to the soldering of components. Today's expectations also include: superior solderability, contact performance, wire bondability, corrosion and thermal resistance, and extended end use life. Designs have changed. Lines and spaces are reduced, solder types and flux chemistries are different due to no-lead requirements, the number of assembly cycles has increased, and the product may need to carry high-frequency signals.

Things to think about when selecting a final surface finish:

- Does the application require tin-lead or lead-free assembly?
- Will the end environment have extreme temperatures or humidity concerns?
- What shelf life is needed? Will it be months or years?
- Volume and throughput
- Does the design have fine-pitch components?
- How many assembly cycles will be required?
- Is this an RF or high-frequency application?
- Will probe-ability be required for testing?
- Is thermal resistance required?

Once the project requirements have been identified, the surface finish options can be reviewed to find the best fit.

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HASL—Hot Air Solder Leveling

Let's start with HASL. Fifteen or 20 years ago, HASL was the universal go-to surface finish. Today, that is not at all the case. A couple of things greatly influenced this change. The first was RoHS and lead-free requirements. The second is miniaturization and the need for tight-pitch components. HASL is blown from the PCB surface to remove excess; this can create uneven coverage, which makes placement of these tight-pitch components difficult at assembly. This finish is used in aerospace, defense and high-performance electronics as well as lower-end consumer markets.

Things to keep in mind:

- The oldest surface finish
- Tin-lead and lead-free versions are available
- Tin-lead HASL currently in limited use due to RoHS and WEEE initiatives
  - Currently exempt: industrial vehicles, military, aerospace and defense, high-performance electronics
- Leaded versions are harder to source
- Long shelf life
- Not suited for fine pitch

OSP—Organic Solderability Preservative

OSP is the highest volume surface finish worldwide, with applications spanning data/telecom, automotive and both low-end and high-end consumer products. Older versions of this chemistry were not thermally resistant and were not able to resist more than one reflow cycle. Improvements have been made to allow higher temperatures and multiple reflows without degrading. This finish does well as a selective finish. For example, when ENIG is applied as a surface finish and OSP is used selectively, it will not adhere to or stain any of the gold surfaces, so there is no need to plasma clean.

Things to keep in mind:

- Highest volume surface finish worldwide
- Applications range from low end to high-frequency server boards; also used in selective finishing
- The latest versions are copper selective and more thermally resistant for high-temp, no-lead applications
- OSP is applied through chemical absorption on the copper surface; there is no metal-to-metal displacement
- Inexpensive surface finish
- Limited shelf life

Immersion Tin

Applications for immersion tin are predominantly in automotive, U.S. military and aerospace. One caution at the assembly level is the fact that pure tin thickness is lost to the copper intermetallic with time and temperature. Loss of pure tin will degrade solder performance. The first reflow exposure will dramatically reduce the pure tin thickness and deposit stress could result in tin whiskers. This is a naturally occurring characteristic of tin in direct contact with copper.

Things to keep in mind:

- Applications are predominately automotive, U.S. military and aerospace
- Excellent for press-fit applications (i.e., large back panels)
- All contain anti-whiskering additives, but tin whisker elimination is not guaranteed
- Low-cost, flat and suited for fine-pitch use
- Aggressive on soldermask

Immersion Silver

Immersion silver is well-suited for high-frequency applications. It has the greatest conductivity of all the surface finishes and it is flat. The signal travels to the top of the circuit reducing signal loss. This finish is often used in the data/telecom, automotive, high- and low-end consumer and medical markets.

Things to keep in mind:

- Greatest conductivity of all the surface finishes; well-suited for high-frequency applications
- Applications range from low-end to high-reliability product
- Topcoats have been formulated to overcome tarnish and corrosion issues in aggressive environments
- Flat—suited for fine-pitch with excellent solderability

- Easily scratched; sliding connector limitations
- Microvoiding is something to be aware of with soldermask defined pads

ENIG—Electroless Nickel/Immersion Gold

ENIG has become one of the most common surface finishes and is often seen in aerospace and defense, medical, and other high performance markets. It is also predominant in the flex market. While this process requires many processing steps and numerous chemical analyses, fabricators run this process day in and day out with very little issue.

Things to keep in mind:

- Applications associated with high reliability
- Used often in the flex market
- High corrosion resistance due to nickel barrier
- Aluminum wire bondable
- No degradation between reflow cycles; can be held mid-assembly for extended times
- Potential for nickel corrosion (aka black pad) if time in gold bath is excessive

ENEPIG—Electroless Nickel/Electroless Palladium/Immersion Gold

ENEPIG is the new kid on the block. A significant advantage to this finish is that it is gold wire bondable. Typical applications are in the medical and the U.S. military markets. This finish is expensive to process and is still relatively low-volume in the market. Fabricators are slowly bringing this process in-house as volume makes outsourcing less economical.

Things to keep in mind:

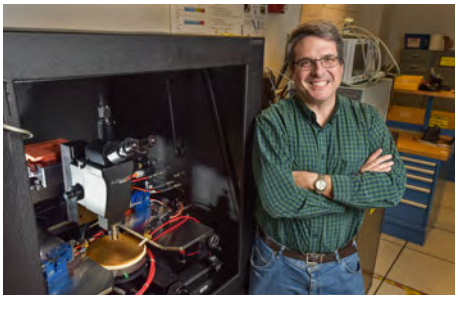
- Gold and aluminum wire bonding
- Applications include medical and U.S. military
- Excellent solderability
- Mitigation of black pad
- Gaining interest and acceptance in the market

There are many factors to consider when selecting a final surface finish and unfortunately, there is not a universal finish that works best for all applications. Understanding the advantages and disadvantages of each surface finish allows the designer to select the surface finish that best fits each application. Chemistry suppliers, fabricators and assemblers are all happy to offer suggestions based on their experience, take advantage of the resources available if you have questions or need assistance. **PCB**

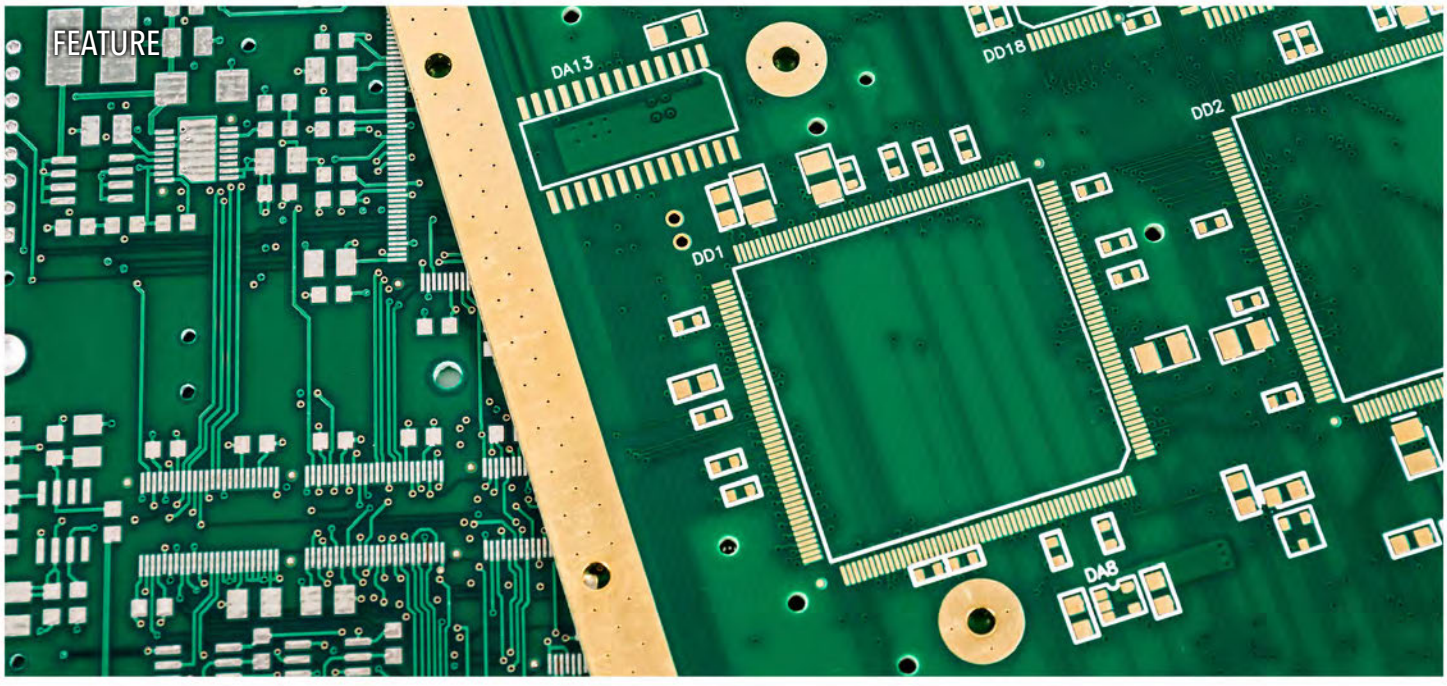
Tara Dunn is the president of Omni PCB. To read past columns or to contact her, click here.

Honey, I Shrunk the Circuit

Sandia National Laboratories researchers have shown it is possible to make transistors and diodes from advanced semiconductor materials that could perform much better than silicon, the workhorse of the modern electronics world.



The breakthrough work takes a step toward more compact and efficient power electronics, which in turn could improve everything from consumer electronics to electrical grids. Power electronics are vital for electrical systems because they transfer power from its source to the load, or user, by converting voltages, currents and frequencies. Sandia's research was published this summer in Applied Physics Letters and Electronics Letters and presented at conferences.



Study of Immersion Gold Processes Used for Both ENIG & ENEPIG

by Don Gudeczauskas, Albin Gruenwald and George Milad
UYEMURA INTERNATIONAL CORPORATION

Abstract

The use of electroless nickel/electroless palladium/immersion gold (ENEPIG) has been steadily increasing the past several years and benefits of the finish have now become well-known throughout the industry. The finish provides both reliable solder joints and wire bonds. In some Asian countries where mass production is performed at many facilities, dedicated production lines have been installed for plating of ENEPIG using an immersion gold optimized for ENEPIG but not for electroless nickel/immersion gold (ENIG). In the North American market, however, many PWB facilities are producing both ENIG and ENEPIG finishes from the same plating line due to lower overall production volumes and desire to use the same immersion gold for both finishes. Most facilities have neither the room for two separate immersion golds nor the desire to tie up capital with the cost of gold for two separate immersion gold tanks. The challenge for North American manufacturers has been in choosing the proper immersion gold chemistry which can suitably deposit gold for ENIG and ENEPIG while providing a robust finish for soldering, wire bonding, and electrical contact with both finishes.

This paper presents results of a comparative study on three types of immersion golds which could be used for both ENIG and ENEPIG deposits in the same production line: standard displacement immersion gold, high efficiency immersion gold which limits nickel dissolution, and a mixed reaction immersion gold which utilizes a mild reducing agent. Comparative results for solder wetting force, solder joint reliability and wire bonding will be presented for ENEPIG. Additionally, plated samples will be examined by SEM for evidence of nickel or palladium damage from the immersion gold plating operation.

Introduction

Recently, it is well-known that the electroless ENEPIG process has excellent solder joint reliability (SJR) and that it has the same wire bond reliability (WBR) compared to electroless Ni/Au with thicker Au (ENAG) process, even if

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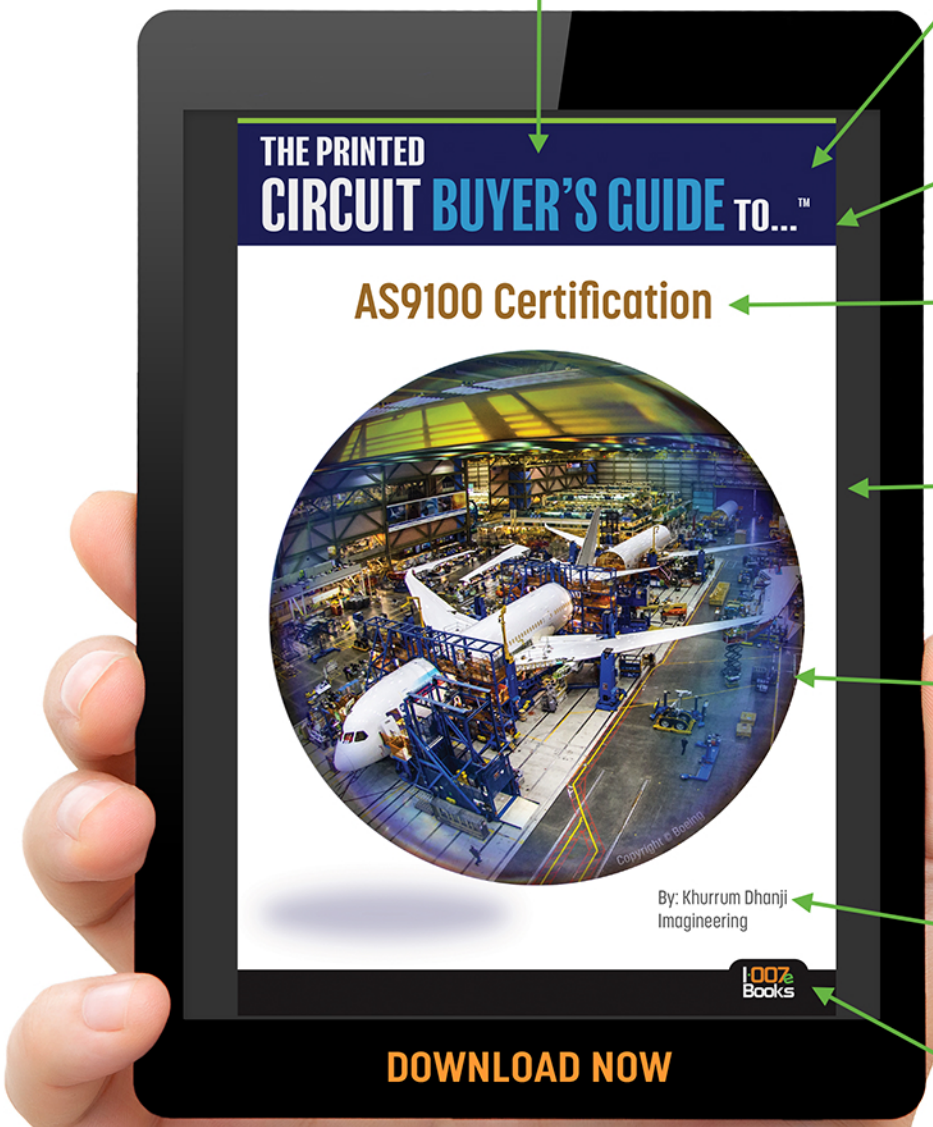

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the electroless Au thickness is between 0.1 to 0.2µm. Past studies have examined the performance of ENEPIG[1,2]. The current IPC ENEPIG specification (IPC-4554 Amendment 1) calls for gold thicknesses between 1.2 µin minimum at 4 sigma below the mean and 2.8 µin maximum, and some specific customer requirements call for even thicker gold. It has been found that thicker deposits of immersion gold might lead to nickel corrosion with ENEPIG if the dwell time in the immersion gold solution is too long.

The goal of this study was to examine the performance of ENEPIG using three different types of immersion gold: standard displacement immersion gold, high efficiency immersion gold, and reduction assisted immersion gold. The three types of immersion gold dissolve corresponding different amounts of nickel while the gold deposits as shown in Figure 1 using ENIG. The high efficiency immersion gold dissolves approximately half the amount of nickel from that of the standard displacement immersion gold while the reduction assisted gold dissolves approximately 60 percent of the nickel dissolved from the high efficiency immersion gold solution. Later studies will compare results for these immersion golds with ENIG only.

Examination methods in this study included solder wetting balance tests, gold sire bonding tests, cross section analysis for nickel corrosion examination and for intermetallic formation after solder testing.

Experimental and Results

The coupons used in this study consisted of a copper metallized and pattern plated (to 25 µm) test board which was subsequently coated with soldermask as shown in Figure 2. For wetting balance tests, standard wetting balance coupons with 36 mm wetting area were used. Specific BGA pads of 0.7 mm diameter connected to a ground plane were used for cross-section examination of nickel corrosion. Two BGA pads in each array were connected to a ground plane containing 0.375 in2 area giving a 629:1 area ratio which has been shown to help cause excess nickel corrosion in the past[3]. A wire bonding coupon was used for wire bonding tests. The test coupon is shown in Figure 1. This substrate was plated with ENEPIG by using plating chemicals commercially available from C. Uyemura & Co., Ltd. The ENEPIG plating process is shown in Table 1.

Process	Chemical	Temp	Time
Cleaner	Mild acid	40 deg. C	5 min.
Etching	Persulfate	25 deg. C	2 min.
Pre-Dipping	3% sulfuric acid	R.T.	1 min.
Activator	Palladium-type	30 deg. C	2 min.
Electroless Ni-P	Mid Ni-P	80 deg. C	25 min.
Electroless Pd-P	Pd-P (P=3%)	66 deg. C	6 - 9 min.
Immersion gold	Conventional Imm. Gold	85 deg. C	12 - 30 min.
Immersion gold	High Efficiency Imm. Gold	80 deg. C	15 - 45 min.
Immersion gold	Reduction assisted Imm. Gold	80 deg. C	5 - 13 min.

Table 1: ENEPIG plating process.

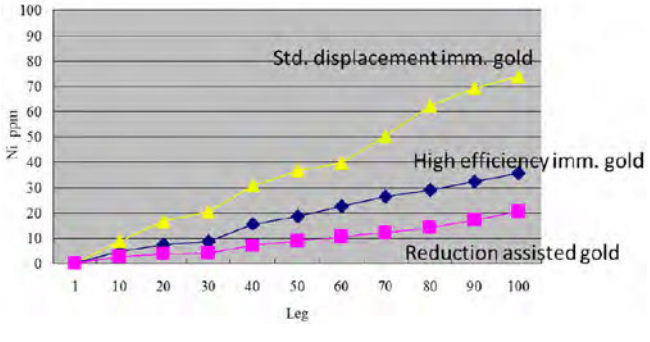

Figure 1: Depiction of nickel concentration in the immersion gold solutions after approximately 0.25 MTO comparing the three different types of gold plating processes used with ENIG.

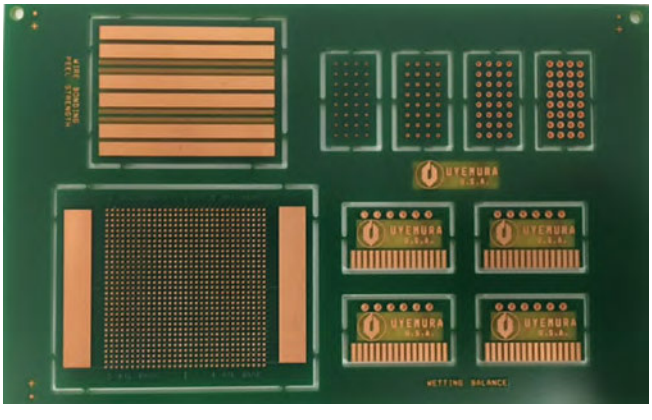

Figure 2: Test board showing wetting balance coupons, BGA array and wire bond array.

Thickness results were recorded using a Seiko SEA-5120 Element Monitor MX XRF. Gold deposit thicknesses were targeted for the lower and upper ranges of the IPC-4556 Amendment 1 specification. The cross-section images of BGA pads were observed using a JEOL JSM-6010LA SEM. Wetting balance coupons were tested in an as-plated condition and after 3x reflow at 255°C maximum temperature using a Heller 1088 reflow oven. Solder wetting balance testing was performed using a Metronelec Menisco ST 50 wetting balance with IPC test flux #1 using SAC305 solder at 255°C. Wire bond coupons were first baked at 175°C for 16 hours in a Fisher Isotemp 400 series oven. The wire bond coupons were subsequently argon plasma cleaned prior to wire bond tests. Wire bond testing was performed at Fast Semiconductor Packaging LLC (Anaheim, CA) using the equipment and conditions shown in Figure 3.

Measured thicknesses are shown in Table 2.

Solder Wetting Balance

Solder wetting balance test results are shown in Table 3.

Equipment	K&S 4524	
	Bond 1	Bond 2
Temp. Setting	150	150
Temp Actual	150	150
Power (mW)	2.54	3.01
Time (ms)	3.0	3.0
Force (g)	3.0	3.5
wire size	1 mil gold	

Figure 3: Wire bond conditions.

Sample	Sample Description	Avg. Au thk. u"	Avg. Pd thk. u"	Avg. Ni thk. u"
1	Red. assisted immersion gold	2.94	9.39	217
2	Red. assisted immersion gold	1.59	7.05	224
3	Std. displacement imm. gold	2.79	7.56	224
4	Std. displacement imm. gold	1.49	7.77	206
5	High efficiency imm. gold	2.98	4.82	204
6	High efficiency imm. gold	1.27	6.35	187

Table 2: Deposit thicknesses in microinches.

Solder wetting curves were compared to the standard curves shown in Figure 4 while a typical curve from the testing (Sample 4, standard immersion gold at 1.49 µin) is shown in Figure 5. Solder wetting times and final wetting forces were excellent for samples tested with good wetting observed as described in the depiction figure. Interestingly, the wetting times decreased in all cases after the 3x reflow exposure. Final wetting forces were all above 0.20 mN/mm. The reduction assisted immersion gold samples showed some of the lowest wetting times while the standard immersion gold samples exhibited the longer wetting times.

Wire Bond Testing

Previous work performed by IPC committee members in the writing of IPC-4556 involved a large round robin test program whereby several

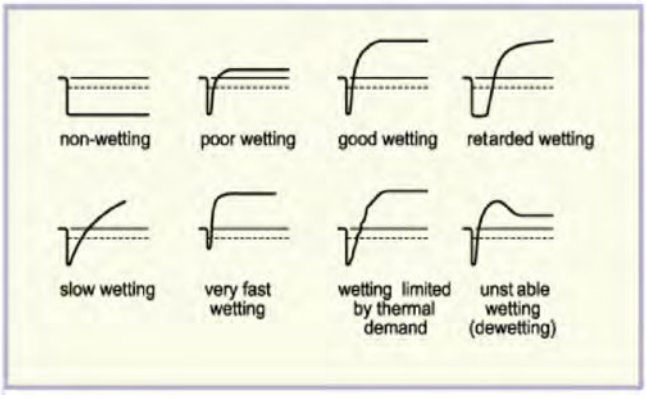

Figure 4: Wetting balance curve depictions.

Sample	Condition	Gold thk. u"	Solder wetting time, sec.	Final wetting Force mN/mm
1	High Eff. Gold as plated	2.94	0.31	0.25
1	High Eff. Gold - 3 reflows	2.94	0.20	0.25
2	High Eff. Gold as plated	1.59	0.27	0.23
2	High Eff. Gold - 3 reflows	1.59	0.26	0.23
3	Std. Displ. as plated	2.79	0.64	0.25
3	Std. Displ. - 3 reflows	2.79	0.42	0.25
4	Std. Displ. as plated	1.49	0.38	0.25
4	Std. Displ. - 3 reflows	1.49	0.36	0.23
5	High Eff. as plated	2.98	0.59	0.24
5	High Eff. - 3 reflows	2.98	0.25	0.26
6	High Eff. as plated	1.27	0.40	0.22
6	High Eff. - 3 reflows	1.27	0.32	0.22

Table 3: Solder wetting balance test results.

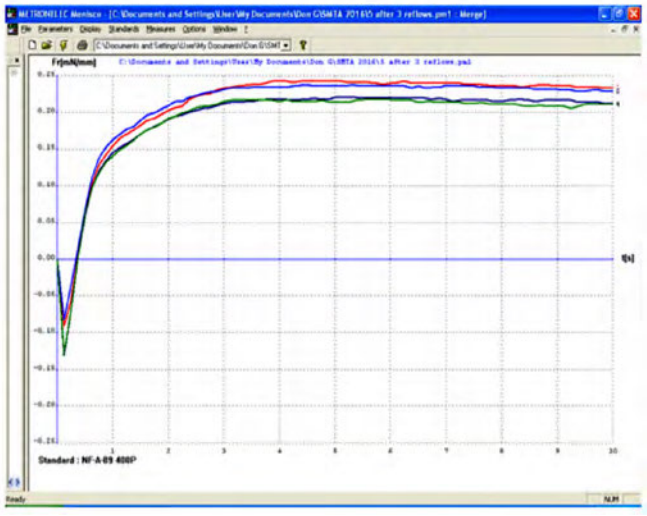

Figure 5: Wetting balance test results, sample 4 after three reflows.

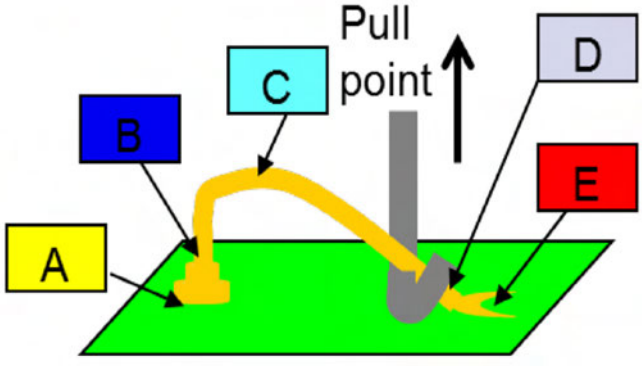

Figure 6: Wire break modes.

ENEPIG deposits of varying gold thicknesses from various suppliers were wire bond tested. It is believed the samples for the IPC study were not baked to simulate die attach and this current study attempted to determine if any effects of baking at 175°C for 16 hours were seen on gold wire bond results when using different types of immersion gold. A depiction of the typical wire break modes is shown in Figure 6. Ideally, wire breaks at locations B, C, and D are preferred. Wire breaks at position A and E would indicate a poor bond between wire and substrate. Results for the current study are shown in Table 4 and Figure 7, respectively. Despite heat aging, all results appeared acceptable, well above the 3-gram pull strength minimum. The standard displacement immersion gold sample with

Sample	Mean	Min	Max	Std. dev.
1-Red. Assisted thick gold	10.3	9.4	11.2	0.48
2- Red. Assisted thin gold	9.9	7.9	10.8	0.78
3-Std. Disp. thick gold	10.2	7.2	11.7	1.07
4-Std. Disp. thin gold	10.3	9.5	11	0.47
5-High eff. thick gold	11.0	9.4	12	0.58
6-High eff. thin gold	10.7	9.9	11.9	0.44

Table 4: Wire bond test result data for the six samples.

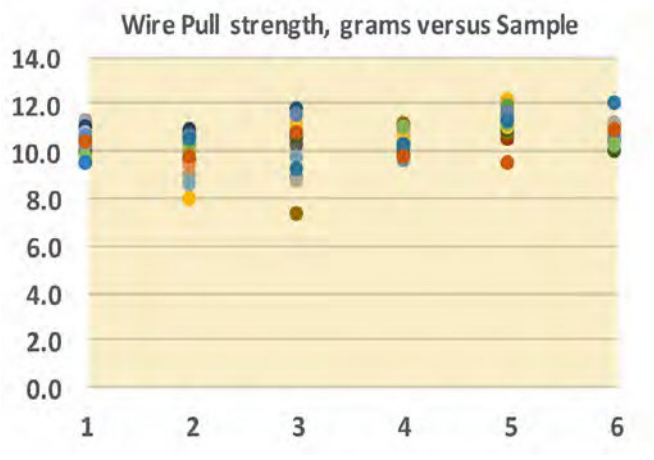

Figure 7: Wire bond data, 20 points per sample.

thick deposit showed lower minimum wire pull strength and higher variation in values when compared to the other samples.

Wire breaks in all tests were in the wire either just above the first bond or just above the second bond (modes B or D). No failures were seen at the wire/substrate interface (modes A or E).

SEM Examination of the Deposits

Figure 8 shows the ENEPIG deposit top-down. In general, the palladium and gold uniformly coat the electroless nickel.

Experience has shown that attempts at obtaining very thick gold with ENEPIG using a standard displacement immersion gold results in some damage in the electroless nickel layer below the electroless palladium deposit. Of the three deposited metals the electroless nickel is the least noble. Any access the immersion gold may find to the nickel will result in nickel dissolution into the immersion gold solution. Excess dwell time in the immersion gold solu-

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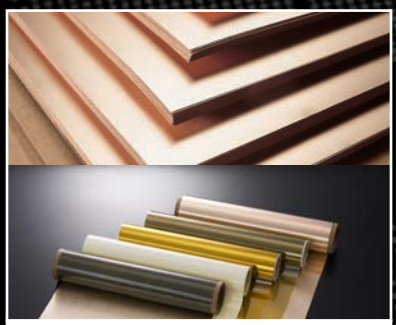

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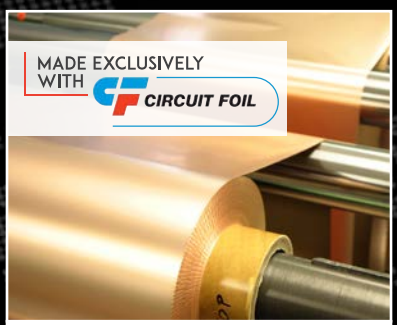

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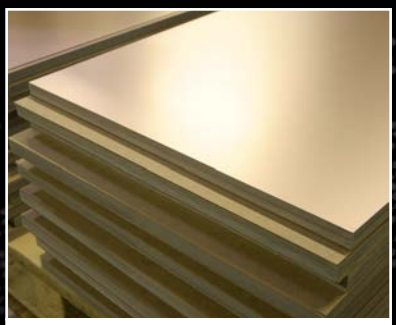

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tion may dissolve enough palladium which may allow a pathway for the gold to attack the nickel deposit. Lateral attack of the nickel underneath the palladium has been seen in some cases where the immersion gold layer has become very thick. The resultant lateral nickel attack in extreme cases may cause delamination between nickel and palladium, especially after wire bonding. The delamination results in wire lifting and connection failure. Figure 9 shows the lateral corrosion from an ENEPIG deposit which contained 5.1 µin of gold and 3.4 µin of palladium. The gold used in this instance was the standard displacement process.

SEM cross section examination was performed for the three samples with thick gold to detect any deposit damage from the immersion gold reaction.

Figures 10 and 11 show cross-section images from the different deposit at the BGA pad edge and pad center. The BGA pad was connected to the ground plane. In these three examples, the thicker gold deposit was examined for each of the three different types of immersion gold solutions. The BGA pad edges showed no nickel corrosion. The BGA pad center showed no corrosion for the reduction-assisted immersion gold while small corrosion spikes were seen with both the standard immersion gold and high efficiency immersion gold. The small corrosion spikes seen are not believed to be of consequence based on the wetting balance and wire bond data collected in this paper but can be considered a process indicator. No corrosion spikes were seen from any of the samples with thinner gold deposits.

While wetting balance testing showed excellent wetting time and wetting force, cross sections were performed on the solder samples from the three thick immersion gold deposits to examine the intermetallic formed. In all cases a uniform, continuous intermetallic layer was observed as shown in Figure 12.

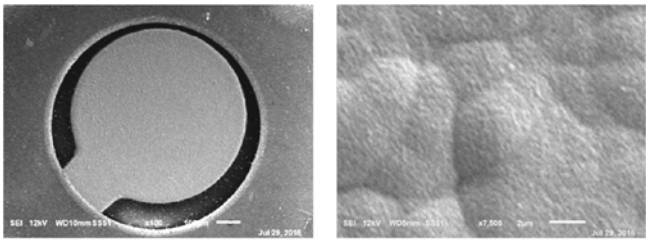

Figure 8: SEM images top-down of the ENEPIG deposit at 100x, 7500x.

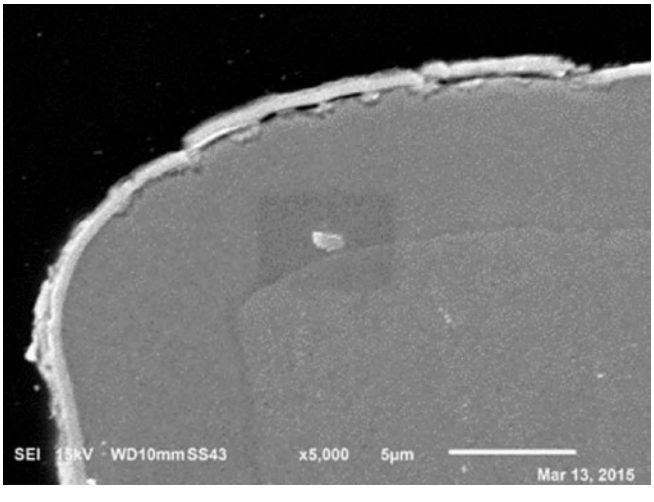

Figure 9: Example of ENEPIG corrosion under the gold and palladium deposit at 5000x.

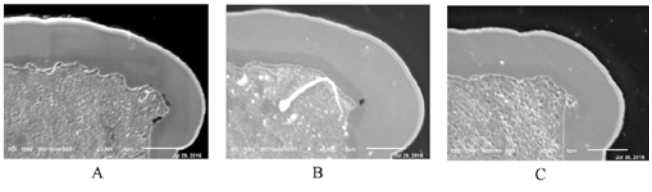

Figure 10: Cross-section on BGA pad edge at 5000x.
A - Reduction assisted thick immersion gold
B - Standard immersion thick immersion gold
C - High-efficiency thick immersion gold

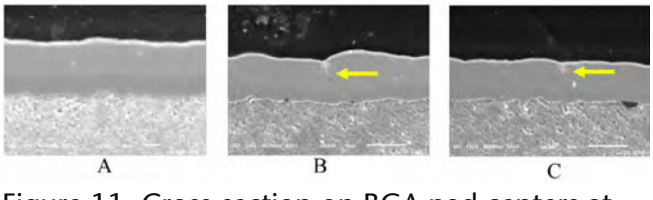

Figure 11: Cross-section on BGA pad centers at 5000x.
A - Reduction assisted thick immersion gold
B - Standard displacement thick immersion gold
C - High-efficiency thick immersion gold

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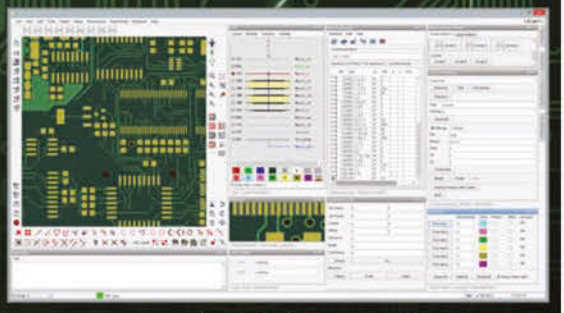

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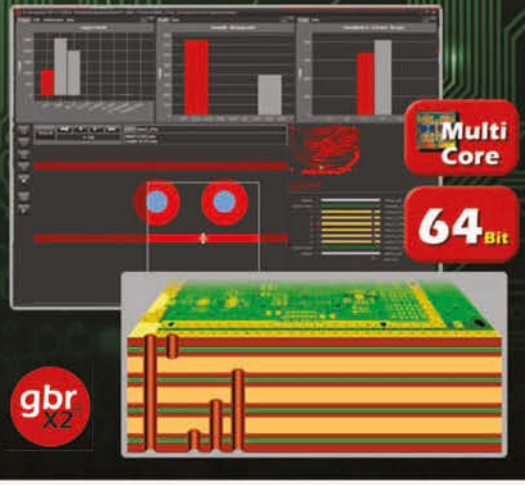

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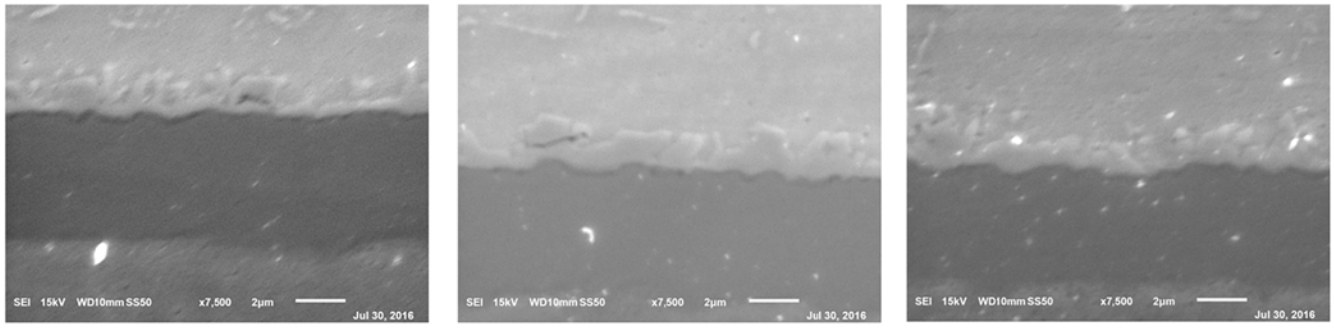

Figure 12: Cross-section examination of the intermetallic formed after wetting balance test, 7500x.
A - Reduction assisted thick immersion gold
B - Standard immersion thick immersion gold
C - High-efficiency thick immersion gold

Conclusions

Solder wetting balance tests showed that the reduction assisted immersion gold process yielded the fastest wetting times while the standard displacement immersion gold showed slightly lower wetting times. All final wetting forces were excellent regardless of heat exposure from 3x reflows.

Wire bond testing showed very good results from all six samples with higher standard deviation observed for the standard displacement immersion gold with thick deposit. Average wire bond values were well above the 3-gram minimum with average readings all above 9 grams.

Cross section analysis of the plated samples showed some small corrosion spikes in the standard displacement and high efficiency immersion gold with no such corrosion spikes seen in the reduction assisted gold deposit. It is thought that the corrosion spikes, if present in higher amounts, would affect solder wetting and wire bond results and could be used a process check for production considerations.

Future data presentations will include the performance of the three immersion gold types with gold thicknesses at the high end of the new IPC ENIG specification. Solder testing and cross-section analysis will be performed. **PCB**

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Don Gudeczauskas is vice president, Uyemura's technical center in Southington, CT USA.

Albin Gruenwald is technical service representative, Uyemura's technical center in Southington, CT USA.

George Milad is national accounts manager for Technology, Uyemura's technical center in Southington, CT USA.

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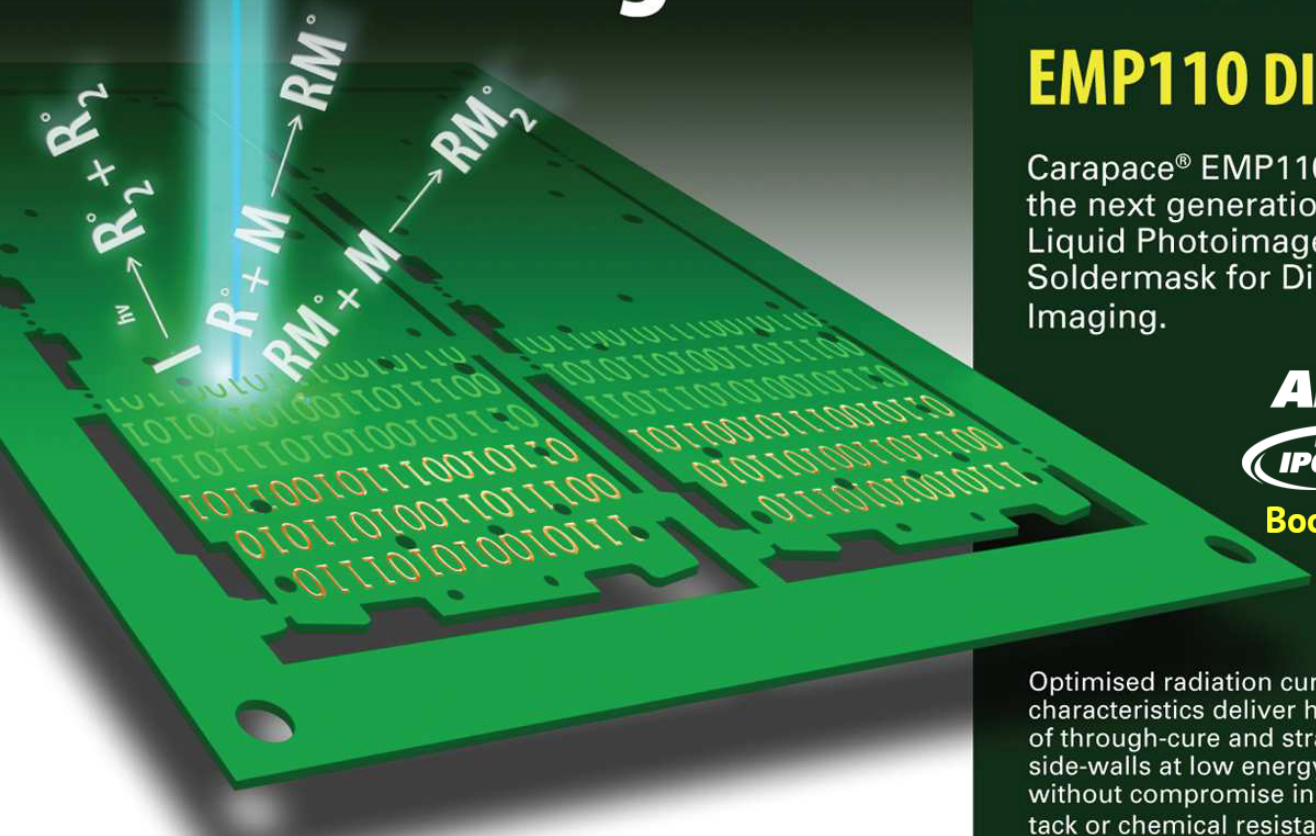

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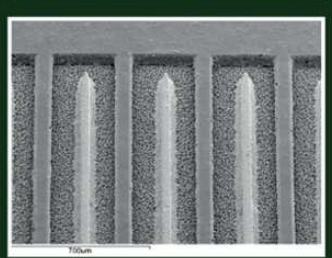

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A Scientific Response to Mr. Laminate Tells All

We read with interest Doug Sober's recent Mr. Laminate Tells All column, "The Certification of IPC-4101D Polyimide Base Materials: Buyer Beware." The article raises interesting questions about the IPC 4101 classification system, primarily, how is a pure resin defined?

New Tools Mean More Designer Control for High-Speed PCBs

In the last hour of the electronica exhibition in Munich, Pete Starkey got the opportunity to sit down with Martyn Gaudion, managing director of Polar Instruments. They discussed the changing state of PCB design, and how the newest software tools allow PCB designers and engineers to have more control when designing high-speed PCBs.

CIPSA Circuits Invests in Orbotech Nuvogo 780 and Additional Fusion 22

Orbotech Ltd. has announced that CIPSA Circuits, a European PCB manufacturer and long-time customer and technology partner of Orbotech, has invested in a Nuvogo 780 Direct Imaging (DI) solution, plus an additional Fusion 22 AOI System to further increase overall productivity.

Doosan Electro-Materials BG Signs Distribution Agreement with Arlon EMD

Doosan Electro-Materials BG and Arlon EMD have reached an agreement whereby Arlon EMD has distribution and sales rights in North America for Doosan's DS600 flexible copper clad laminates, as well as Doosan's high-Tg FR-4 and halogen-free laminate and prepreg product lines.

Rogers on the Booming Wireless Infrastructure Market

With the advent of 5G and next generation antennas, the already booming wireless infrastructure market is slated for continued growth through 2021, and as the primary material supplier for this sector, Rogers Corp. must continue to meet the technological demands of the Verizons and AT&Ts of world.

Let's Talk Testing: Are You Getting What You've Asked for?

A lot of things are taken for granted nowadays. Even in our everyday lives, we order things, but are we always getting exactly what we've ordered? What we've paid for? Maybe…hopefully…but maybe not. In the testing world, we call this double-checking "supplier surveillance."

Ladle on Manufacturing: Making Suppliers Work for You

Every company has its own way of doing things. For some, the engineering team develops a detailed specification for the equipment they would like to purchase and this is put out to multiple suppliers for tender, along with full documentation for the commercial terms that will apply to the purchase.

Rogers Launches Laminates for Automotive Radar Sensor Applications

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Plating and Surface Finish: The Challenges to Electrical Test

by Todd Kolmodin
GARDIEN SERVICES USA

Plating

Plating and surface finish applications are not without their own set of challenges but these manufacturing processes also affect the electrical test theatre. Microvias, high-aspect ratio plate quality, and surface finish all have their own challenges in ET.

Let's face it, the largest challenges regarding plating involve the detection of voids. Whatever type they may be is insignificant in ET as the detection is foremost the main focus. Unfortunately, with standard ET detection processes many partial voids go undetected. This also can be said for a barrel that is voided outside of the electrical test signature.

The undetected partial void is usually the "taper plate" or "narrowing" void. These defects usually have adequate plating near the annular rings towards the outer layers but then narrow as they reach the center of the barrel. Figure 1 shows a typical taper plate defect.

This type of defect usually will not fail the standard ET continuity test. There is sufficient plating in the barrel to pass the electrical signal within the continuity threshold (usually 10–20 ohms depending on performance class). For the capture of anomalies such as this it is recommended that a 4-wire Kelvin sampling test be performed. This type of continuity test is designed to capture minute fluctuations in barrel resistivity. These measurements are in the milliohm (mO) range.

Microvias pose another challenge to ET. Usually these are buried (manufactured in the sub-part level) and have no direct landing pad accessible from the outer layer. In Figure 2, we

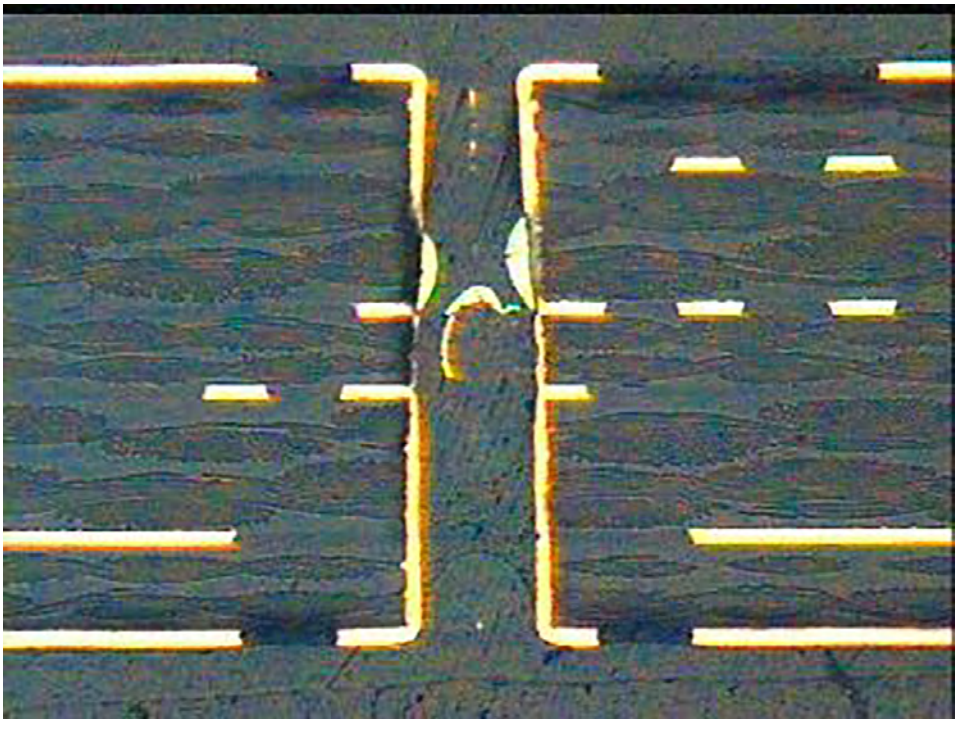

Figure 1: Taper plate defect.

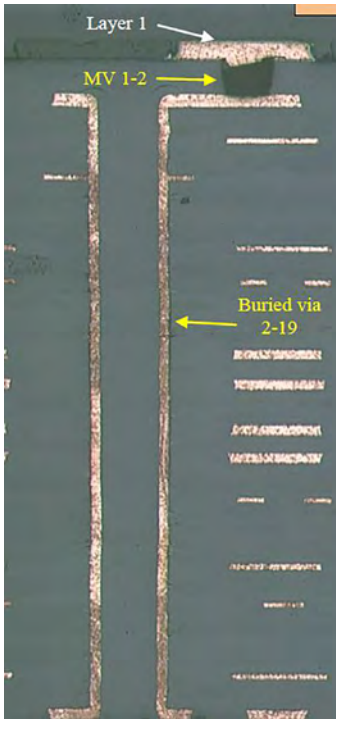

Figure 2: Microvia void.

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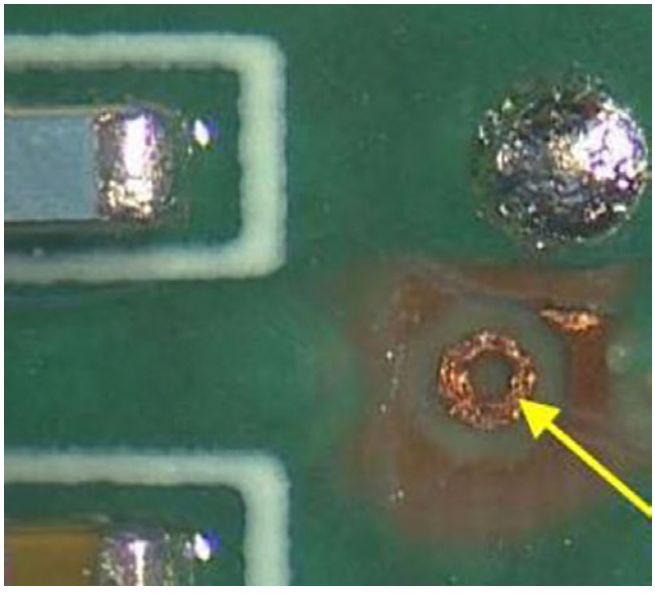

Figure 3: Microvia barrel (outer layer).

see an example of a buried microvia that has voided. In this example, we see that there is only an annular ring termination on layer 1. This is shown in Figure 3. In this case the electrical signature is passing through the sub-part (layers 2–19). In many cases this type of net has final terminations of the electrical net in different locations on either layer 1 or 20. This specific void may not be detected, as the landing pad on layer 1 in the example may be deemed a mid-point and thus be optimized out. This defect would be captured during functional test as that point in Figure 3 may be used as a signature validation or In-Circuit Test Point.

Surface Finish

With today's final surface finishes on modern PCBs, the challenge for ET is to make sure defects are detected without scrapping the board in the process. While it has always been a ballet to successfully test the circuit board without damaging it, the more modern finishes make it much more difficult. Back in the day it was just plated holes and HASL (hot air solder leveling). This is extremely robust and in the unfortunate event of significant test marks it could be run back down the line and reflowed. Today that is far from the norm.

Today the most challenging finish for ET to successfully test is immersion silver. This delicate finish carries the high solderability characteristic but is usually applied very thin due to cost. Electrical test probes from either fixture testers or flying probes can unfortunately leave unfavorable witness marks. In the worst case, they can break through the finish exposing the copper landing pad below. In some cases, although rare due to via capping, these boards can be reworked. In most cases, if significant witness marks are made, the board will be scrapped.

ENIG and other gold finishes take up the remainder of the surface challenges. The same hazard exists here with damage to the finish.

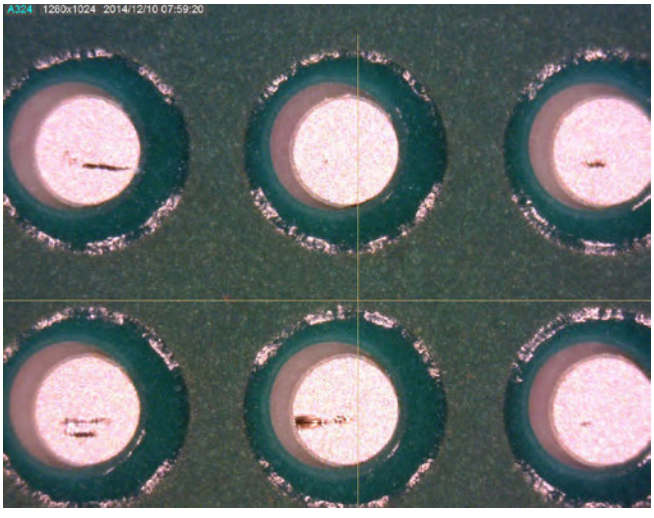

Figure 4: Witness mark 1.

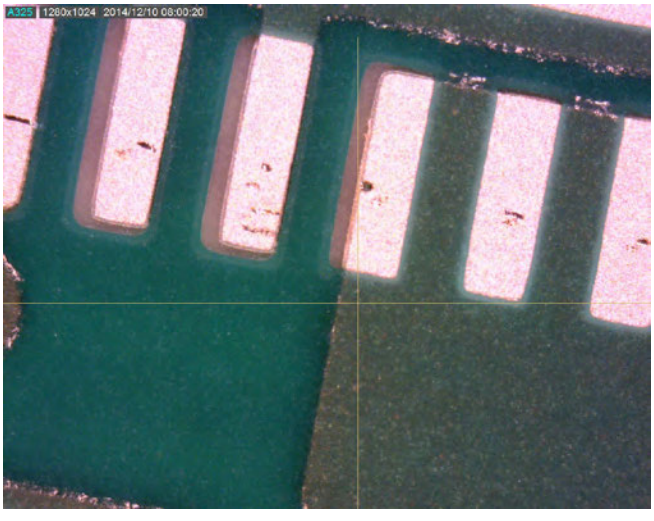

Figure 5: Witness mark 2.

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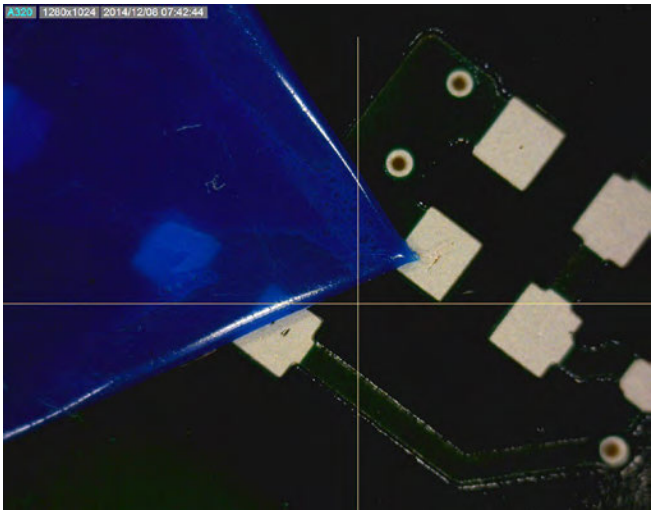

Figure 6: Witness mark 3.

Although in some cases it also can be reworked, customer/industry requirements may disallow the rework. Again, in this case the board would be scrapped. Figures 4–6 are examples of witness mark damage.

Combating excessive witness marks can be a challenge. With fixture testers, there are multiple variables that can contribute to damaging marks. A malfunctioning fixture is the most significant contributor. In these cases, a test probe can stick or become jammed which will not allow it to travel freely when compressed. The probe locks in place and drives a damaging signature into the targeted landing pad. Second, the actual pressure used by the machine itself can contribute to the excessive marks. Therefore, it is imperative that proper set-up procedures be used when fixture testing. The time it takes to properly set up the fixture test greatly outweighs the cost and time lost scrapping an expensive board—not to mention the unhappy customer who now has a delayed delivery.

Flying probes, although not known to contribute extensively to board damage, do have their caveat as well. Improper setup or adjustments with these machines can also cause damage. The main attributes are velocity and compression. Most significant is the Z-axis velocity. When the Z-axis travels to the board surface, its speed is important as it will travel at full velocity until the board surface is detected. If this velocity is too high the inertia of the movement may be too significant for the tensile strength of the surface finish and may damage the surface upon impact. Further, once contact is made the variable of compression also may contribute. This is the further distance the probe will move towards the landing pad once contact has been initiated. Proper adjustments to these parameters are crucial to provide the desired results without leaving damaging witness marks.

As illustrated here, even mechanical and chemical processes pose challenges to ET. It's not just the cut and dried check for opens and shorts. Care and different diagnostic measures must be used to successfully validate the product without leaving an "ET was here" type of damaging mark on the board.

HAPPY NEW YEAR! **PCB**

Todd Kolmodin is the vice president of quality for Gardien Services USA, and an expert in electrical test and reliability issues. To read past columns, or to contact Kolmodin, click here.

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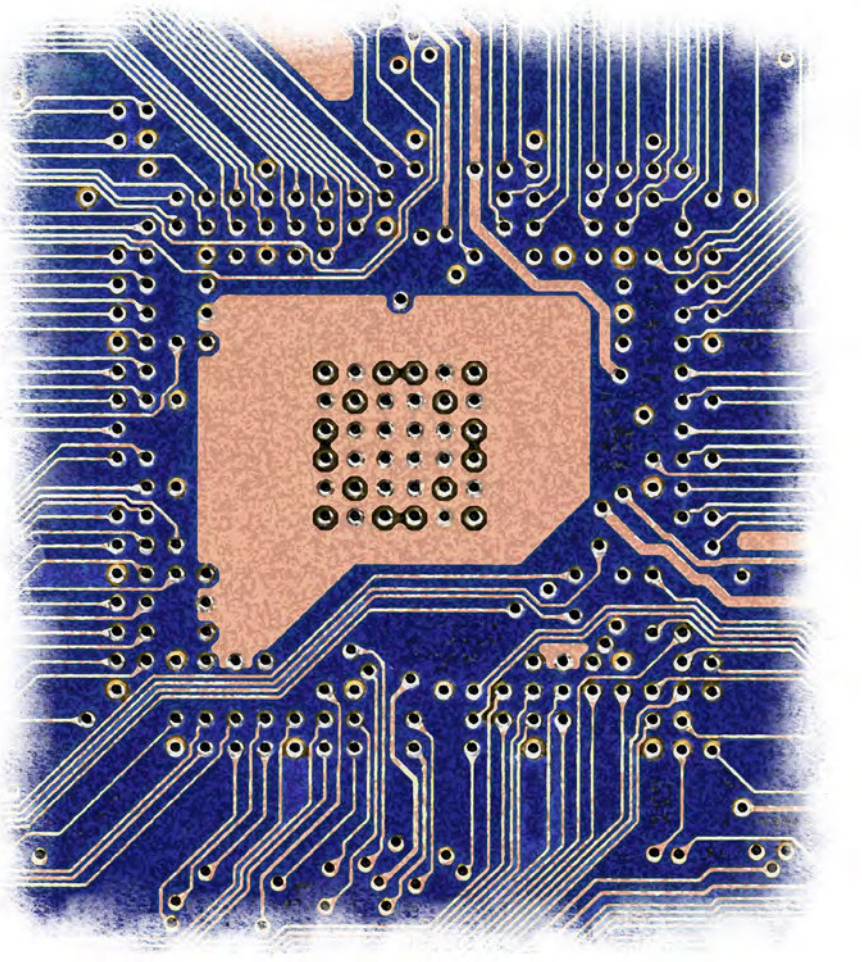

by Michael Carano
RBP CHEMICAL TECHNOLOGY

Introduction

Electroplating a printed circuit board is by no means a trivial task. Higher layer counts, smaller-diameter vias (through-hole and blind) as well as higher-performance material sets contribute to the greater degree of difficulty with today's technology. So, process engineers pay close attention to the "softer" issues such as cathode current density, solution chemistry (copper sulfate and sulfuric acid concentration) and addition agent control (well, sometime!).

The concern here is that acid copper pattern plating of a printed circuit board has many more critical aspects that must be diligently controlled for optimum performance. These include solution agitation and filtration, anode length and placement, current distribution effects, reducing electrical resistance in the plating cell, photoresist development and controlled organic contamination in the plating solutions. These are the subjects of this article.

Solution Agitation

For uniform surface plating distribution, a homogeneous mixing of the electrolyte is necessary to avoid overplating the surface while the through-hole or blind via is being plated from the bottom up. The engineer should adjust flow rates so as to not create an excessively turbulent solution movement.

Solution agitation of the copper plating electrolyte maybe accomplished with air agitation, eductors, solution impingement and/or cathode bar movement. The main purposes of agitation have been stated many times and include:

- Elimination of solution stagnation and dispersal of reaction products
- Increase of deposition rates by mass transfer enhancement
- Dissipation of heat at electrode/solution interfaces

While the use of air agitation (supplied by a blower) was the standard method for agitating

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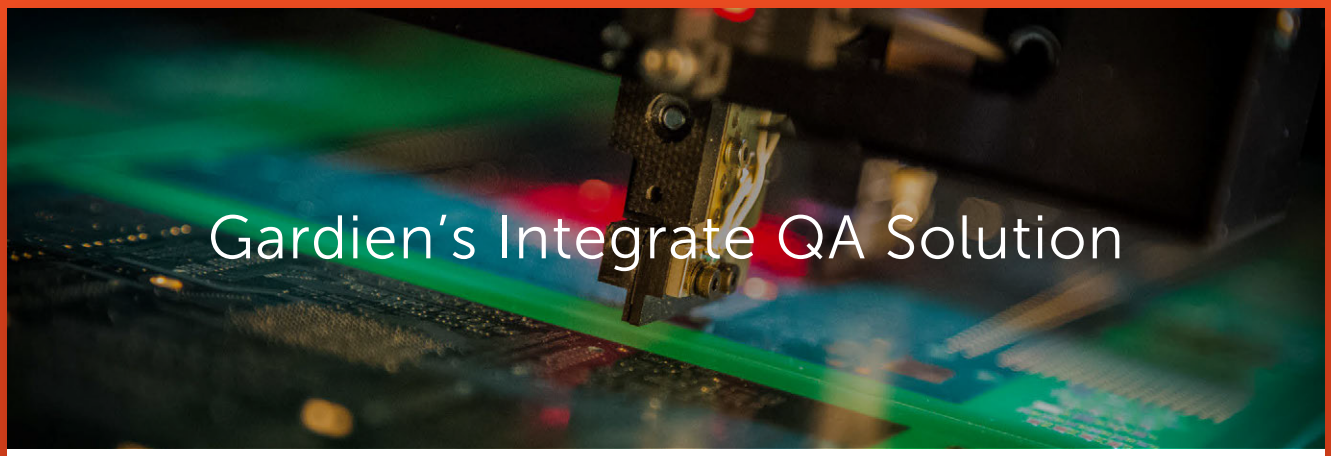

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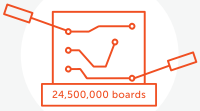

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acid copper solutions for many years, as circuit board designs have evolved into higher density patterns and smaller diameter vias, air agitation has reached its limitations. Air suffers from three main disadvantages: It has a chemical oxidative action towards solution constituents; it is electrically resistive when present as a cloud or foam of bubbles; and the general plating rate enhancement is modest despite several possible parameters for adjustment. The least appreciated characteristic is the resistivity which can lead to an increase in electroplating voltage power of 25–30% and is therefore a significant electrical cost factor. It also generates environmental pollution through its dispersion of air bubbles. In addition, these tiny bubbles can lodge into the through-holes and blind vias, leading to a reduction in plating thickness or voids.

One ideal solution (pun intended) to the need for solution agitation is to employ eductors and eliminate the use of air agitation completely. Eductor agitation is based on the Venturi principle, whereby one volume is pumped and up to four volumes are drawn in by the pressure drop, making it a highly efficient jetting system. When the system is fully submerged, no air is entrained. Such eductors are marketed by several manufacturers. Eductor agitation overcomes several of the disadvantages associated with air agitation. Air bubbles and misting are eliminated. In addition, eductor agitation provides a more uniform mixing of the plating solution. This minimizes potential dead spots in the cell where the air agitation is lacking. It is well known that educators provide more uniform agitation, better known as laminar flow. In contrast, air agitation provides a turbulent flow, and may only promote mixing of the solution. For quality plating results, it is preferable to have interface agitation. That is, one interface agitation is directed more at the cathode diffusion layer. This helps to reduce the diffusion layer thickness thus permitting the efficient delivery of additives and ions to the cathode surface[1].

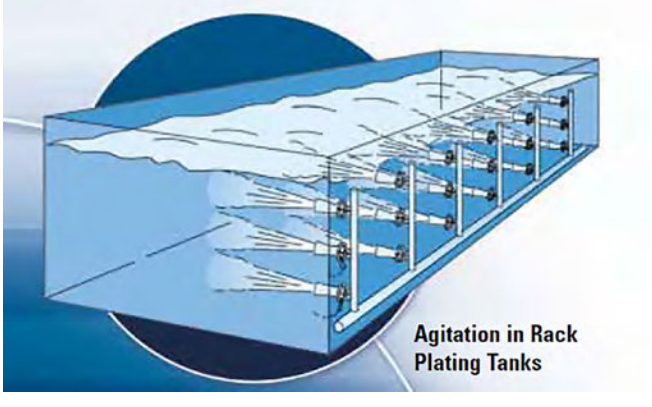

Figure 1: Schematic of plating cell outfitted with eductors. (Source: Spray Systems Company's "A Guide to Optimizing in-Tank Agitation")

Figure 2: Actual photo of plating cell outfitted with bottom-up eductors. (Source: RBP Chemical Technology)

Figure 1 shows a schematic of a plating cell outfitted with eductors. This shows the eductors pointing towards the surface to be plated. However, there are additional options available with respect to educator designs. In a second case, the eductors are pointed up from the bottom of the plating cell (Figure 2).

Both designs have extensive research and field experience that shows that with either design, surface distribution of electrolytic copper plating is greatly improved.

Monitoring and Controlling Carbon Content

Engineers fully understand the need for organic addition agents in the plating solution. Whether it be for acid copper or etch-resistant tin, organic chemicals are required to enhance the physical properties of the deposit, effect leveling and help minimize overplating in high current density areas. However, these organic materials, even when controlled under the most diligent protocols, do form break-down by-products over time. Essentially these break-down products accumulate in the plating solution. There is also the potential for additional organic materials entering the plating electrolyte from photoresist leachants and pre-plate cleaner drag-in. Negative effects of the accumulated organics include rough copper-plated deposits, reduced ductility of the copper, and concerns over long-term resistance to thermal and mechanical excursions that the printed circuit device functions reliably in service over long periods of time. Higher-than-normal levels of organic break-down products will also lead to cosmetic issues.

One tool that is used to monitor organic content in plating solutions is TOC—total organic carbon analysis. Since a TOC analyzer can be used to manage the concentrations of organic material in plating solution, it can be utilized for quality management of electroplated products and the overall health of the plating solution. While it is not expected that every printed circuit board manufacturer would have its own TOC unit in-house, most chemical suppliers provide this service. What is critical for the manufacturer is to monitor the TOC content over a time interval and equate these values with end-product performance. It should be noted that not all acid copper plating additives are created equal. Therefore, one should not try to draw conclusions on organic content with values of TOC from two different suppliers.

Anode Length and Placement

The placement of the anodes in a plating cell is critical with respect to plating distribution. One should look at the anode as where the lines of flux or current is distributed into the cell and onto the cathode (the circuit board). Electricity follows the path of least resistance. That is precisely why it is often difficult to achieve optimum surface plating distribution across a printed circuit board panel. Typically, those isolated circuit features and the top of the circuit board attracts more current than other areas. Thus, these areas tend to plate to higher thicknesses than the lower current areas. The engineer's job is to find ways to reduce these current variations. Certainly, chemical and other operational parameters can be adjusted to aid distribution. However, one should not overlook the anode placement and length. As a rule of thumb, distribution and throwing power are improved if the cell design allows for a longer distance between the anode and cathode (ideally, 10–12 inches is recommended). In addition, anode length should be 4–6 inches above the lowest level of the circuit board in the plating cell.

Finally, there are additional techniques that can be used to enhance plating uniformity. One such method is the use of non-conductive shields. These shields are strategically placed in the cell to redirect current away from the perceived higher-current density areas of the circuit board. The shields can always be removed.

Electrical Resistance in the Plating Cell

While most engineers work diligently to control the chemical aspects of the electroplating process to insure optimum throwing power (surface-to-hole ratio), they often overlook other critical parameters of the process. These include resistance through the cabling leading from the power supply to the plating cell, plating rack current-carrying capacity, and additional resistances within the cell. As it stands, electroplating is governed by Ohm's law. The greater the resistances within the plating cell, the more difficult it will be to achieve uniform plating thickness distribution. If the author can use this analogy:

- Current flow (analogy) is likened to a flow of water through a hose
- Flow of water:
  – GPM = pressure divided by resistance
- In other words, the longer the hose or the smaller the diameter of the hose opening, the less water you will get

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The same can then be said about current flow to the plating cell. Current is dependent on resistance and voltage. If resistances increase, the flow of current to the plating cell is reduced.

Based on this analogy, the author prefers to design the cell with minimal distance of the cables from the power supply to the plating cell. In addition, the current-carrying capacity of the cables is critical to achieve uniform current flow and to minimize current loss. If the cabling from the power supply (rectifier) to the cell feels hot to the touch, this is an indication that there is a loss of current reaching the cathode (circuit board to be electroplated). It is wise to replace these cables on a regular basis to insure quality plating.

Finally, do not overlook the quality and material of construction of the plating racks. While stainless steel is a rugged material for rack construction, it does not have the conductivity of copper. A well-designed copper plating rack will deliver 88–92% of the current supplied by the rectifier to the cathode. Conversely, stainless steel is only 50–55% effective!

Filtration

The need for filtration cannot be emphasized enough, especially when plating in through-holes and blind vias. Any void in the plating in the hole caused by small pieces of contaminant causes a reduction in the area available to carry the electric current. Rejects would also be caused when insoluble debris is co-deposited on the surface or in the hole.

Flow rates are the only means of carrying solids to a filter or bringing fresh solution into contact with the particulate matter. The rate of flow is referred to as the turnover—total gallons pumped per hour in relation to the size of the tank (for example, 200 gal/hr on a 100-gallon tank equals two turnovers per hour). Dirt holding capacity is essential and can be attained with throw-away paper, or cartridges of different porosities, or filter surfaces coated with filter aid. Porosities of 100 microns down to less than one micron are typical. In practice, the average plating solution is turned over once per hour. The recommended flow rates should provide at least two complete tank volume turnovers per hour. However, to achieve the ultimate in clarity, turnovers of up to ten times per hour may be necessary. Keep in mind that the initial flow rate is not the average flow rate. In other words, if one started at 1000 gal/hr, and cleaned or replaced the filter when the flow was reduced to 200 gal/hr, the actual average flow would probably be about 600 gal/hr, depending upon the type of filter media used.

Developing

Developing photoresist is one of the simpler chemical processes in the making of a PCB, yet one of the more crucial, as it defines what the circuitry will look like when the PCB is finished. Because developing is apparently so simple, it is easy to overlook its significance to the production of high quality PCBs, and to overlook the details necessary to produce high quality developing. Incomplete developing, over-developing, positive or negative foot, etc. will plague even the most experienced plating engineer.

The standard developer today is a 1% solution of either sodium carbonate monohydrate (Na-2CO3.H2O), or potassium carbonate (K2CO3). There is not much to choose from between the two, although the use of potassium carbonate has been reported to give slightly better quality developing, and have a wider process window. Potassium carbonate can be purchased in concentrated liquid form, allowing convenient feed and bleed application, without large feed tanks.

In the days when 6-mil lines and spaces were considered fine lines, using developer solutions to the point where the developing slowed dramatically and then dumping them, was an acceptable scenario. However, this modus operandi is no longer effective. Today's higher circuit density creates a washboard effect, making it more challenging to deliver sufficient amounts of developer solution to the circuit board. Therefore, manufacturers insure that tightly pH-controlled developing processes are in use. While understanding that feed and bleed systems allowing for steady pH control are critical for optimum performance, there are several other aspects of developing that are often overlooked as to their importance. One such aspect is the spray nozzles used in the developing and rinsing chambers.

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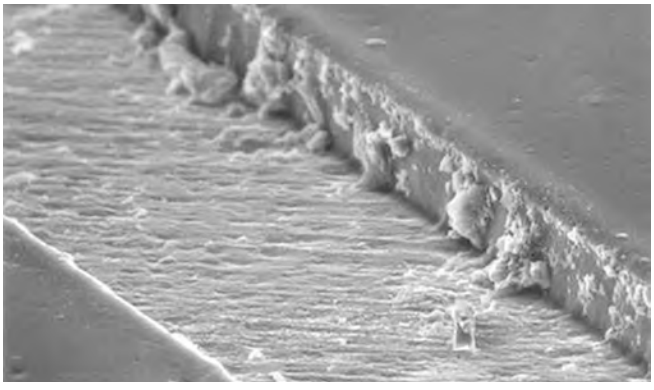

Figure 3: Developer/resist residues remaining on sidewall and surface. (Source: IPC-9121 Process Effects Handbook)

Figure 4: Plugged nozzles in developer chamber. Note uneven developing patterns on the test panel. (Source: RBP Chemical Technology)

modules for PCB processing. The advantage of the cone nozzle is its high liquid volume delivery. However, fan nozzles provide higher impact (impingement). This is highly effective especially when developing finer lines and spaces. The author wrote in a previous column[2] that high impingement fan type nozzles work very well in the aqueous development for the removal of resist and developing solution residues from the copper surface and the exposed sidewalls of the resist. A clean removal of all residues from the copper surfaces and sidewalls is required for defect-free plating and to insure the circuit trace is as uniform as possible. In addition, rinsing after developing with a minimum of 70°F water temperature is most effective in removing these alkaline residues. Figure 3 shows incomplete development due to either low pH, inadequate rinsing or insufficient developing/rinsing spray pressures.

And finally, proper maintenance of the spray nozzles in both the developing and rinsing chambers is necessary to ensure nozzles remain clean and free of resist residues. An example of what plugged nozzles will lead to is shown in Figure 4.

At this point, the operator needs to suspend the operation and either replace the nozzles or at the very least clean the machine and nozzles.

Summary

To deliver a high-reliability printed circuit board, engineers must not overlook or take for granted aspects of the process that have great impact on the end result. Certainly, most operators and engineers worry about controlling the wet chemistry of the plating process and imaging fundamentals such as exposure. Yet, they are often surprised and disappointed that the quality of the finished product is not meeting stringent quality requirements. Further examination will find that other aspects of the process often overlooked were not sufficiently controlled and maintained. Thus, it only makes sense that in addition to wet chemistry, other factors such as resist developing, rinsing and nozzle maintenance, resistances in the plating cell, and agitation and filtration will contribute to overall quality. Ignore these at one's peril. **PCB**

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2. Primary Imaging for Pattern Plating, Part 2: Development, The PCB Magazine, June 2016.

Michael Carano is VP of technology and business development for RBP Chemical Technology. To reach Carano, or read past columns, click here.

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Electroplated Copper Filling of Through-holes: Influence on Hole Geometry

by Ron Blake, Andy Oh, Carmichael Gugliotti, Bill DeCesare, Don DeSalvo, and Rich Bellemare
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Abstract

This paper discusses a through-hole copper filling process for application in high-density interconnect constructions on thin IC and LED substrates where high reliability and thermal management are essential. The process consists of a two-step acid copper plating cycle. The first step utilizes periodic pulse reverse (PPR) electroplating to form a conductive copper bridge across the middle of a through-hole and is followed by direct current electroplating to fill the resultant vias formed in the bridge cycle.

The ability of the process to fill a variety of through-hole sizes on substrates of varying thickness while minimizing the overall surface copper build-up are critical in applications requiring efficient thermal management as circuit miniaturization continues.

The through-hole fill technology and factors that affect its performance such as substrate thickness and through-hole diameter will be presented in this paper.

Introduction

Resin or paste plugging of through-holes in cores has been a part of build-up technology, especially in IC substrate construction, for many years. Technological advances encompassing increased circuit density and stacked via construction, coupled with higher power devices, have added an extra dimension of thermal management where a copper filled through-hole becomes advantageous (Figure 1).

Advantages of copper filled through-holes include:

- Reduction in CTE mismatch of resin/paste plug
- Stable platform for stacking microvias
- Solid pillar structure within through-hole
- Lower likelihood of adhesion failure on the plated-over filled via
- High thermal conductivity of copper

New technologies were developed to completely fill through-holes and vias in build-up core layers in HDI and IC substrates with solid copper. Among the approaches for filling through-holes in a thin core board with copper was DC plating.

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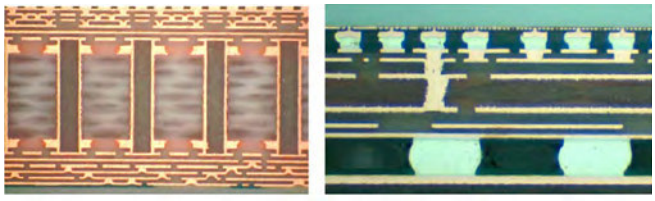

Figure 1: Paste-plugged vias and copper-filled vias.

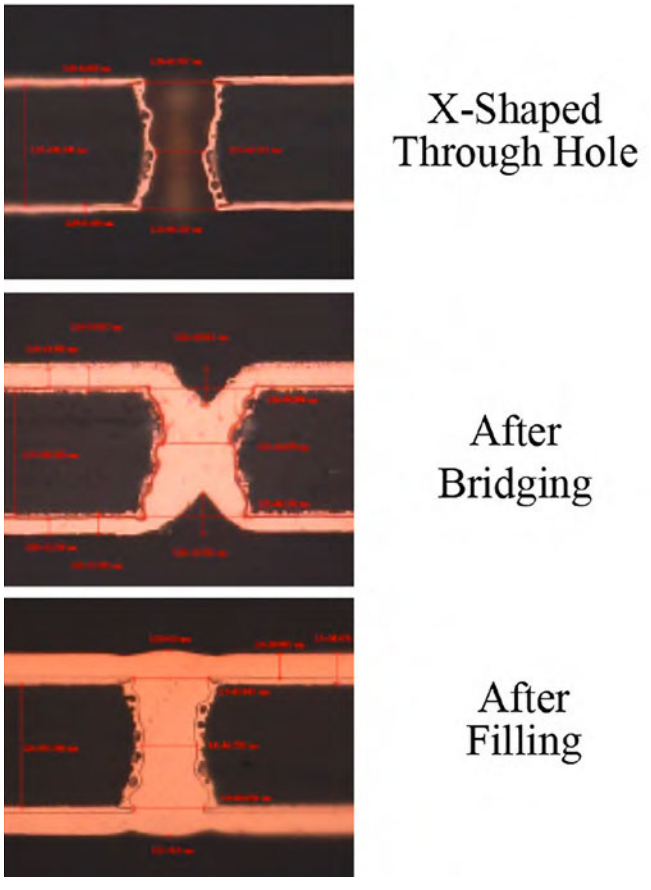

Figure 2: Stages of DC copper filling.

In this two-stage technique, one begins with an X-shaped through-hole. In the initial stage of plating, copper is preferentially deposited in the middle of the through-holes until the growing copper deposits meet to form a bridge. The resulting double-blind vias then fill to complete the copper filled through-hole. Terms to describe this process are bridge and fill (Figure 2).

The use of a single copper plating solution in a single step is the ideal process for filling through-holes with copper. For thin core materials of approximately 100 µm in thickness with through-holes of 100 µm diameter at the

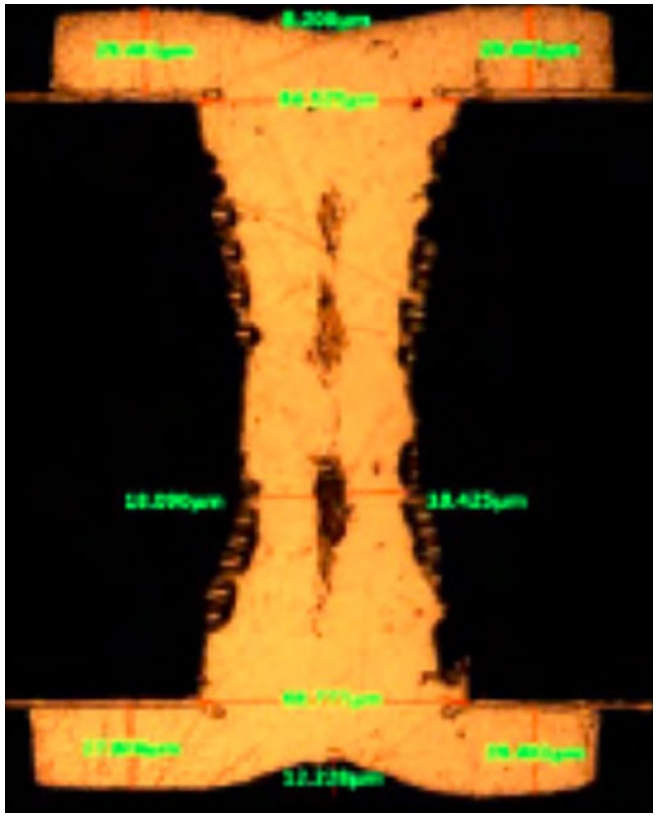

Figure 3: Cavity defects and surface copper in thicker substrates.

outsides and 50–70 µm at the middle, a plated surface copper thickness of less than 25 µm can be expected.

DC copper plating for through-hole filling is limited by the thickness of the substrate. As substrate thicknesses approach 200 µm, the propensity for the formation of cavities and inclusions increases as well as the necessity to plate much higher thicknesses of surface copper. This is due to extended plating times necessary to completely fill the through-hole (Figure 3). This effect is exacerbated for boards with mechanically drilled, straight walled, through-holes, as the "dogboning" tendencies of electroplating will tend to close the openings of the through-holes more quickly.

Background

Two-Step Through-Hole Fill Technology

In the two-step through-hole fill process, the bridging and filling steps are split into two

separate steps utilizing two different plating solutions. The advantage is that each process can be optimized for its intended function. The combined process offers a much more robust bridge and fill system capable of filling a broader range of hole diameters and substrate thicknesses with copper while minimizing excessive plated surface copper.

The two-step through-hole fill technology begins with either mechanically or laser-drilled through-holes processed through primary metallization including plasma and/or permanganate desmear and made conductive either through electroless copper or the commonly available direct metallization processes such as graphite, carbon black, or organic polymer. A flash plate of copper can be used to ensure conductivity across the entire through-hole wall.

The bridging of the center of the hole to form a double via utilizes a periodic pulse reverse copper plating system optimized to provide a cavity-free bridge with minimal surface copper. The filling of the resulting double vias utilizes via fill copper plating technology to provide accelerated filling of the vias while also minimizing surface copper.

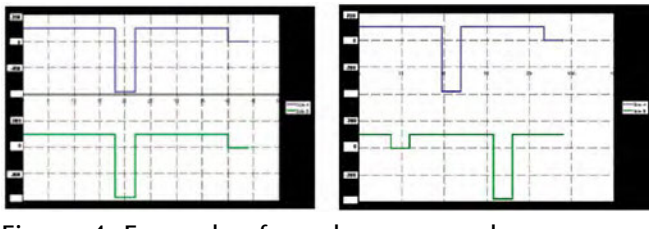

Figure 4: Example of synchronous and asynchronous waveforms.

Figure 5: Example of accelerated plating at hole center.

Bridge Step using PPR Plating

PPR plating is widely used for the conformal plating of high aspect-ratio through-holes. New rectifier designs and software now offer greater flexibility in developing complex waveforms that can provide plating results previously unobtainable. One of the features of newer rectifiers is the ability to impress asynchronous waveforms into a plating panel (Figure 4).

The use of asynchronous pulsed waveforms can accelerate the plating rate of the copper in the middle of the through-hole up to 5x that of conventional pulse waves (Figure 5).

The electrolyte components of the bridge solution are typical of acid copper plating solutions: copper sulfate, sulfuric acid, chloride ion, and additives. The concentrations in this study are presented in Table 1.

Filling Step Using Via Fill Plating

Copper via filling technologies have been widely used in the manufacturing of HDI and IC packaging substrates. Copper via fill baths are DC plating systems that are specifically designed for filling vias. They provide preferential copper deposition within the via and inhibited deposition on the surface (Figure 6).

This effect is accomplished by taking advantage of the difference in behavior of the additives in a via fill bath under different current density environments. The inside of the via is considered a low current-density area versus the surface of the substrate. Suppressor additives in the via fill chemistry adsorb onto and inhibit copper deposition in high current-density areas. The

Component	Concentration
Copper Sulfate	240g/L
Sulfuric Acid	110g/L
Chloride Ion	85ppm
Wetter	3%v/v
Brightener	0.05%v/v

Table 1: Bridge bath composition.

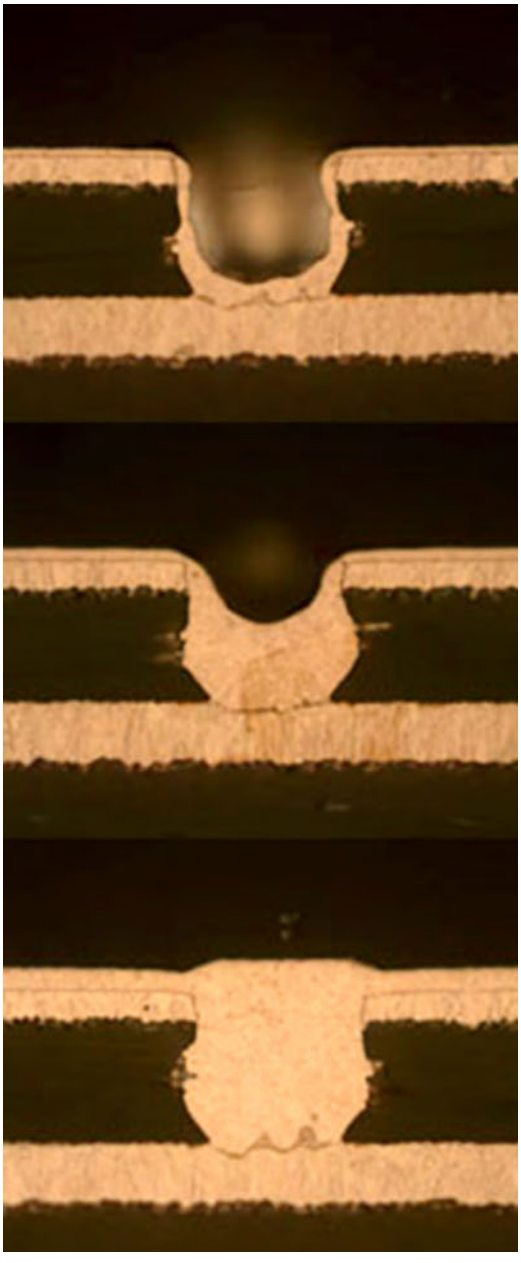

Figure 6: Example of accelerated plating within via.

brightener additives adsorb onto and accelerate copper deposition in low current density areas.

At the beginning of the fill process, where the current density differences between the bottom of the via and top are the greatest, the differential in deposition rate is greatest resulting in bottom-up filling. As the via fills, this differential in deposition rate decreases until the via is near filled, at which point the deposition rates in the via and on the general surface become equal due to the equalization of current densities. At this point, the copper deposits at an equal rate on both the surface and in the via.

Component	Concentration
Copper Sulfate	200g/L
Sulfuric Acid	100g/L
Chloride Ion	75ppm
Wetter	0.9%v/v
Brightener	0.45%v/v
Leveller	0.8%v/v

Table 2. Via fill bath composition.

The electrolyte components of the via fill solution are typical of acid copper plating solutions: copper sulfate, sulfuric acid, chloride ion, and additives. The concentrations in this study are presented in Table 2.

Experimental

One of the key steps in the through-hole bridge and fill process is the determination of the bridge cycle to form a via with a shape and dimensions that is optimal for filling. Generally, a via of approximately 7 mils or less in diameter with an aspect ratio of approximately 0.75–1.0 is preferred for optimal filling. In this paper, a constant hole diameter and substrate thickness were used to illustrate bridge optimization with respect to time. Plating was done for various times and via depth, aspect ratio, surface copper, and bridge thickness were recorded.

Measurements of plated substrates of various thicknesses, hole diameters, and pitches were collected from various sources under optimized bridge and fill cycles. The data was analyzed to demonstrate the effect of hole size and panel thickness on the resulting deposits.

Results

Bridge Optimization

The results of the bridging cycle testing with respect to time are summarized in Figure 7.

The results showed that the bridge thickness increased quickly and linearly during the early stages of the process where the copper deposit extends outward from the center of the hole to close it and then begins to thicken and grow

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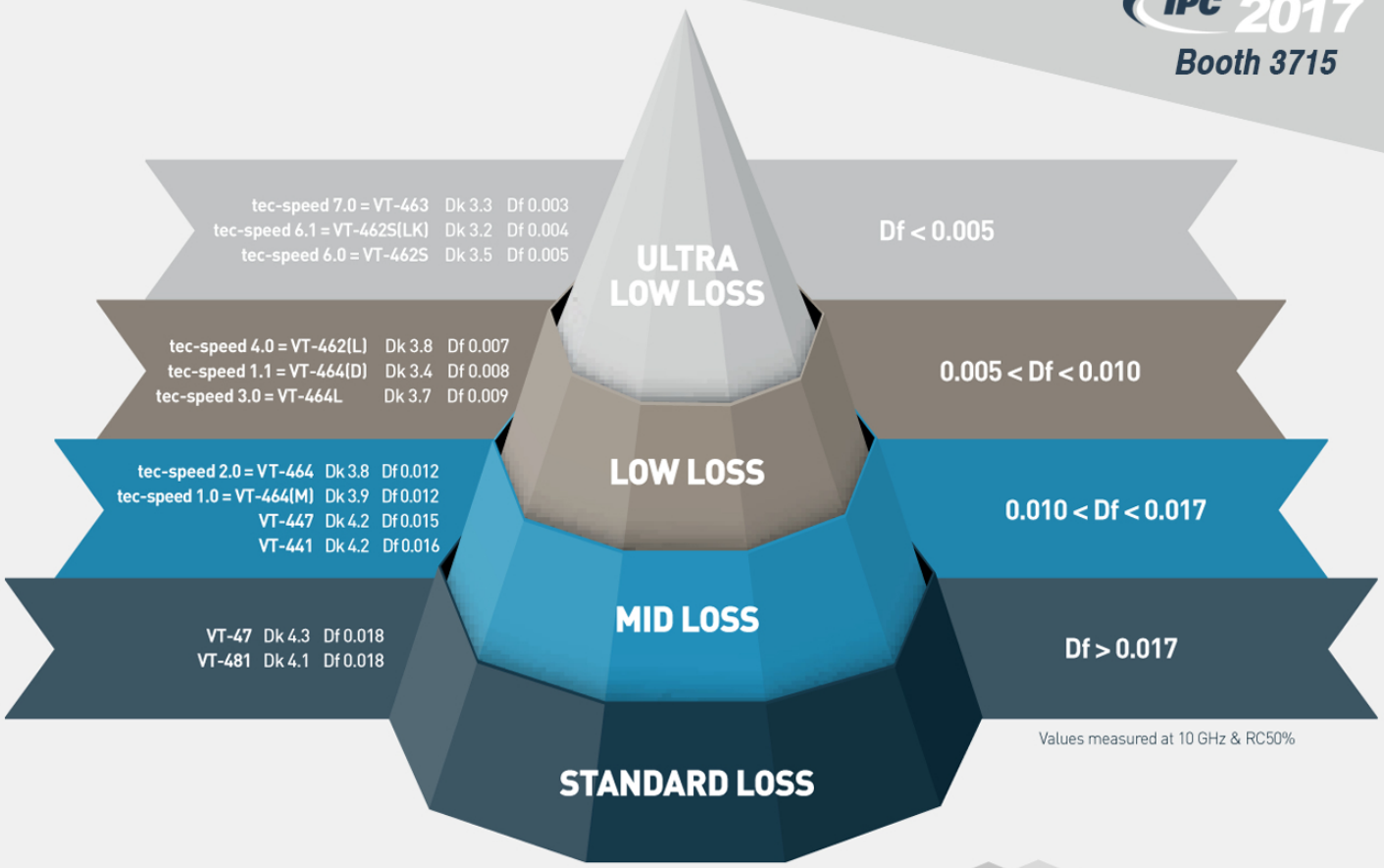

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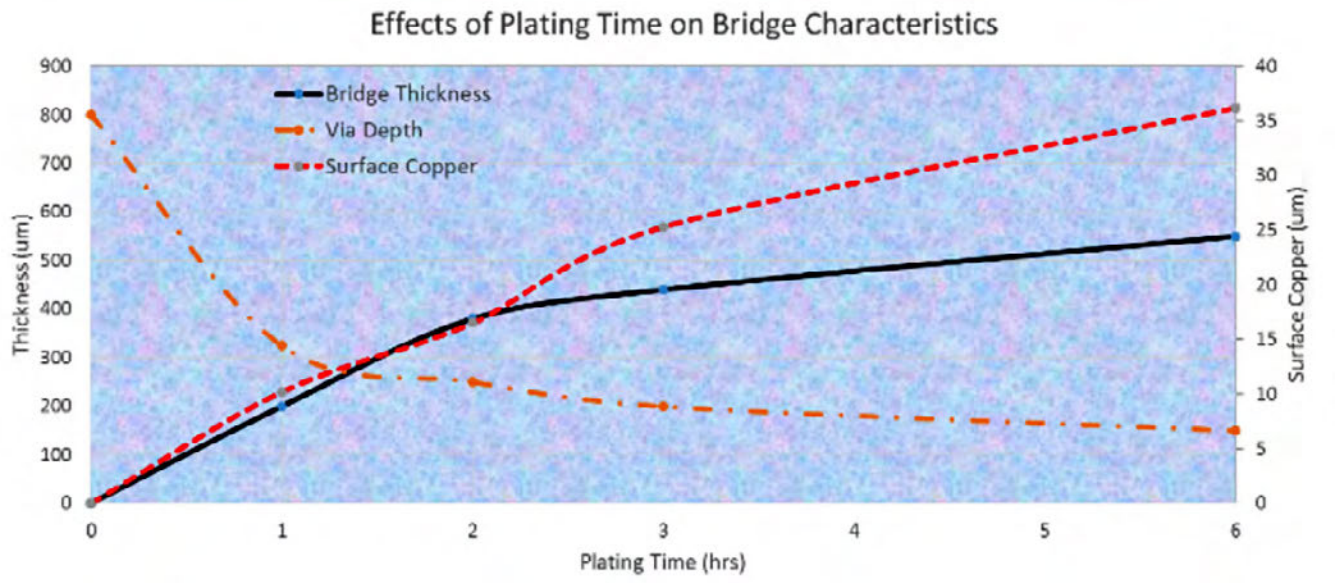

Figure 7: Bridge characteristics vs. plating time.

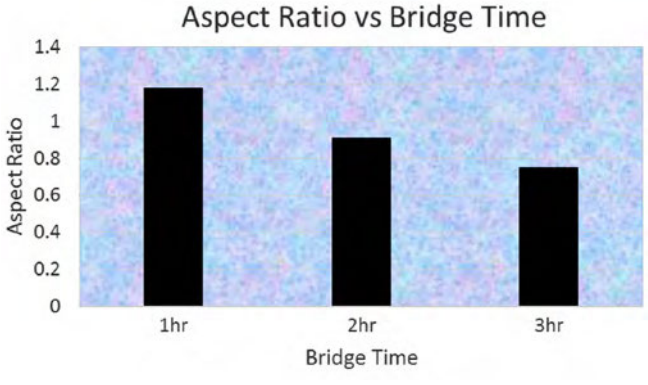

Figure 8: Via aspect ratio vs. plating time.

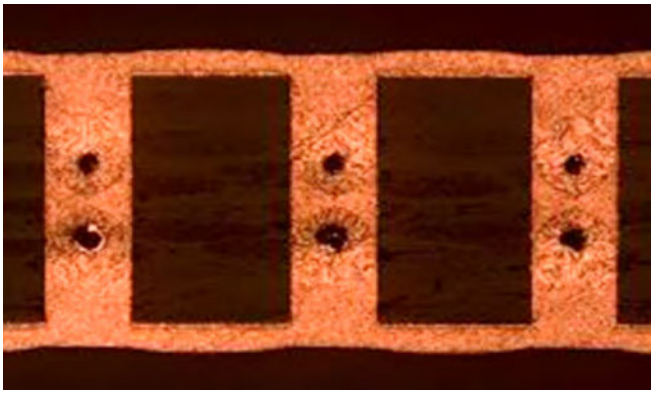

Figure 9: Cavities in high aspect-ratio vias.

towards either side of the substrate surface. At a certain point, the thickness of the bridge levels out, increasing only slightly with time. The via depth decreased greatly in the early stages of plating and leveled out at a certain point. This occurred in the region where the bridge thickness also leveled out indicating that little further change in via dimensions can be expected after this point.

The plated surface copper increased steadily during the entire process. Minimization of plated surface copper from the bridge step is dependent upon the total plating time necessary to form an optimum via.

The change in the aspect ratio of the vias formed on either side of the plated copper bridge are presented in Figure 8.

The results showed that the aspect ratio of the vias formed on either side of the bridge decreased with time. In this case, the desired aspect ratio of 0.75 was obtained in three hours for this particular hole size and substrate thickness. If the aspect ratio of the vias is too great, there will be a tendency to form cavities in the fill process, as the tops of holes will close faster than the via can fill (Figure 9). If the aspect ratios of the vias are too low or the diameters of the vias are too great, one will then get conformal plating due to

the mechanism of differential current densities previously discussed.

Effects of Hole Size and Substrate Thickness on Through-Hole Fill Results

The data of surface copper as a function of through-hole diameter and panel thickness is presented in Table 3. The main effects plots are presented in Figure 10. The total plated surface copper is the sum of the plating thickness from both the bridge and the via fill processes.

It is readily observed that hole diameter greatly affects the amount of total plated surface copper that can be expected for the through-hole copper filling process. As the diameter of the through-hole increases, the amount of surface copper that can be expected as a consequence of successfully meeting through-hole filling requirements, increases. This is because larger diameter holes require longer periods of time for the copper bridging process to extend across the diameter of the hole to close and form the vias and the longer periods of time to fully fill the resulting larger diameter vias. This can be substantial in the case of extremely wide holes.

It is also clear that panel thickness greatly affects the amount of total surface copper for sim-

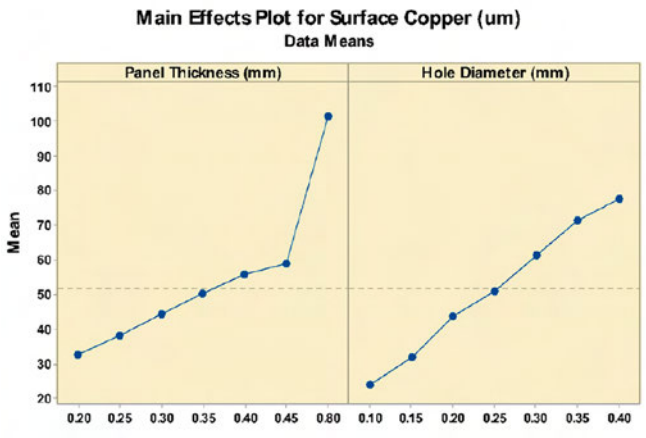

Figure 10: Main effects plot for surface copper.

Hole Diameter	Panel Thickness						
	0.2 mm 8 mil	0.25 mm 10 mil	0.3 mm 12 mil	0.35 mm 14 mil	0.4 mm 16 mil	0.45 mm 18 mil	0.8 mm 32 mil
0.1 mm 4 mil	20 µm	22 µm	24 µm	26 µm	28 µm		
0.15 mm 6 mil	25 µm	27 µm	30 µm	33 µm	36 µm	40 µm	
0.2 mm 8 mil	30 µm	32 µm	36 µm	40 µm	44 µm	48 µm	75 µm
0.25 mm 10 mil	35 µm	37 µm	42 µm	46 µm	50 µm	56 µm	90 µm
0.3 mm 12 mil	40 µm	44 µm	50 µm	56 µm	60 µm	70 µm	110 µm
0.35 mm 14 mil	45 µm	50 µm	58 µm	65 µm	72 µm	80 µm	130 µm
0.4 mm 16 mil		55 µm	70 µm	85 µm	100 µm		
0.45 mm 18 mil							

Table 3. Total surface copper vs. hole and panel dimensions.

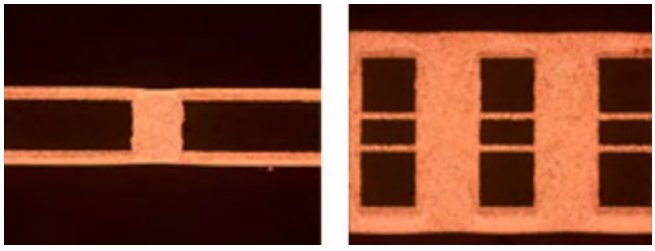

Figure 11: Effect of substrate thickness on surface copper.

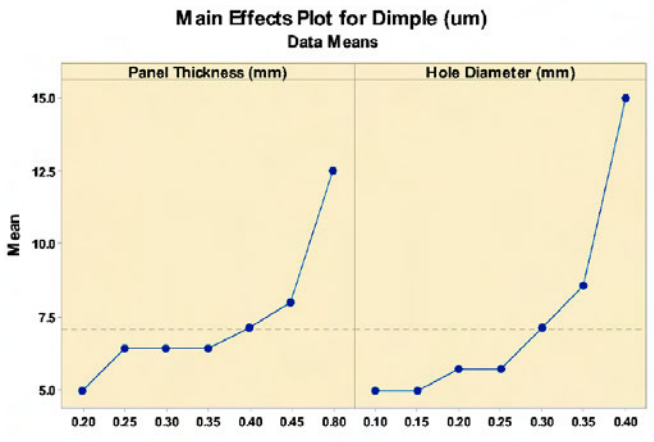

Figure 12: Main effects plot for dimple size.

ilar reasons. In the case of thicker panels, it requires more time for the bridge to build enough to provide vias of optimum aspect ratio. It logically follows that combining both large diameter holes with thicker substrates will result in more total plated surface copper than a thinner substrate with smaller diameter holes. This is illustrated in Figure 11. Plated surface copper for the thinner core material was 35 µm while the thicker core material was 93 µm.

Another important characteristic of the copper plated through-hole is the dimple size, especially if vias will be stacked or planarization is not desired. Figure 12 illustrates the main effects plots of hole diameter and panel thickness on dimple size.

Dimple size, as with total copper surface plating, is greatly influenced by hole diameter and panel thickness. Dimple size increases greatly with holes greater than approximately 0.25 mm in diameter and with panel thicknesses of greater that approximately 0.4 mm in thickness. The increase in dimple size with

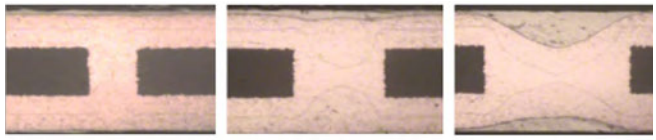

Figure 13: Effect of hole diameter on dimple size.

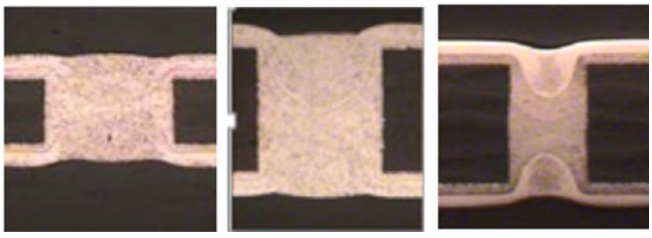

Figure 14: Effect of panel thickness on dimple size (0.25, 0.40, and 0.80 mm core).

hole diameter is due to the geometry of the vias formed in these larger holes after bridging. The larger diameter, lower aspect ratio holes will have more of a tendency to conformal plate due to the mechanisms of via fill previously discussed (Figure 13).

The increase in dimple size with panel thickness is due to the greater time in forming the bridge and getting an acceptable via while controlling the plated surface copper within reasonable limits. Figure 14 illustrates this effect on 0.35 mm holes in 0.25, 0.40, and 0.80 mm core materials where plating was stopped as the maximum allowed plated surface copper was reached.

Limited work was done on the effect of the pitch of an array of holes on copper through-hole filling in terms of dimple size. The results are summarized in Figure 15.

The results indicated that, for a set hole diameter and panel thickness, the lower the pitch of the through-holes (higher hole density), the larger the resulting dimple size. The reason for this phenomenon is that high-density arrays can be considered high surface area features. As such, they will act as lower current density areas requiring longer times and/or higher current densities to meet minimum requirements versus isolated areas.

The physical properties of copper deposited in the copper through-hole fill process are

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critical to the overall reliability of the electronic device in which it is used. Typical properties for the combined deposit are presented in Table 4.

Conclusions

As technological advances continue in the electronics industry in the manufacturing of substrates for applications in HDI, IC, and LED, new challenges will arise for the design engineers. With continued trends toward miniaturization, new manufacturing techniques such as stacking of vias, and the use of high power devices that generate considerable heat, the need for improved methods of thermal management are required to efficiently conduct heat away from the electronic devices to improve device reliability and life. Copper through-hole plating provides another tool to the engineer for the design of electronic circuitry. Figure 16 illustrates a real-world application of copper through-hole plating to conduct heat away from an LED device allowing it to operate at a lower temperature. In this example, the use of copper through-hole filling reduced the operating temperature of the device from 126°C to 92°C.

The copper through-hole plating process provides a versatile two-step process consisting of a periodic pulse reverse step with specialized waveforms that allow the middle of a through-hole to be bridged and sealed, forming two microvias that can subsequently be filled with DC-based via fill chemistries.

The design engineer must understand the nuances of the copper through-hole plating process and how the design of the board

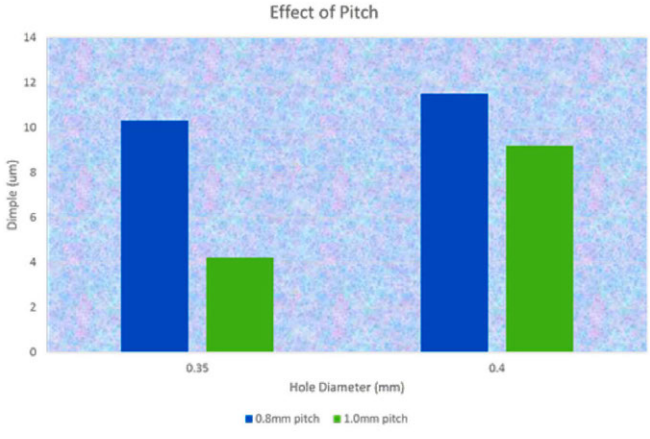

Figure 15: Effect of hole pitch on dimple size.

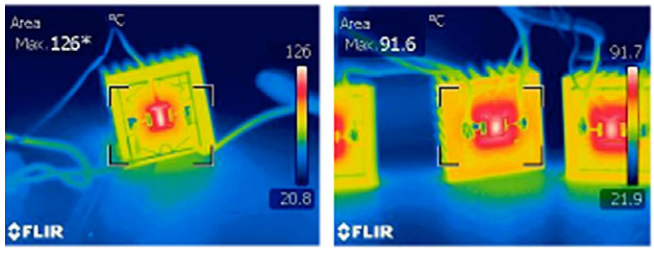

Figure 16: Use of copper through-hole plating to conduct heat (right photograph).

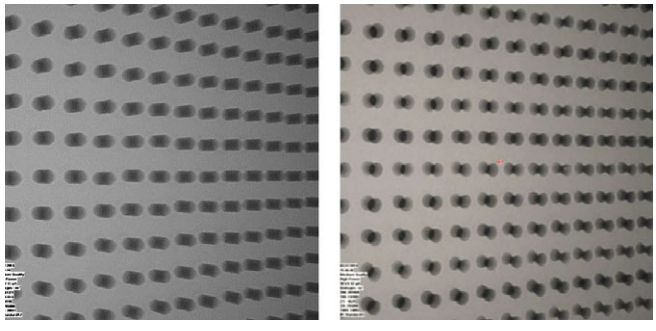

Figure 17: X-ray imaging of copper through-hole plating.

Plating Cycle	Sample #	Plated Copper Thickness (mil)	Break Force (lbf)	Weight (g)	Elongation (%)	Tensile Strength (PSI)
Copper plated with bridging plus via fill process	1	2.82	62.75	0.9726	21.92	47098.0
	2	3.23	72.83	1.1146	21.19	47699.5
	3	2.71	60.21	0.9348	20.79	47018.9
	4	2.87	62.89	0.9901	19.46	46368.8
	5	3.05	68.12	1.0510	22.47	47314.6
	mean	3.94	65.36	1.0126	21.17	47100.0

Table 4: Typical Properties of Copper Through-Hole Fill Deposit.

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influences the results of each step of the plating process. The results presented in this paper illustrate the influence that board design features such as hole size and pitch and core thickness have on the critical outputs of the plating process such as ability to bridge, total plated surface copper, dimple size, aspect ratio, and total process time. When designing a substrate for the utilization of copper through-hole plating, the design engineer must choose a suitable substrate and thickness and incorporate hole sizes and layouts that will minimize output variations. In this way, a robust, reliable copper through-hole process can be realized (Figure 17). **PCB**

This paper was originally presented at SMTA International 2016 in Rosemont, IL, USA, and published in the proceedings.

Ron Blake is senior process specialist

Andy Oh is technical service specialist

Carmichael Gugliotti is metallization applications specialist

Bill DeCesare is research engineer

Don DeSalvo is global product development manager

Rich Bellemare is global applications manager, metallization

An Interview with TTM President Thomas Edman

The TTM and Viasystems merger put the PCB industry on notice last year when it created one of the biggest powerhouses in the world. At the recent HKPCA and IPC show, I-Connect007 Publisher Barry Matties met with TTM Technologies President and Chief Executive Officer, Thomas Edman, to get his views on the market, technology, the culture of TTM, and even the Trump effect.

***Barry Matties:** Thomas, please start with an overview view of TTM for our readers.*

Thomas Edman: We are now the largest manufacturer of rigid printed circuit boards in the world and the second largest overall, and that›s mainly due to the acquisition of Viasystems, which nearly doubled the company's size to about $2.5 billion in revenue. We have 25 production facilities worldwide, three of which are smaller assembly operations, and the rest focus on manufacturing printed circuit boards.

***Matties:** And how do you look at the markets?*

Edman: When TTM looks at the markets we serve, we›re very focused on what our end-markets and our customers are requiring. Looking at technology trends in the industry today, a lot of focus is on miniaturization and really shrinking down the space and improving information content. We see an emphasis is on speed, and sensing applications are becoming more critical as well, certainly in the automotive space.

As we look at process technologies, we're focused on reducing lines and spacing. That's a regular cadence of improvements that we're involved with. We're also very focused on continuing to improve our RF processing capability, both in the U.S. and Asia.

To read the full interview, click here.

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ENIPIG–Next Generation of PCB Surface Finish

MACFEST Dissemination Webinar, December 2016

by Pete Starkey
I-CONNECT007

MACFEST is a multi-partner project co-funded by Innovate UK to develop an electroless nickel/immersion palladium/immersion gold (ENIPIG) "universal surface finish" for printed circuit boards. Project partners are University of Leicester, MTG Research, C-Tech Innovation, A-Gas Electronic Materials, Merlin Circuit Technology and the Institute of Circuit Technology. Now in its 23rd month of 24, project progress to date has been reported in a webinar moderated by specialist in electronics assembly technology Bob Willis.

Representing the Materials and Interfaces research group at the University of Leicester, Professor Karl Ryder explained the background to the project and its key aims: to develop new high-performance solderable and wire-bondable finishes based on deposition from ionic liquids, with improved coating quality and solderability, to give improved solder joint reliability in harsh operational environments. The process would be compatible with existing printed circuit manufacturing processes, with low environmental impact and no toxic components.

Professor Ryder described the nature of ionic liquids and recounted some of their many successful applications in metal finishing processes. Deep eutectic solvents were a class of ionic liquid of particular interest for industrial processes because of the ready availability of their constituents in bulk quantities. They were composed of organic cations with halide anions and complexing agent to make anionic complexes. Specifically, a deep eutectic solvent known as Ethaline 200, composed of ethylene glycol and choline chloride in 2:1 molar ratio, had been used as the basis for the immersion deposition processes developed in the MACFEST programme. It was relatively inexpensive, had low environmental impact and offered unusual solvation properties with metal salts. Additionally, it readily dissolved metal oxides and could be very successfully used in innovative soldering fluxes.

He referred to previous successful projects associated with printed circuit finishes: IONMET which had resulted in a low-temperature immersion silver process showing reduced sol-

Bob Willis

Professor Karl Ryder

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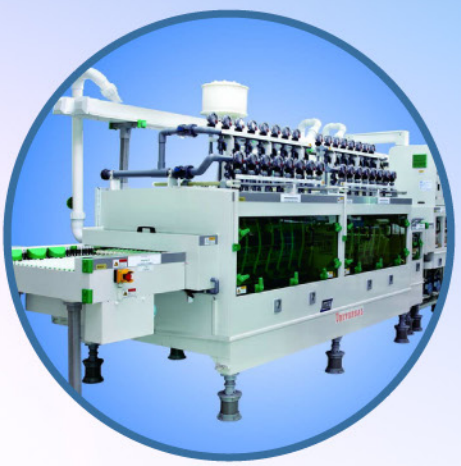

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der-mask attack and excellent surface wetting by solder, whilst eliminating nitric acid, and ASPIS which had studied the mechanism of the black pad effect associated with the widely used electroless nickel/immersion gold finish (ENIG) and concluded that the acidic components in aqueous immersion gold chemistry caused corrosion at the grain boundaries of electroless nickel, which could be avoided by using ionic liquid chemistry.

MACFEST had extended the knowledge gained from the ASPIS work to develop an ENIPIG finish, based on deep eutectic solvents, as a high-reliability alternative to ENIG, with improved functionality and reduced toxicity and environmental impact.

Using a standard commercial phosphorus electroless nickel as the base layer, a novel immersion process had been used for depositing palladium, based on palladium chloride in Ethaline, operating at 80°C, to give a coating thickness of 70–100 nanometres in 20 minutes. This was then overplated with immersion gold at 50°C for 9–15 minutes from an Ethaline solution containing gold as either gold chloride or sodium gold thiosulphate, which was both acid-free and cyanide-free. A study of the effect of the immersion coating on the electroless nickel substrate revealed no evidence of the type of corrosion effects seen on conventional ENIG, and hence no possibility of black pad failure.

Initial solderability testing had shown rapid solder-substrate interaction, with consistent performance across multiple samples, for gold plating times of nine, 12 and 15 minutes. And there was no evidence of voiding or grain boundary attack.

In a separate exercise, the solderability was independently benchmarked by Bob Willis in cooperation with Merlin Circuit Technology, and the results were reported by Tom Jones from Heriot-Watt University, studying at Merlin for an engineering doctorate. He described in detail the test vehicles supplied by Willis, each of which included 18 test coupons for solder spot and wetting balance measurements, with six rows of tracks for spot pattern, 22 paste dots and seven pads for wetting balance measurement. These were plated with ENIPIG from the process formulated at Leicester, and plating thicknesses measured by X-ray fluorescence against the relevant IPC specification. Prior to solderability

Tom Jones

testing, coupons were subjected separately to reflow oven heating and vapour phase heating, then left for four days. Reference samples had no thermal pre-conditioning. Jones showed a series of wetting balance and spot-wetting test results comparing the ENIPIG samples with ENIG, copper-OSP, immersion tin and HASL.

On the wetting balance, ENIPIG performed well in terms of soldering force and wetting speed, and the spot wetting test demonstrated that ENIPIG was comparable to or better than ENIG that had been pre-conditioned under equivalent conditions. Separate test boards had been designed for wire-pull and ball-shear testing, but the results were not yet available.

The MACFEST webinar prompted a very lively question-and-answer session, moderated by Bob Willis, and it was clear that there was considerable interest in following the progress of the project. In fact, a recording of the whole of the webinar, including the slides, the audio presentations and the Q&A session is available by clicking here. **PCB**

Pete Starkey is based in the UK, and joined I-Connect007 as technical editor in 2008. Starkey has more than 30 years of experience in the PCB industry, with a background in process development, technical service and technical sales. To contact Starkey, click here.

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MilAero007 Highlights

Cartel Electronics Signs Definitive Agreement to Acquire Cirtech

On December 1, 2016, Cartel Electronics Inc. and its affiliates signed a definitive agreement to acquire Cirtech Inc.

One World, One Industry: Strengthening Your Value Proposition to Boost Organization Success

John Mitchell's new column's title says it all: One World, One Industry. In the coming columns, the IPC president will be covering issues affecting the entire global electronics industry supply chain with specific expertise on global standards, education, advocacy and solutions.

Tin Whisker Mitigation Methodologies: Report from SMART Group, Part 1

Since the introduction of the RoHS legislation in 2006, the threat of tin-whisker-related short circuit failure from pure tin finished components has remained a major concern within the high-reliability electronics manufacturing industry. In this article, Editor Pete Starkey reviews a recent seminar by the SMART Group to discuss tin whisker mitigation methodologies and strategies.

IPC Study on N.A. PCB Industry Reports Growth in Milaero Market

Printed circuit boards for military and aerospace applications remain the largest vertical market segment for PCB manufacturers in North America, representing about one-third of the market. And it is the only vertical market segment expected to grow in 2016 as a share of the North American market, according to IPC's 2016 Analysis and Forecast for the North American PCB Industry.

Orbit International's Electronics Group Lands $1.23M U.S. Navy Contract

Orbit International Corp.'s Electronics Group has received an award from a U.S. Government Procurement Agency valued in excess of $1,230,000 for its MK 119 Gun Computer System Cabinet (GCSC).

Eltek Signs Definitive Agreement for the Sale of Kubatronik

Eltek Ltd. announced today that it has signed a definitive agreement for the sale of all the Kubatronik-Leiterplatten GmbH (Kubatronik) shares it holds to Mr. Alois Kubat, Kubatronik's only other shareholder and founder. The parties expect to consummate the transaction by the end of 2016.

Sanmina's Salt Lake City Facility Earns AS9100C Certification

Sanmina Corp.'s Salt Lake City, Utah facility has been awarded the AS9100C certification for printed circuit board assemblies (PCBAs), subassemblies and systems.

Ellsworth Now Authorized Distributor of Henkel Products for Aerospace Industry

Ellsworth Adhesives has announced that it is now an authorized distributor of Henkel's surface treatments and structural adhesive products for the aerospace industry in Canada.

Laser-based Navigation Sensor Could Be Standard for Planetary Landing Missions

A laser-guided navigation sensor that could help future rovers make safe, precise landings on Mars or destinations beyond will soon undergo testing in California's Mojave Desert.

The Trump Effect on the Rules of Engagement

For many decades, and more so than any other nation, the U.S. helped shape the world we live in. Directly or otherwise, Washington nurtured the institutions that helped establish the international economic rules of the game.

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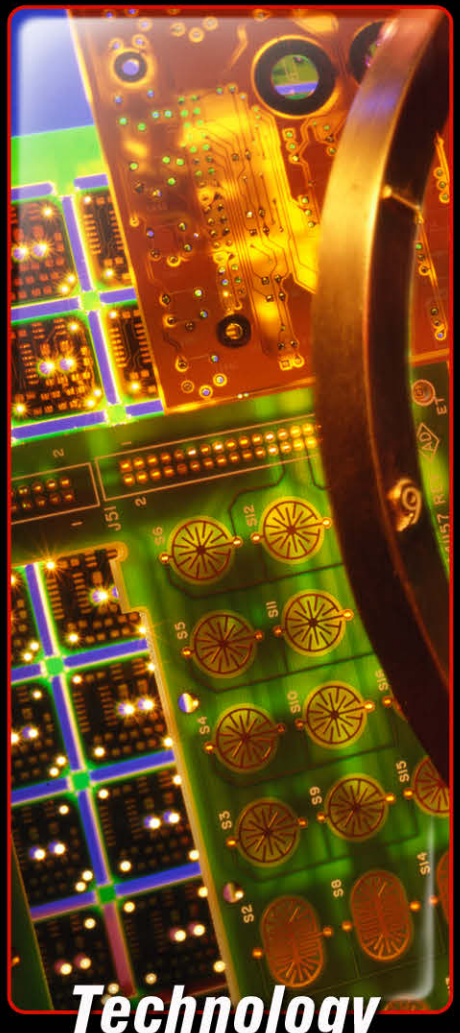

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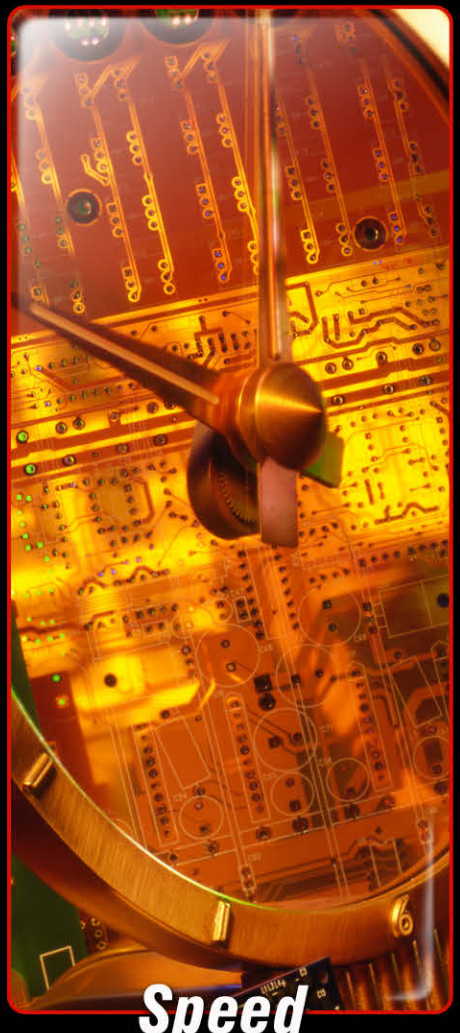

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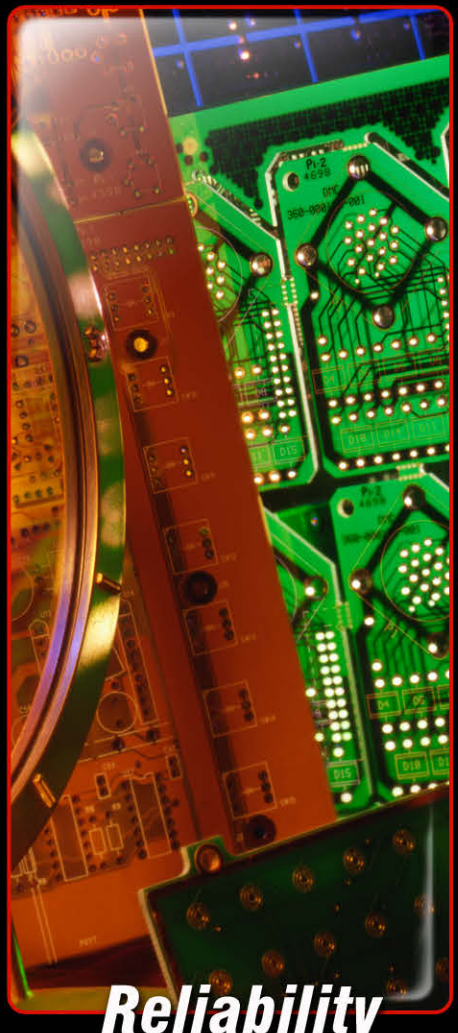

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Implications of the Trump Presidency

by John Mitchell
IPC—ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

Later this month, Donald Trump will enter the White House as the 45th president of the United States. Regardless of whether you are a Republican, Democrat, or Independent, we at IPC believe this leadership change will present meaningful opportunities for the electronics industry.

Under normal circumstances, the newly unified Republican control of Congress and the Executive Branch could be expected to translate into a more coherent, pro-business governing agenda. However, President-elect Trump is not a traditional Republican, and his operating style often detracts from the merits of his message. There are some who suggest that the new president's plans might diverge enough from those of the Republican Congress that a legislative stalemate may ensue.

What does this mean for the worldwide electronics industry?

Our biggest concern is the impact on international trade. Specifically, President-elect Trump has said he would drop U.S. participation in the Trans-Pacific Partnership (TPP), put a hold on the Trans-Atlantic Trade and Investment Partnership (T-TIP), seek to renegotiate NAFTA, slap higher tariffs on imports from China, and seek greater penalties on nations accused of dumping products or raw materials and committing intellectual property violations.

If these drastic U.S. policy shifts are pursued and enacted, we might expect to see a strong outcry from the business community and the general public. Increased uncertainty is rarely good news for most businesses, and that's especially true in the complex world of trans-national trade.

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Also, considering that many electronics products and components are manufactured overseas, the price of these devices could jump by nearly 50% if the tariffs described during the campaign are enacted.

Likewise, President-elect Trump's promise to renegotiate NAFTA will affect many industries but especially the U.S. automotive sector, which has outsourced much of its production to Mexico. Electronics account for up to 30% of the cost of today's cars, and some economists have estimated that a total repatriation of automobile manufacturing to the U.S. could increase the consumer cost of small cars by $5,000 each.

The road to higher consumer prices resulting from a more protectionist U.S. policy is one that few will want to travel.

In addition, the President-elect's anti-immigration views could affect many electronics manufacturers and their customers in the United States, where there is already a skilled worker shortage. American citizens with the skills needed to staff advanced manufacturing facilities simply are not available in the numbers required.

Part of the answer is workforce development initiatives and higher educational standards at all levels, especially in science, technology, engineering and math (STEM). To help meet this need, IPC is committed to being a leader in training and certification courses. Our new learning-management platform, IPC EDGE, is designed to deliver the knowledge and skills necessary to excel in the electronics industry.

On each of these major issues, President-elect Trump was somewhat vague and contradictory during his campaign, so understanding how he will govern and seize opportunities will require significant government relations work and agility on our part.

On the bright side, we are optimistic that a one-party government will pave the way to progress in several important areas. For example, we expect that President Trump and leaders in Congress will collaborate on a corporate tax reform package that will stimulate business growth and investment. We also expect that a Trump administration will take a lighter approach to regulation, including a better balance among the risks, costs and benefits of new rules, and a better grounding in the best available scientific research.

As an industry, we will move forward, and IPC—whose chief goal is to ensure the success of our members—looks forward to playing an active part in that progress.

Because at the end of the day, we make progress together—part of one world, and one industry. **PCB**

John Mitchell is president and CEO of IPC–Association Connecting Electronics Industries. To read past columns or to contact Mitchell, click here.

Design Your Own Custom Drone

New FAA regulations have made drone flight easier than ever for companies and consumers. A new system from MIT's Computer Science and Artificial Intelligence Laboratory (CSAIL) is the first to allow users to design, simulate, and build their own custom drone. Users can change the size, shape, and structure of their drone based on the specific needs they have for payload, cost, flight time, battery usage, and other factors.

To demonstrate, researchers created a range of unusual-looking drones, including a five-rotor "pentacopter" and a rabbit-shaped "bunnycopter" with propellers of different sizes and rotors of different heights.

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Now is the Time for Comprehensive Tax Reform

by John Hasselmann
IPC GOVERNMENT RELATIONS

Tax policy is among the most basic tools of any government to accomplish its objectives. From the private sector perspective, taxes are one of largest expenses of any business.

But despite being such an important topic for government and business, there is widespread agreement that the U.S. federal tax code is a mess. Most observers agree it does not strike the right balance between ensuring fairness and simplicity, raising needed revenues, and spurring economic growth.

Now, with the new political line-up in Washington, D.C., the prospect of sweeping tax reform is back at the center of political debate, and it's crucial that policymakers strike a better balance.

It has been 30 years since there has been a comprehensive overhaul of the federal tax code. Today, the U.S. has the third-highest corporate income tax burden[1] in the world at 39%. Many nations in the Americas, Asia, and even Europe have much lighter tax burdens, putting the U.S. at a competitive disadvantage. And because the tax code is filled with special provisions to lower taxes for various favored groups, the overall tax rate must be higher to compensate for this imbalance.

President-elect Donald Trump, House Speaker Paul Ryan (R-WI) and Senate Majority Leader Mitch McConnell (R-KY) have all said they want to enact a sweeping tax reform package that cuts the overall tax burden for individuals and businesses. The chairman of the House Ways and Means Committee, Rep. Kevin Brady (R-TX), says House Republicans are ready to move a bill in 2017.

Donald Trump's campaign tax plan[2] proposed lowering the corporate income tax rate

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—David Dibble

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from 35% to 15%, eliminating most business tax credits except the R&D credit, and allowing accelerated write-offs for capital investments. Chairman Brady's plan[3] is similar in that it would lower the corporate rate to 20% and shift to a territorial system under which revenues earned abroad would not be double-taxed in both the United States and the country of origin.

Meanwhile, it has been a year since Congress enacted, and President Obama signed, the Protecting Americans from Tax Hikes (PATH) Act in December 2015.

> "IPC and many other business groups fought hard for the PATH Act, which provided for long-term extensions of more than 50 tax provisions that were previously renewed—or not—on an annual basis."

IPC and many other business groups fought hard for the PATH Act, which provided for long-term extensions of more than 50 tax provisions that were previously renewed—or not—on an annual basis. Among those provisions were a permanent extension of the R&D tax credit and the extension of bonus depreciation. Both were significant victories for companies that rely heavily on R&D to stay competitive in the global economy, which includes nearly all IPC member companies.

IPC continues to advocate for a stronger R&D tax credit by supporting H.R. 5187, the Research and Experimentation Advances Competitiveness at Home (REACH) Act of 2016, introduced by Rep. Patrick Tiberi (R-OH), which would increase the alternative simplified credit (ASC) from 14% to 20%. Although the PATH Act made the R&D tax credit permanent, the ASC was kept at the 14% rate. Most IPC members utilize the ASC, which is an alternative method used to compute tax credits for R&D.

An interesting aspect of the tax reform debate is that the PATH Act improved the budget baseline by raising more than $500 billion, which should make it easier for Congress to lower tax rates this time around. However, the lower rates could come at the expense of eliminating many of the special provisions that impact various industries. During a time when the United States is working so hard to bring back and retain manufacturing jobs, one idea that IPC is exploring is a lower tax rate for advanced manufacturing that is done in the United States.

Even if the momentum for tax reform continues to build, there will be many hurdles to cross: competing proposals, hearings, committee markups of draft legislation, committee votes, floor votes, and a possible House-Senate conference committee to iron out differences between the two chambers' approaches.

IPC will lead efforts on tax reform specific to our industry as well as work in collaboration with other industry associations to advocate for the best possible balance among all the competing priorities. Tax policy will be among the priority topics of IMPACT Washington, DC 2017[4]—our annual executive-level advocacy event—coming up on May 1–3, 2017. But with one-party control of the Congress and the White House, we are cautiously optimistic that policymakers will complete the process and for the first time in decades, the United States will revamp its tax code to be more competitive in the global economy.

Stay tuned! **PCB**

References

1. How U.S. Corporate Tax Rate Compares to the Rest of the World
2. Donaldjtrump.com
3. A Better Way Tax Snapshot
4. IMPACT Washington DC 2017

John Hasselmann is IPC's VP of Government Relations. To contact him, click here.

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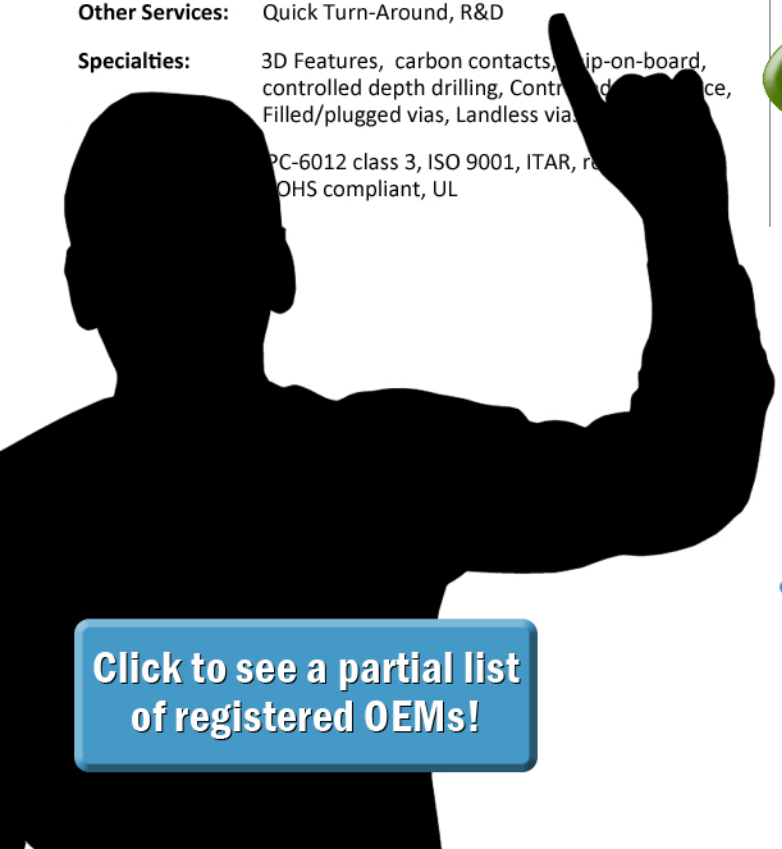

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Fake News: It Could Happen to You

by Barry Lee Cohen
LAUNCH COMMUNICATIONS

This month's column was written a month after a historic U.S. presidential election that pitted a business billionaire that previously never ran for public office versus a 30-year public servant who was the first female nominee of a major political party. As the state-by-state results rolled in late into the evening and stretched into the wee hours of the morning, most major media outlets begrudgingly declared the winner. Like a hanging chad blowing in the wind, each outlet's entourage of political pundits was bewildered and began questioning, "How did the polls get it sooo wrong?" To a much lesser and refreshing extent, admissions of honesty were expressed that ranged from, "We blew it," to "Let's see if the boss renews my contract."

Many hypotheses were and continue to be offered as to the "surprising results." Several invoked the fragile reliability of casino betting odds (no joking!), whereas most revolved around the media and "fake news," as reported by The New York Times. On this last prognostication, claims flourished that fake news posted on Facebook (and spread to other social media channels) potentially influenced the election results. Given that well over 50% of those eligible to vote in the U.S. obtain all or part of their news via social media, such claims are disturbing at a minimum when you consider that anyone can write "news" and post it for virtually anyone that chooses to read—and believe—it.

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Make no mistake about it: Fake news occurs at your company too. Although to a much smaller extent than a presidential election, the impact that fake news has on a company's reputation, employee confidence, customer trust and bottom line can be substantial.

Blast-off

To combat erroneous information, incorrect assumptions, and the lack of business integrity and ethics you may experience by some competitors or former, disgruntled employees, it takes a village of internal and external communications.

> "Make no mistake about it: Fake news occurs at your company too."

Internal communications via email is the predominant method used by HR and corporate management to inform team members as to changes in corporate capabilities and organizational structure. It's also used more selectively on new product and service introductions. However, the overuse of email has somewhat diluted the impact and perceived importance for many recipients, even when sent by senior management. Therefore, town hall meetings followed by department discussions are highly advised, as there is still no substitute for "looking them in the eyes" whenever possible. And, if getting those warm bodies in the same room is not feasible, it's even more of a reason to employ webinars, Skype or other live video alternatives. For many large companies, easel pads and bulletin boards are being replaced with digital displays placed throughout common areas of their campuses, thereby enabling their communications to be largely unobstructed from cloistered cubicle chatter and other non-productive distractions.

For those companies with employee Intranets, podcasts and video clips, along with transcripts or consolidated notes summarizing the meeting presentations, should be posted as a reference. This is especially important when reviewed by employees with different first languages.

In terms of external communications, the lightning-fast speed that news is disseminated in our digital era necessitates companies to deploy a wide net of tactics to successfully refute false news. Should it be a combination of social media (yes!), targeted e-newsletters (yes!), and other methods (yes!), your company should have an integrated plan in place as part of its standard operating procedures to respond to rumors, ridiculous claims, and unsubstantiated information. The plan should entail the use of the company's existing communications platforms. If your company has been communicating on a regular basis, rebuttals to false news being made by enemy combatants will be weighed more thoughtfully, as your company has earned a level of credibility and trust.

Centric to social media, strategically increasing and cultivating connections on LinkedIn (yes!) and followers on other selected channels are critical to ensuring your communications are heard and shared. Connections who are truly engaged in your business are more likely to be more responsive to your comments. In essence, they become a communications network that will spread your gospel. Conversely, these folks are more likely to be more circumspect of questionable statements being made about your organization.

Most importantly, it is senior management's responsibility to provide an open environment to effectively foster and lead discussions on topics that address current and future concerns. The worst mistake is not communicating at all, whereas the organization will most often find itself responding in a defensive mode. Not communicating regularly will cast a company as being insular and, yes, fake. **PCB**

Barry Lee Cohen is president and managing director of Launch Communications. To read past columns or to contact Cohen, click here.

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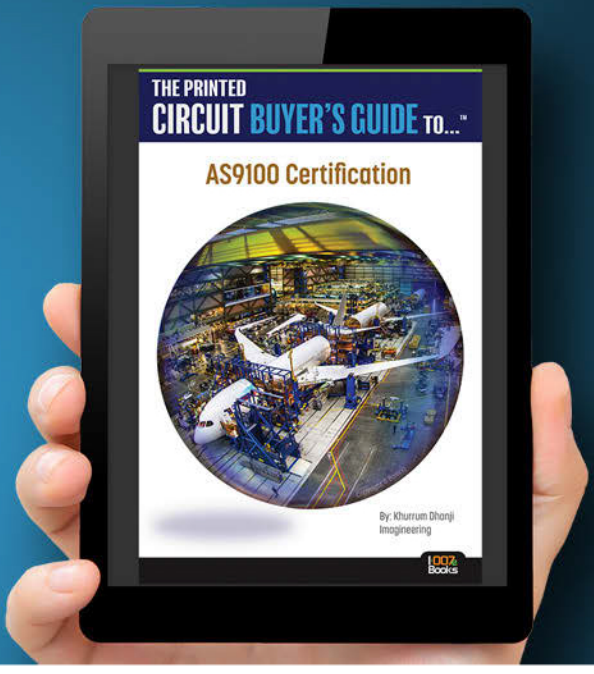

I-Connect007 is excited to announce the release of the first title in its *Printed Circuit Buyer's Guide to...* series, ***The Printed Circuit Buyer's Guide to... AS9100 Certification***.

Authored by industry veteran Khurrum Dhanji, of Imagineering, Inc., this is a must-read for buyers, specifiers, engineers or anyone involved in the procurement of printed circuit boards.

The *Printed Circuit Buyer's Guide to... AS9100 Certification* provides a high-level overview of the standard, as well as a breakdown of each of the five major requirements.

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- ***The Printed Circuit Buyer's Guide to... Solderless Assemblies*** by Joe Fjelstad
- ***The Printed Circuit Buyer's Guide to... Flex Design*** by American Standard Circuits
- ***The EMS Buyer's Guide to... Choosing the Right Contract Manufacturer*** by Zentech

We hope you enjoy *The Printed Circuit Buyer's Guide to... AS9100 Certification*.

TOP TEN

Recent Highlights from PCB007

1 EuroTech: Institute of Circuit Technology Northern Seminar 2016, Harrogate

A new location for the Institute of Circuit Technology Northern Seminar: Harrogate, the elegant and historic spa town in North Yorkshire, England. And an impressive venue: the chandeliered drawing room of the palatial and stately Majestic Hotel, dating from the Victorian era.

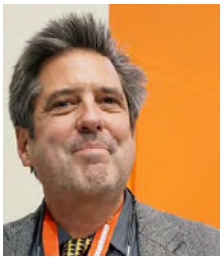
2 Weiner's World

Here we go again! The winter holiday (and trade show) season is upon us. Electronica's mood was upbeat. Next, the Asia and San Diego shows. We just received word as we were preparing for our trip to next month's HKPCA/IPC event in Shenzhen, China that the CPCA show suddenly changed its March 2017 date and venue.

3 TTM President Thomas Edman on the Global PCB Market, Technology, and More

The TTM and Viasystems merger put the PCB industry on notice last year when it created one of the biggest powerhouses in the world. At this year's HKPCA and IPC show, Barry Matties met with TTM Technologies President and Chief Executive Officer, Thomas Edman to get his views on the market, technology, the culture of TTM and even the Trump effect.

4 KCE Group: A Thailand-Based PCB Manufacturer with a Growing Global Footprint



Recently, while at electronica in Munich, Germany I-Connect007's Judy Warner met KCE America President Rick Rhodes, and Joe Yeo of KCE Group. They discussed the unique challenges and opportunities that come with the rigorous automotive market, and explained why they continue to enjoy explosive growth.

5 EPTE Newsletter: Preliminary PCB Industry Results For 2016

I can't believe we are in the last month of 2016. We have almost a year of sales data from the global printed circuit industry, so this is a good time to analyze this year's performance and consider business plans for 2017. Since printed circuits are the major components in electronic products, let's review PCB market trends in the global electronics industry.

6 IPC APEX EXPO 2017 to Debut Flexible Hybrid Printed Electronics Pavilion

Apart from its more than 450 industry-leading exhibitors, the IPC APEX EXPO 2017 will debut its Flexible Hybrid Printed Electronics Pavilion to offer attendees a great opportunity to experience how these trending printed electronics products and technologies apply to hybrid PCBs and PCB assemblies.

7 All About Flex: Disruption in the Supply Chain

Manufacturers need a highly dependable supply chain to successfully support their products. This is especially true of custom designed and built components, as many times, only one supplier is available for a component since tooling and development costs discourage dual sourcing.

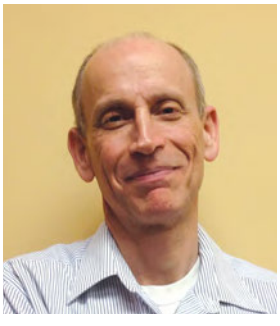
8 IPC: Connected Factory Initiative Subcommittee's Progress on Machine Data Interface Standard

Representatives of industry's leading manufacturers, machine, device, sensor and software companies that comprise IPC's 2-17 Connected Factory Initiative Subcommittee have made significant strides in developing a machine data interface standard, "Connected Factory Exchange or CFX."

9 Innovative Use of Vias for Density Improvements

In today's fast-paced global, economic environment—which requires constant innovation, upskilling, and performance improvements— there is a need for increasing density. The classic way to increase density is to reduce the trace and spacing.

10 Launch Letters: Programs, Not Projects



Sometimes, an uncontrollable tick in my neck emerges. The wrinkle in my forehead that now has no boundaries slowly makes its way to my balding scalp. My porcelain china doll-like complexion gradually transforms itself to resemble a Honeycrisp, and ultimately, a Red Delicious apple.

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Events

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Printed and Flexible Electronics China
January 11–13, 2017
Shanghai, China

46th NEPCON JAPAN
January 18–20, 2017
Tokyo Big Sight, Japan

DesignCon 2017
January 31–February 2, 2016
Santa Clara, California, USA

EIPC Winter Conference
February 2–3, 2017
Salzburg, Austria

MD&M West
February 7–9, 2017
Anaheim, California, USA

IPC APEX EXPO 2017 Conference and Exhibition
February 14–15, 2017
San Diego, California, USA

China International PCB & Assembly Show (CPCA)
March 7–9, 2017
Shanghai, China

14th Electronic Circuits World Convention
April 25–27, 2017
Goyang City, South Korea

KPCA Show 2017
April 25–27, 2017
Goyang City, South Korea

IMPACT Washington D.C. 2017
May 2–3, 2017
Washington, D.C. USA

Thailand PCB Expo 2017
May 11–13, 2017
Bangkok, Thailand

JPCA Show 2017
June 7–9, 2017
Tokyo, Japan

IPC Reliability Forum: Emerging Technologies
June 27–28, 2017
Düsseldorf, Germany

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

SALES: **ANGELA ALEXANDER**
(408) 489-8389; angela@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

EDITORIAL:
MANAGING EDITOR: **PATRICIA GOLDMAN**
(724) 299-8633; patty@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

MAGAZINE PRODUCTION CREW:
PRODUCTION MANAGER: **MIKE RADOGNA**
mike@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **MIKE RADOGNA, SHELLY STEIN, TOBEY MARSICOVETERE**

INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**

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EDITORIAL CONTACT

Patty Goldman
patty@iconnect007.com
+1 724.299.8633 GMT-4

SALES CONTACT

Barb Hockaday
barb@iconnect007.com
+1 916 365-1727 GMT-7

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